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► **To cite this version:**

Ali Beydoun, Philippe Benabes. BANDPASS / WIDEBAND ADC ARCHITECTURE USING PARALLEL DELTA SIGMA MODULATORS. 14th ESPC, Sep 2006, Italy. pp.CD-ROM Proceedings. hal-00229779

**HAL Id: hal-00229779**

**<https://centralesupelec.hal.science/hal-00229779>**

Submitted on 31 Jan 2008

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# BANDPASS / WIDEBAND ADC ARCHITECTURE USING PARALLEL DELTA SIGMA MODULATORS

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## ABSTRACT

This paper presents a new method for digitizing wideband signals. It is based on the use of parallel analog delta sigma modulators, where each modulator converts a part of the input signal band. A major benefit of the architecture is that it widens the conversion band of the input signal and increases its dynamic range. Two solutions are proposed to reconstruct the signal: the first one uses bandpass filters without demodulation and the second demodulates the signal of each modulator, and then processes it in a lowpass filter. This paper focuses essentially on the digital part of the system and the overall performances are compared by using simulation results.

## 1. INTRODUCTION

The current trend in telecommunication is high data rates, versatility and interoperability between digital mobile systems. Most of these systems are designed in a way that puts the digital processing as close to the antenna end of the receiver as possible in order to obtain a more robust system. This is due to the fact that a direct digitization of the Radio Frequency (RF) signal simplifies processing tasks like channel filtering and demodulation. In order to evolve in that direction, many problems must be handled such as: enlarging the frequency bandwidth of the analog to digital converter and improving technology efficiency (for instance using parallelism technology).

Recently, several solutions such as Time Interleaved Delta Sigma ( $T\Delta\Sigma$ ) [1] [2][3], Parallel Delta Sigma ( $\Pi\Delta\Sigma$ ) [4] and Frequency Band Decomposition (FBD) [5][6] have been proposed to widen the band of operation of the converters using discrete-time delta sigma modulators for their higher accuracy. These architectures are all based on the implementation of parallel delta sigma modulators but have two main drawbacks: first, the whole frequency band between 0 and  $f_s/2$  is converted,  $f_s$  being the sampling frequency, instead of the limited useful signal band. Moreover an increase in resolution implies an increase in the number of modulators and therefore a larger silicium area.

Finding a proper solution for this problem is the main goal of our method. Our architecture is able to convert a band-limited signal by using  $N$  parallel analog bandpass modulators, each of which processes an equal share of the useful signal band, as shown in Figure 1. By limiting the processing to the useful band, the resolution will be improved compared to the previous method using the same number of modulators.

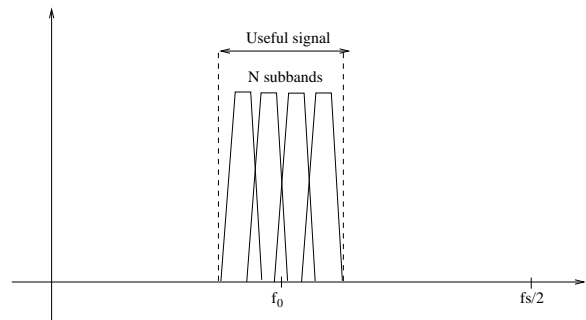


Figure 1: Decomposition of the input signal band

This combination of modulators must be followed by a digital system to reconstruct the signal with a transfer function as close as possible to a simple delay (minimum in-band ripple and linear phase). The remaining problem is the digital reconstruction of the input signal. In this paper, we consider that the characteristics of the modulators are known and we try to evaluate the computing power needed for this reconstruction. Even though, this processing cannot be achieved in real time today, this should become possible using near future technologies. We choose to separate phase issues in the transition zone between adjacent modulators from amplitude issues related to the Signal Transfer Function (STF) of each modulator and the quantization noise. An example with eight third order modulators will be given to illustrate the proposed architecture.

## 2. ARCHITECTURE

In order to widen the converter's band and increase the resolution, one may use parallel delta sigma modulators as in the architecture represented in Figure 2. In this case, the Oversampling Ratio (OSR) of each modulator is equal to the global OSR multiplied by  $N$ . The input signal is processed simultaneously by multiple analog delta sigma modulators as shown in part A. The outputs from all the channels are then recombined by a digital system (part B) in order to reconstruct the signal.

### 2.1 Analog modulators

Continuous-time modulators (Figure 2, part A) are used to overcome difficulties related to the frequency limitations of the discrete-time integrators that are built with switched capacitor circuits [7]. These modulators are uniformly dis-

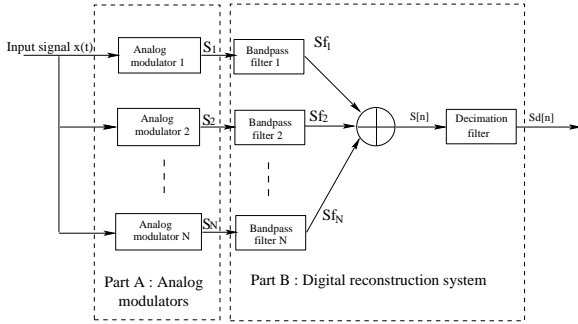


Figure 2: Wide band converter's architecture

tributed in the useful signal band. Each modulator forms a bandpass filter around its working band as it is shown in Figure 3.

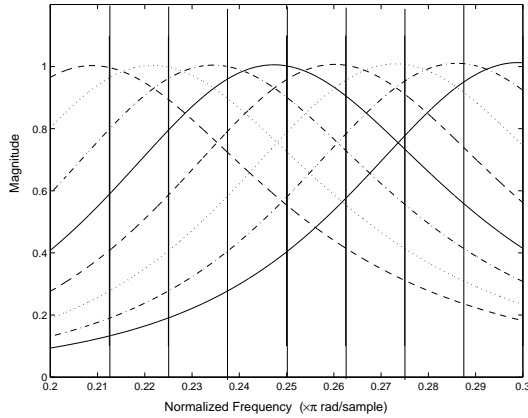


Figure 3: Signal Transfer Function of each modulator

## 2.2 Digital reconstruction

For reconstructing the signal, two conditions must be met by the digital system :

- A minimum global quantization noise which is equivalent to a minimum quantization noise outside every sub-band.
- A reconstruction of the output signal with as little in-band ripple as possible.

Two approaches may meet these criteria:

- Direct processing using bandpass filters.
- Digital demodulation followed by a decimation filter, and lowpass filter.

It is shown that (due to the decimation) the second solution has a better performance with the same number of filter coefficients.

### 2.2.1 Solution without demodulation (solution I)

This solution consists in reconstructing directly the signal by using a bandpass filter for each output  $S_k$  (Figure 2, part B). Then the outputs of all bandpass filters  $Sf_k$  are recombined to rebuild the signal. The signal is then decimated to decrease the signal data rate. This solution involves high order bandpass filters that complicates the digital process. For instance,

only an 11.5 bit resolution can be reached using an 8 modulator filter bank with 256 taps Hann bandpass FIR filters compared to an expected 14 bit resolution : 1024 coefficients would be required to reach this resolution, this implies enormous computing resources and makes this solution difficult to realize.

### 2.2.2 Solution with demodulation (solution II)

In this solution (Figure 4), the outputs of all the channels are digitally demodulated so that their frequency band is centred on zero. Because of the previous oversampling by the modulators, the outputs must be decimated to reduce the data rate. Then, each signal is processed by a lowpass filter, before being remodulated and recombined with the signals of all the other channels. The value of the maximum decimation factor is equal to the floor value of the global OSR, that is  $f_s/2B$ ,  $B$  being the input signal's bandwidth. The low-pass filters' transfer functions carry significantly fewer coefficients thanks to the decimation that eases the constraints on digital filters by widening the transition zone. The choice

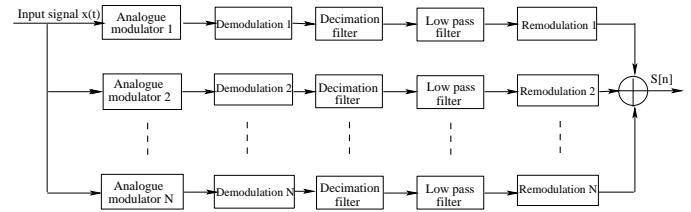


Figure 4: Digital processing with demodulation

of the window will influence the performance of the reconstruction and particularly the residual noise outside the band. This will be illustrated in section 4 by simulating three types of windows and comparing their results. Figure 5 represents the frequency response of the filters which are used in all of the channels, eight in this case, and also their sum. This sum shows a very weak ripple inside the frequency band, about  $10^{-3}$ , with attenuations on the edges as high as 6 dB. Note that the band is limited to  $[0 f_s/2]$  due to the decimation.

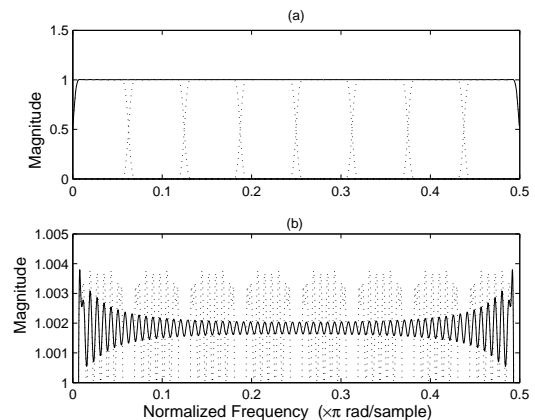


Figure 5: Frequency response for eight 128 taps Hamming FIR filters in the band (a) and a zoom on the ripples (b).

### 3. CORRECTION PROCESS

The STF of analog modulators is not a simple time-delay transfer function as in discrete-time modulators. However, it can be calculated and plotted if the input signal is band limited. During calibration that might be mandatory to adapt to the specifications of real modulators, we prefer to separate between amplitude correction of the STF, modulator phases alignment, decimation filter's amplitude correction and elements phase alignment in low frequency.

#### 3.1 Amplitude correction of the STF

As shown in Figure 3, the STF of each modulator is not flat in the band, but presents approximatively a parabolic form. A correction filter with three coefficients (Figure 6) is enough to flatten the STF.

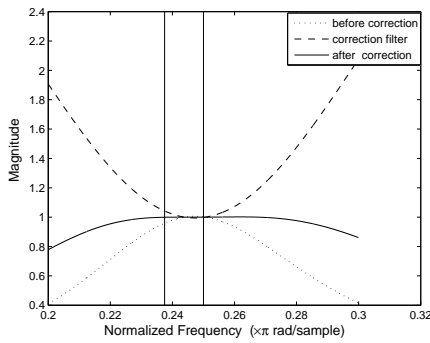


Figure 6: Signal Transfer Function for analog modulator before and after correction

#### 3.2 Modulator phases alignment

The delta sigma converters have an almost linear phase in the band around the central frequency (Figure 7.a). However, their phases are not connected in the transition zone. So a signal in the transition zone between two adjacent modulators will have two different phases which can influence the output signal. This phase mismatch is compensated for by multiplying the signal in each channel with a complex number which allows an almost linear phase in the full band that is being processed (Figure 7.b).

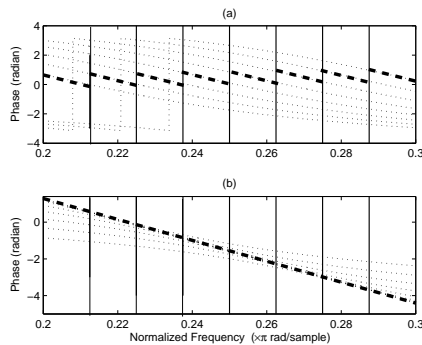


Figure 7: Delta sigma phases before correction (a) and after correction (b).

#### 3.3 Decimation filter's amplitude correction

The frequency response of the comb filter used for the decimation has a sinc shape, with a cut-off frequency of  $\frac{1}{N_d}$ ,  $N_d$  being the decimation factor. It is given by (1) :

$$H(e^{j\Omega}) = \left( \frac{1}{N_d} \frac{1 - (e^{j\Omega})^{N_d}}{1 - e^{-j\Omega}} \right)^{k+1} \quad (1)$$

$k$  : modulator's order

This filter is followed by a three-coefficient correction filter in order to obtain an almost flat gain limited by  $\frac{1}{N_d}$  and prevent the attenuation of the signal.

#### 3.4 Elements phase alignment in low frequency

The lowpass filters that are used, such as the decimation filters, have a linear phase. Due to demodulation and remodulation, the signals in the transition zone between two adjacent channels will have opposite phases. This creates in-band ripple in the output signal that can be countered by multiplying every channel by the complex number  $e^{-j\Delta\varphi}$ ,  $\Delta\varphi$  being the total band phase mismatch :

$$\Delta\varphi = \pi B(L-1) \quad (2)$$

$L$  : filter's length

#### 3.5 Integration in the main filter

Practically, the low pass filter following the decimation filter (Figure 4) includes all the elements that contribute to the previous corrections. Its frequency response is equal to the product of all contributing elements including the original lowpass filter.

## 4. MAIN RESULTS AND SIMULATIONS

To illustrate the discussion above, an architecture with eight third order modulators and a large band input signal are given as an example. The input signal is a cardinal sine and has a square limited band of  $320 \text{ MHz}$  centered around  $800 \text{ MHz}$  for a sampling frequency  $f_s = 3.2 \text{ GHz}$  which is equivalent to a normalized band  $B = [0.2 \ 0.3]$ . The resolution obtained by solution I with a 256 taps Hann bandpass FIR filters is 11.5 bits. On the other hand, solution II gives a 13.9 bit resolution by using 64 taps Hann lowpass FIR filters. Figure 8 represents the power spectral densities of the input signal, the output signal, and the output noise that are obtained with solution II. There is a slight difference on the edges of the spectral densities between the input signal and the output signal. This is related to the fact that the sum of lowpass filters responses is attenuated on the edges, (Figure 5), and that the ripple inside the band is about  $10^{-3}$  which doesn't decrease the signal's reconstruction.

The sampling frequency  $f_s$  is equal to  $4 \times f_0$ ,  $f_0$  being the central frequency of the useful signal's band. This choice facilitates the implementation of delta sigma modulators [8].

Figure 9 shows the evolution of the theoretical resolution as function of the number of modulators for different orders. It can be noticed that the resolution is increased by  $k$  bits every time the number of modulators is doubled,  $k$  being the order of the modulators. Even though, the improvement of resolution requires an increase in the number of modulators,

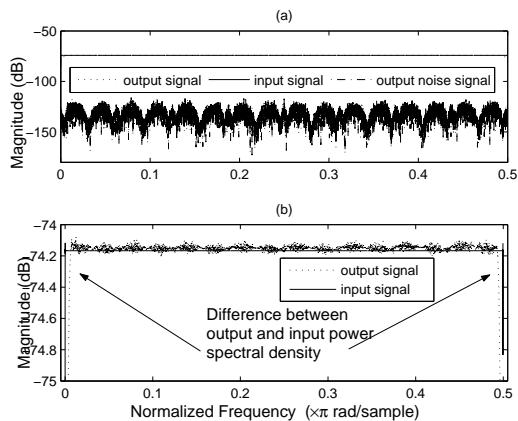


Figure 8: Power spectral density for output signal, input signal and output noise signal (a) and a larger view (b).

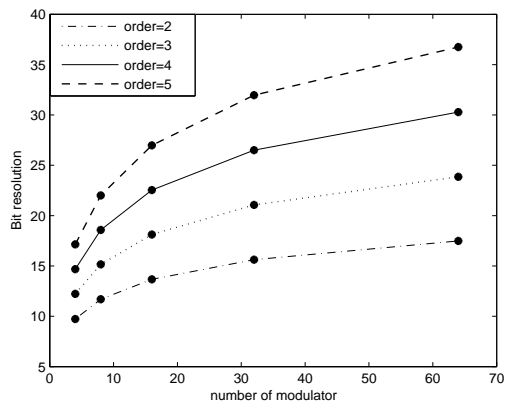


Figure 9: Theoretical resolution compared to number of modulator for different modulator orders.

the advantage of this architecture compared to the architectures proposed in [1]-[6] is the fact that to obtain the same resolution fewer modulators are required which means smaller silicon area. The resolution can be improved by increasing the order but this may lead to unstable modulators. The number of coefficients of the lowpass filters is carefully chosen in a way that does not decrease the overall performance.

Table 1 describes the loss of resolution compared to the one obtained with ideal lowpass filter (14.6 bits) according to the number of coefficients in the lowpass filters with three types of windows. One can notice that the best resolution is obtained with the Hann window due to its particular shape that attenuate the noise outside every subband. It is worth mentioning that after reaching a certain threshold (96 coefficients), increasing the number of coefficients doesn't improve the resolution more than 0.5 bits. In the previous example with a sampling frequency of  $10 \times B$ ,  $B$  being the input signal's band, and a decimation factor of 5, the problem is reduced to realizing 8 FIR filters with 64 coefficients each, that is 512 Multiply-Accumulate (MAC) operations at  $2 \times B$  frequency, in addition to the decimation and correction filters. To date, the maximum DSP performance available on the market is 8000 MIPS. The number of DSP needed in the

Table 1: Resolution loss with different windows

Number of coefficients	48	56	64	96	128	256
Resolution loss (bits), Hamming	-3.8	-3	-1	-0.5	-0.3	-0.1
Resolution loss (bits), Blackman	-1.7	-1.3	-1	-0.5	-0.3	-0.1
Resolution loss (bits), Hann	-1.2	-0.9	-0.7	-0.25	-0.15	-0.01

previous example (section 4) is 41. This number is too high to be applicable in current technologies. On the other hand, due to the silicon evolution, these computing resources will be soon available in a single chip.

## 5. CONCLUSION

This paper describes an architecture for limited wideband signal conversion that helps reaching the requirements for improving telecommunication systems. It is based on the use of analog modulators. Two solutions are proposed to reconstruct the input signal and have been tested by digital simulations. The results of these simulations further the adoption of the digital reconstruction with demodulation and decimation as it requires less computing resources. We also estimated the computing power needed for the implementation with future technology.

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