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Performance of subband HFB-based A/D converters

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Abstract—Subband Hybrid Filter Bank (HFB) structures may replace the classic ones in parallel A/D Converters (ADC). In this paper, subband and original HFB-based A/D converters are simulated and compared in the time domain. For this purpose, firstly a brief survey on subband HFB-based A/D converters is presented. According to the simulations, subband HFB-based ADC exhibits a lower sensitivity to realization errors than classic one. Besides, compensation techniques such as noise canceling may be used for correcting the analog imperfections of subband HFB. This is not possible for classic HFB. The output resolution of subband HFB-based ADC is shown to be better than the one related to classic architecture using FIR synthesis filters with the same order for some exemplary inputs. Computation complexity related to subband architecture is compared with the one due to classic structure. It may be seen that subband HFB-based ADC includes less computational complexity than the classic architecture if an adaptive compensation of analog imperfections is considered.

I. INTRODUCTION

The parallel structures of A/D converters may be applicable for wide-band analog signals [1]. The Hybrid Filter Bank (HFB) structure of A/D converters has been proposed as a candidate for realizing parallel A/D converters [2]. The original HFB-based ADC is shown in figure 1 [3]. Aliasing

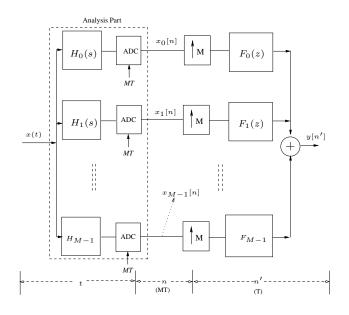


Fig. 1. The original architecture of M-channel maximally-decimated A/D converter using HFB structure. It consists of the analysis (analog) and synthesis (digital) filter banks.

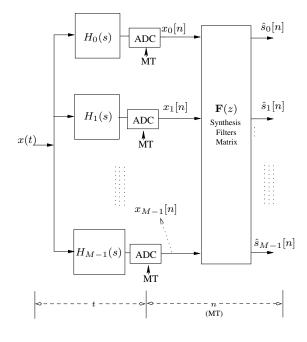


Fig. 2. The subband architecture of HFB-based A/D converter for estimating the subband components of input signal. The outputs $\hat{s}_0[n]$, $\hat{s}_1[n]$, ..., and $\hat{s}_{M-1}[n]$ are the estimated subband signals.

terms are interferences that restrict the resolution of classic HFB-based A/D converters [4]. HFB-based A/D converters may exhibit an acceptable resolution using FIR synthesis filters if a small oversampling ratio is used [5]. However, they are very sensitive to realization errors so that the output resolution reduces drastically when the analysis filters of HFB include even small errors [7]. Sensitivity to realization errors increases too when oversampling process is used [7]. Analog imperfections are unavoidable because of fabrication errors and ambient parameters such as temperature [6]. Subband HFB architecture has been recently proposed for A/D conversion as shown in figure 2 [8]. Based upon an LTI Multiple-Input Multiple-Output (MIMO) model of the analysis part, it uses a matrix of synthesis filters (Fig. 2). Subband HFB-based A/D converter behaves like a Frequency Division Multiplexing (FDM) receiver [8]. It assumes that the input signal is divided into M narrow-band signals. The decimated version of these signals are called subbands and are estimated as the outputs of the subband structure. The resolution of subband HFBbased ADC is limited by Inter-Channel Interference (ICI) terms [8]. The aim of this paper is to compare the performance of both original and subband HFB structures in terms of interference and sensitivity to realization errors. For this purpose, both structures have been simulated in time-domain using Simulink/MATLAB. To better focus on the aliasing and ICI interferences, the quantization noise is neglected in this paper [4]. In the next section, the subband HFB-based A/D converter is reviewed and the design method of its synthesis filters matrix is also described. Both (original and subband) HFB structures are simulated in time-domain in section III and the residual interferences are exhibited. Section III provides also a comparison between two architectures in terms of computational complexity, output resolution and sensitivity to realization errors. The two structures are discussed in terms of the capability according to which analog imperfections may be compensated as well. At last, the conclusion is summarized in section IV.

II. SUBBAND HFB-BASED A/D CONVERTER

Subband HFB structure has been proposed to provide a parallel A/D converter using analog analysis and digital synthesis filters [8]. It provides M output signals for an M-channel structure (Fig. 2). The outputs $\hat{s}_0[n], \hat{s}_1[n], ..., \hat{s}_{M-1}[n]$ are the estimated forms of M input subbands $s_0[n], s_1[n], ..., s_{M-1}[n]$. These outputs are associated with the sampling rate $\frac{1}{MT}$ where $\frac{1}{T}$ stands for the overall sampling rate. It is supposed that the wide-band input x(t) always respects the Nyquist criterion to avoid any spectral overlapping. Figure 3

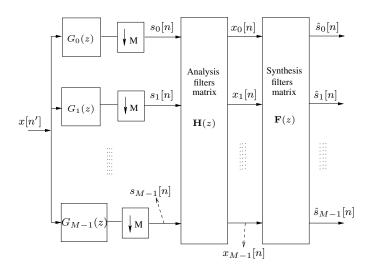


Fig. 3. The discrete-time model of subband HFB-based A/D converter. Analysis part has been modeled using virtual subband filters $G_k(z)$.

exhibits schematically the model of subband HFB-based A/D converter in discrete-time domain when the quantization noise of ADCs is neglected [8]. The input subbands $s_0[n],...$, and $s_{M-1}[n]$ may be virtually extracted from the original analog input x(t) (Fig. 3). Each subband filter $G_k(e^{j\omega})$ ($0 \le k \le M - 1$) is a virtual filter with the following definition for

 $|\omega| \leq \pi$ [8]:

$$G_k(e^{j\omega}) = \begin{cases} 1 & k\frac{\pi}{M} \le |\omega| \le (k+1)\frac{\pi}{M} \\ 0 & else \end{cases}$$
(1)

The analysis filter matrix $\mathbf{H}(z)$ includes M^2 digital filters which are obtained from the original analog analysis filters [8]. For obtaining the elements of $\mathbf{H}(z)$, the intermediate digital filter $H_k(e^{j\omega})$ is defined in terms of analog analysis filter $H_k(j\Omega)$ as following:

$$H_k(e^{j\omega}) = \frac{1}{T} \sum_{m=-\infty}^{+\infty} \check{H}_k(j\Omega - \frac{2\pi}{T}m) \Big|_{\Omega = \frac{\omega}{T}}$$
(2)

where,

$$\check{H}_{k}(j\Omega) = \begin{cases} H_{k}(j\Omega) & \Omega \in \left[-\frac{\pi}{T}, +\frac{\pi}{T}\right] \\ 0 & elsewhere \end{cases}$$

 $H_{k,r}(e^{j\omega})$ is the $(k,r)^{th}$ element of $\mathbf{H}(z)$. It is associated with the k^{th} analysis filter $H_k(j\Omega)$. If r is even (r = 0, 2, ...), it is described as:

$$H_{k,r}(e^{j\omega}) = \begin{cases} \frac{1}{M} H_k(e^{j\frac{\omega}{M} + jr\frac{\pi}{M}}) & \omega \in [0,\pi] \\ \\ \frac{1}{M} H_k(e^{j\frac{\omega}{M} - jr\frac{\pi}{M}}) & \omega \in [-\pi,0] \end{cases}$$
(3)

and in the odd case (r = 1, 3, ...), it is:

$$H_{k,r}(e^{j\omega}) = \begin{cases} \frac{1}{M} H_k(e^{j\frac{\omega}{M} - j(r+1)\frac{\pi}{M}}) & \omega \in [0,\pi] \\ \frac{1}{M} H_k(e^{j\frac{\omega}{M} + j(r+1)\frac{\pi}{M}}) & \omega \in [-\pi,0] \end{cases}$$
(4)

 $H_k(e^{j\omega})$ is obtained from the analog analysis filter $H_k(j\Omega)$ according to (2). So, the analysis filter matrix $\mathbf{H}(z)$ is obtained. To design the matrix of synthesis filters, Perfect Reconstruction (PR) conditions are considered. If $\mathbf{F}(e^{j\omega})$ represents the synthesis filters matrix, the PR equation will be:

$$\mathbf{F}(e^{j\omega}).\mathbf{H}(e^{j\omega}) = \mathbf{I}.e^{-j\omega n_d}$$
(5)

where I is the $M \times M$ identity matrix and n_d stands for an arbitrary delay. n_d has been considered for maintaining the causality of synthesis filters. Using Least Squares (LS) optimization, the equation 5 leads to the following solution at each frequency ω :

$$\mathbf{F}(e^{j\omega}) = e^{-j\omega n_d} \mathbf{H}^H(e^{j\omega}) \left(\mathbf{H}(e^{j\omega}) \mathbf{H}^H(e^{j\omega}) \right)^{-1}$$
(6)

where superscript $(.)^{H}$ stands for conjugate-transpose operation. This relation may be established for N frequency points (N >> 1) [5]. Thus, the frequency response of each synthesis filter $F_{ij}(e^{j\omega})$ is obtained using (6). An FIR filter may be considered for estimating the $(i, j)^{th}$ element $F_{i,j}(e^{j\omega})$ of the synthesis filters matrix. Using FIR estimation of synthesis filters, the equality (5) does not hold exactly. So:

$$\mathbf{T}(e^{j\omega}) = \mathbf{F}(e^{j\omega})\mathbf{H}(e^{j\omega}) \tag{7}$$

This exhibits that the k^{th} output $\hat{s}_k[n]$ may be described in the frequency domain as:

$$\hat{S}_k(e^{j\omega}) = T_{k,k}(e^{j\omega})S_k(e^{j\omega}) + \sum_{m=0,m\neq k}^{M-1} T_{k,m}(e^{j\omega})S_m(e^{j\omega})$$
(8)

where $T_{k,k}(e^{j\omega})$ is the distortion function and $T_{k,m}(e^{j\omega})$ is the ICI component related to the m^{th} subband input. ICI terms are similar to aliasing terms considered in the original HFB structure. The output resolution is restricted by ICI and aliasing terms for subband and classic architectures respectively.

III. MAIN RESULTS

In this section, the PR equation will be used for design of synthesis filters. To implement the HFB structures, a simply realizable analysis filter bank is considered and FIR synthesis filters are designed. Assuming an 8-channel HFB, the analysis filter bank includes an RC (first-order) circuit along with seven RLC (second-order) circuits. Using this set of analysis filters, the analysis filter matrix has been calculated according to (3) and (4). Then, synthesis filter bank is obtained using (6). Each element $F_{i,j}(e^{j\omega})$ of the synthesis filters matrix may be approximated by an FIR synthesis filter. In the subband case, some percents of each subband are considered as guard band to provide an acceptable performance [8]. In this paper, guard band ratio is supposed to be 10%. The optimum value of oversampling ratio (7%) is also used for the classic HFB case [7].

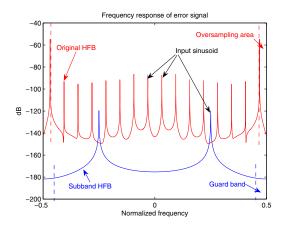


Fig. 4. The FT of error signal (dB) versus normalized frequencies for original and subband HFB-based ADC. Analog input is a sinusoidal signal at the first subband. Each FIR synthesis filter has 64 coefficients. There is a shift in the frequency of input sinusoid due to subband HFB because related output is decimated.

Resolution

Both structures have been simulated in time-domain considering different input signals. Considering a sinusoidal signal at the frequency $0.5 \frac{\pi}{8T}$ (in the middle of first subband), the Fourier Transform (FT) of the error signal is shown in figure 4. All outputs of subband structure are null except the output of the first one $\hat{s}_0[n]$. It may be seen that there is only one

peak (at positive frequencies) in the error signal due to the subband architecture. It is associated with the input sinusoid frequency with a shift in the frequency domain because of decimation. However, the error signal due to the original structure includes eight (M = 8) error peaks (Fig. 4). In other words, it may be interpreted that the error related to one input subband appears at the other M - 1 subbands on the output of M-channel original HFB-based ADC. To better compare the output resolutions, a chirp signal is also considered as input. The frequency of this chirp is swept between $0.1 \frac{\pi}{8T}$ and $0.9 \frac{7\pi}{8T}$. The outputs of subband HFB-based ADC are null except for the first subband. Figure 5 illustrates the FT of

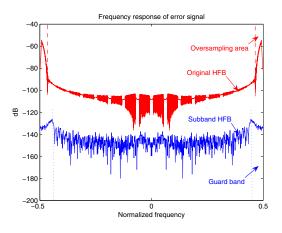


Fig. 5. The FT of error signal (dB) versus normalized frequencies for original and subband HFB-based ADC considering a chirp as input signal. The oversampling and guard band ratios are 7% and 10% respectively.

the error signal versus the normalized frequencies for original and subband structures using FIR synthesis filters with 64 coefficients. It shows that post-filtering is essential for original HFB to suppress the oversampling band (here $|f| \ge 0.9\frac{7\pi}{2T}$) even though there is no input component in oversampling area (Fig. 5). The output resolutions of the two structures are shown in table I for FIR synthesis filters with 64 and 128 coefficients. The resolution due to the original HFB is related to the case where post-filtering has been applied. It may be seen that subband HFB-based ADC provides a better resolution than the original structure supposing FIR synthesis filters with the same order.

TABLE IResolution of HFB-based ADC assuming a chirp signal asinput(L represents the number of coefficients for FIRSynthesis filters).

Resolution (bits)		
Structure	L=64	L=128
Original HFB	9.5	11.2
Subband HFB	17.6	20

• Sensitivity analysis

The electronic elements are often associated with a nominal value plus a deviation or realization error. The subband and original structures have been simulated considering Gaussiandistributed realization errors for the electronic elements of analysis filter bank. The simulations were repeated for 1000 trials of random mutually-independent realization errors. Analog input signal consists of eight sinusoidal signals which cover the whole spectrum so that there is one sinusoid at the middle of each subband. Figure 6 shows the average resolution

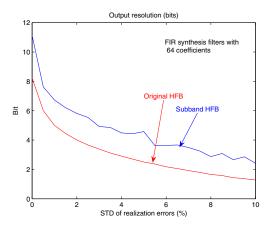


Fig. 6. The resolution (bits) of original and subband HFB-based ADC versus STD of realization errors. Gaussian errors have been applied to analysis filters. FIR synthesis filter bank includes 64 coefficients.

of each HFB structure versus STandard Deviation (STD) of error distribution using 64 coefficients for FIR synthesis filters. It may be seen that the sensitivity of subband HFB-based A/D converter to realization errors is less than the one related to the classic architecture. Some correcting methods such as blind deconvolution and noise canceling may be used for digitally compensating the realization errors [9]. Those methods may be applied to the subband HFB because input and output are related through an LTI relation (Fig. 3). This is not valid for the original HFB since there is a time-varying operation of decimation between its input and output [8]. Compensation techniques may even provide a better resolution in the case of no realization error for subband architecture using the outputs of the other subbands.

• Computational complexity

The classic HFB-based A/D converter consists of M FIR synthesis filters, but the subband architecture needs M^2 ones (see figures 1 and 2). For an FIR filter with L coefficients, L multiplying operations and delay components are effectively necessary. Then, for implementing the synthesis stage, subband architecture will need M^2L multiplications to be compared with ML ones in the classic case. Although, it does not require the upsampling operations (zero-padding by M). To compare the computational complexity, one has also to consider the design phase from which FIR synthesis filters are designed. Assuming N frequency points for the design of the synthesis filters, original HFB structure would require the

inversion of an $MN \times MN$ matrix [5]. The subband HFB needs the inversion operation of N matrices of $M \times M$ [8]. In practice, N must be much larger than M (N >> M) to have an acceptable interpolation. Thus, the design phase of subband architecture is obviously much more complex than the classic one. The complexity of the design phase is particularly important when an adaptive method is applied to estimate the real analysis filter bank for compensating realization errors. For example, the design phase of synthesis filters has to be regularly repeated to compensate the variations due to temperature. Accordingly, subband HFB-based ADC may be preferred to the original structure when realization errors are regularly compensated.

IV. CONCLUSION

In this paper, a brief survey on the subband HFB-based A/D converters was presented. The Perfect Reconstruction (PR) conditions related to this architecture were expressed, and ICI terms associated with each subband signal were formulated as well as the distortion function. The subband HFB structure of A/D converters has been compared with the original architecture. It was shown that subband HFB may provide a better resolution than original architecture for exemplary inputs of sinusoidal and chirp signals. Subband HFB also exhibits a lower sensitivity to realization errors than original HFB structure. However, it is necessary to mention that subband HFBbased ADC may include a digital compensation stage using some techniques such as noise canceling. This is not applicable for original HFB-based A/D converters. Subband HFB-based A/D converters require M^2 FIR filters in the synthesis stage but the original architecture uses only M FIR synthesis filters. Nevertheless, the overall computational complexity of subband HFB-based A/D converters is lower than the one related to original architecture if a regular compensation of realization errors is considered.

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