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***Abstract*—A low-input voltage high-power realization is presented with the aim to demonstrate the feasibility and the interest of topologies using intercell transformer. They constitute a promising option to interleave converter stages, and therefore, can answer to the specifications considered in this paper. These specifications require a galvanic insulation and the chosen topology is the Intercell Transformer (ICT) flyback converter, previously proposed by the authors. In a first part, the operating principle of the ICT flyback converter is recalled. The second part presents briefly the main features of the intercell transformer design, more precisely described in a previous paper. This part includes a discussion about the choice of the cell number. The last part presents the design and the implementation of the complete flyback converter using eight cells. A preliminary work concerns the choice, the design, and the test of each cell elements, mainly the transformer and the primary switching stage. In the end, the experimental results are presented and discussed. They demonstrate the potential of this original topology that needs only one level of magnetic components. Considering the suitability of the converter interleaving for the high-power–low-voltage applications, the ICT flyback converter constitutes a good candidate in that field.**

***Index Terms*—Coupled inductors, flyback, intercell transformer, interleaved converters, interphase transformers.**

I. Introduction

INTERLEAVED multicell converters are now widely used, especially for low-voltage/high-current applications. Among which voltage regulator module (VRM) is probably the most prominent example. Other emerging applications fields of these topologies are provided by systems connected to low-voltage energy sources and storage elements as photovoltaic (PV) arrays, fuel cells, batteries, ultracapacitors [1]–[5], especially when these systems are onboard and weight and space savings are required.

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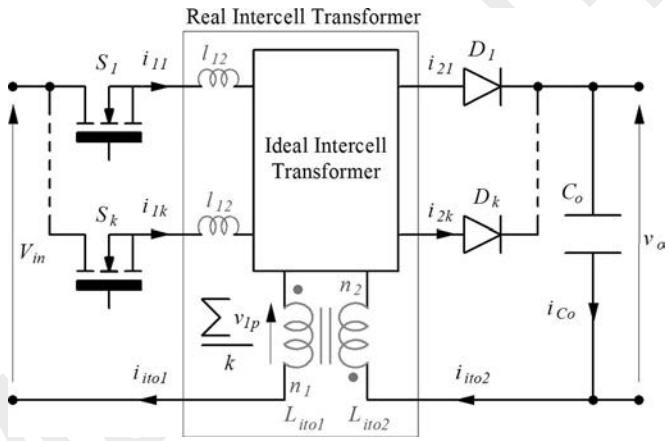

Fig. 1. General topology of the ICT flyback converter.

The aim of this paper is to present the design and implementation of a converter with a high power density; the main function is to feed a 12 kW/300 V load from the 28 Vdc of an embedded network with galvanic insulation.

The specifications of this converter for the considered application are as follows.

1) Input voltage: 28 Vdc.
2) Output voltage 300 Vdc.
3) Output power: 12 kW.
4) Weight: to be minimized.

These specifications lead the authors to design an original converter, the ICT-based multicell flyback. This topology recently described in [6], seems in adequation with such specifications, but its relatively complex operation requires developing a specific know-how; the authors have thus tried to push the design one step further to evaluate more precisely the potential of this topology.

In the first section, the basic properties of ICT-based multicell flyback are recalled.

Other points of interest such as the design of the ICTs and the number of cells are then discussed in a second section.

Last, the different steps of the design and the experimental results are described.

II. ICT Flyback Converter Topology

The ICT flyback converter has been detailed in [6]. Fig. 1 displays the topology of such an ICT flyback converter with k cells.

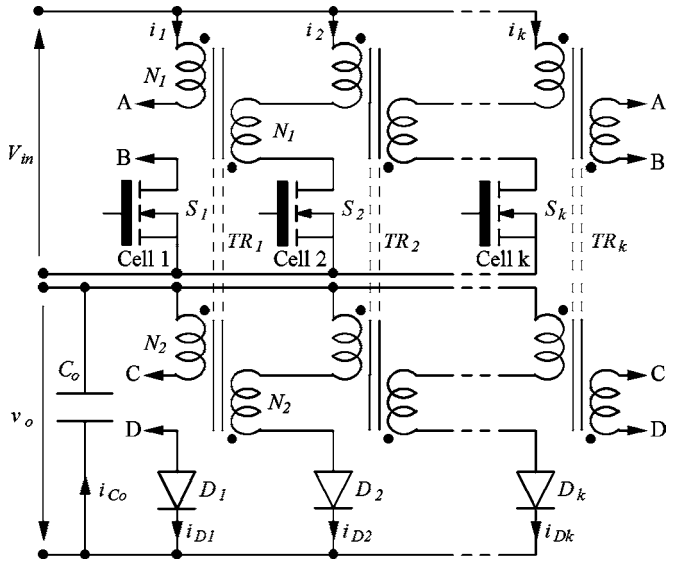

Fig. 2. ICT flyback converter with separated transformers (*T* switching period, $i_{\rm ito} = i_{\rm ito1} + n_2/n_1\ i_{\rm ito2}$).

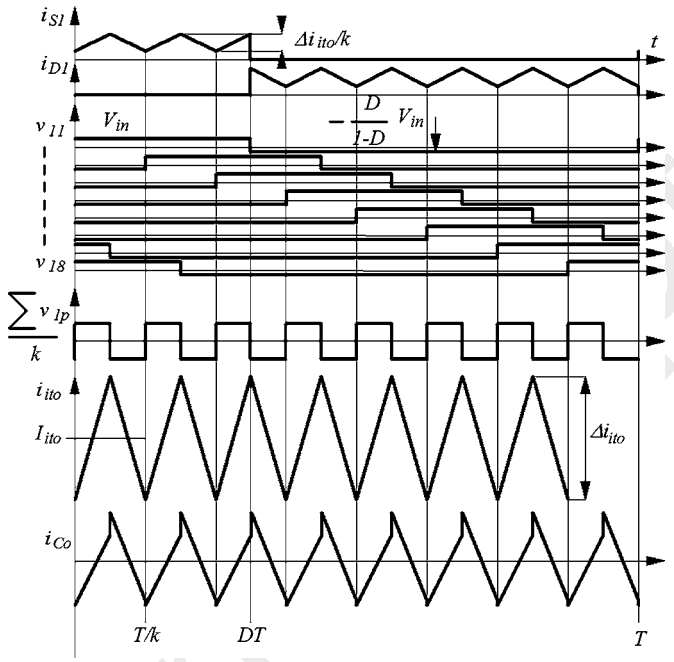

Fig. 3. Theoretical waveforms of the ICT flyback converter (*F* switching frequency).

It has been shown that ICTs can be implemented either as monolithic devices or as separate devices [7]–[9]. The second form is used in this paper, according to the circuit shown in Fig. 2. Each elementary transformer comprises four windings (two primaries and two secondaries), so that *k* such devices can be arranged to form a *k*-phase ICT. In this configuration, the storage inductance $L_{\rm ito1}$ (respectively, $L_{\rm ito2}$) required for the flyback operation is the leakage inductance between the two primary windings (respectively, secondary). To clarify next sections, this leakage inductance will be named in the following ICT common-mode inductance. The leakage inductances shown in Fig. 1 (l_{12}) are related to the coupling coefficient between homologous primary and secondary windings.

Interleaving the control signal of the switches produces the waveforms shown in Fig. 3. These waveforms are given for the eight-cell configuration, which is chosen in the last section of this paper. Due to interleaving and relatively high number of cells, a low value of the storage inductance can be used. Building the transformer so as to obtain an ICT common-mode inductance that is only slightly above the minimum feasible leakage inductance, the continuous conduction mode of the flyback is obtained. An optimal flyback ICT with a very low dc flux and no air gap is thus obtained. Its design is almost only related to the ac components, and is therefore, similar to a transformer design.

The evolution of the current ripple versus the duty cycle is given in Fig. 4, which still relates to an eight-cell design. Like other interleaved converters, the current ripple is minimized for duty cycles multiple of 1/*k*, but unlike interleaved buck converters, the local maxima are different

$$\Delta i_{\rm ito} = \frac{[kD - q + 1]\,[q - kD]}{1 - D}\frac{V_{\rm in}}{k^2 L_{\rm ito} F}.$$

III. General Features of the Design

A. ICT

The design of ICT is somewhat specific especially because of the shape and the distribution of the currents among the different windings, as explained in [10]. This is summarized in Fig. 5 related to transformer $\rm TR_2$. Since planar transformers are to be used, the four windings should be stacked vertically with an interval of height h_a separating the windings of one phase from the windings of the other phase. The interval allows choosing the coupling between phases and thus the ICT common-mode inductance (the storage inductance).

For one phase, the ac ampere turns can be split in two components: the differential-mode and common-mode components. As can be seen from the waveforms in Fig. 5, the differential-mode components of currents i_k and i_{Dk} are in opposition like in a standard transformer. A 1-D model including eddy-current effects can thus be applied to calculate the copper losses in each of the two groups i_1, i_{D1} and i_2, i_{D2}. The losses in the two groups are identical. The common-mode components have the same amplitudes in all four windings but they have different signs. The 1-D approach still applies if an equivalent primary composed the two windings of phase 1 and an equivalent secondary composed the two windings of phase 2 are considered. The total joule losses are then the sum of the losses generated by the two components (differential mode and common mode), and are thus, easily calculated.

A complete design method of the ICT has been presented in [10]. It involves deriving from the specifications (power, ambient temperature, frequency, current ripple, winding geometry, etc.), the core and copper losses, the heat exchange area, the operating

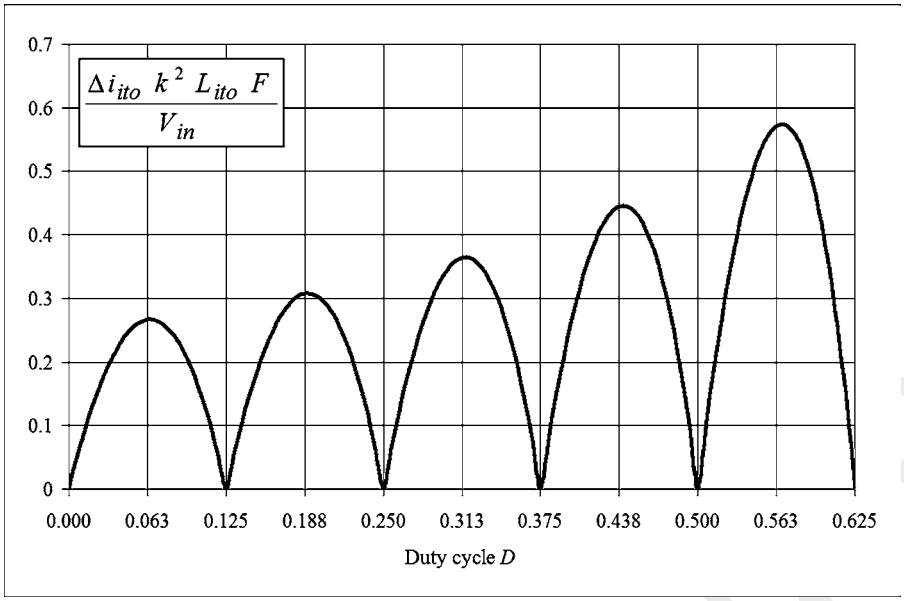

Fig. 4. Current ripple in ICT flyback converter (example of eight cells).

temperature and, in the end, the number of turns and all the dimensions of the ICT.

B. Number of Cells

The choice of the number of cells is another crucial point of the design. Using the method described in [10], several designs have been made for different number of cells and switching frequencies. This preliminary study has been made with the specifications of the application described in the last section of the present paper, namely $V_{\rm in} = 28$ V, $V_{\rm out} = 300$ V and a power of 12 kW. Planar cores are *a priori* chosen, because they are compatible with the high power density specification.

On the other hand, it is difficult to obtain high values of leakage inductance with these cores, and a relatively high current ripple is used in the chosen design. A standard ferrite material has been selected in accordance with the frequency.

The key characteristics of these designs are represented in Fig. 6. The first set of curves gives the total volume of the k transformers, each of them comprising a planar $E + I$ core and four windings. The characteristic dimension is the width of the core, which is generally used as a reference by ferrite manufacturers. The discretization of existing cores is not accounted for in the design routine (in this case relevant standard dimensions are 64, 58, and 43 mm).

These first curves show that with eight cells or more, the total volume is acceptable and that it is possible to use standard core EI 58. Using nine cells still does not allow using standard cores one size smaller (43 mm).

The second set of curves gives the estimated total losses in the k cells as well as the value of $k_a = h_a/l_w$ (see Fig. 7) giving a current ripple of 50%. Once again, no significant gain is obtained when increasing the cell number to more than eight.

It should also be noted that reasonable k_a values are rapidly obtained. Above 70 kHz, the intrinsic leakages are enough for storage, which reveals a great similarity with the design of a standard transformer.

Based on these results, eight cells are used in the implementation described in the next section. The choice of an even number of cells allows a symmetrical layout, which is generally an advantage. The switching frequency is kept relatively low (50–60 kHz), which gives similar results and reduces the design problems associated with the switching stages.

IV. Design of the 28 V-to-300 V/12 kW ICT Flyback Converter

Designing an ICT flyback converter for these specifications has been decided with two aims in view: demonstration of the feasibility of this topology, and evaluation of its performance in this low-voltage high-power context for which paralleling converters or cells is quasi-compulsory.

Because of the relative complexity of the complete converter, a first step was to design and test the elements of a single cell, namely, an elementary transformer and a commutation cell of 1500 W (12 kW/8).

A. ICT

The design of the elementary ICT has been initiated using the general results presented in Section III-B. Then, additional implementation constraints of the windings have been taken into account. The elements of this design are summarized in Table I.

The two primary windings are made of a single and massive layer of copper with a thickness of 0.8 mm. As shown in Fig. 7, these windings are sandwiched between two halves of secondary windings with six turns each.

The two halves of secondary windings are made using a PCB technology. For the first prototype, double-sided epoxy PCB isolated with a Kapton foil was assembled to form the complete winding [see Fig. 8(a)]. For the final device, the two halves of

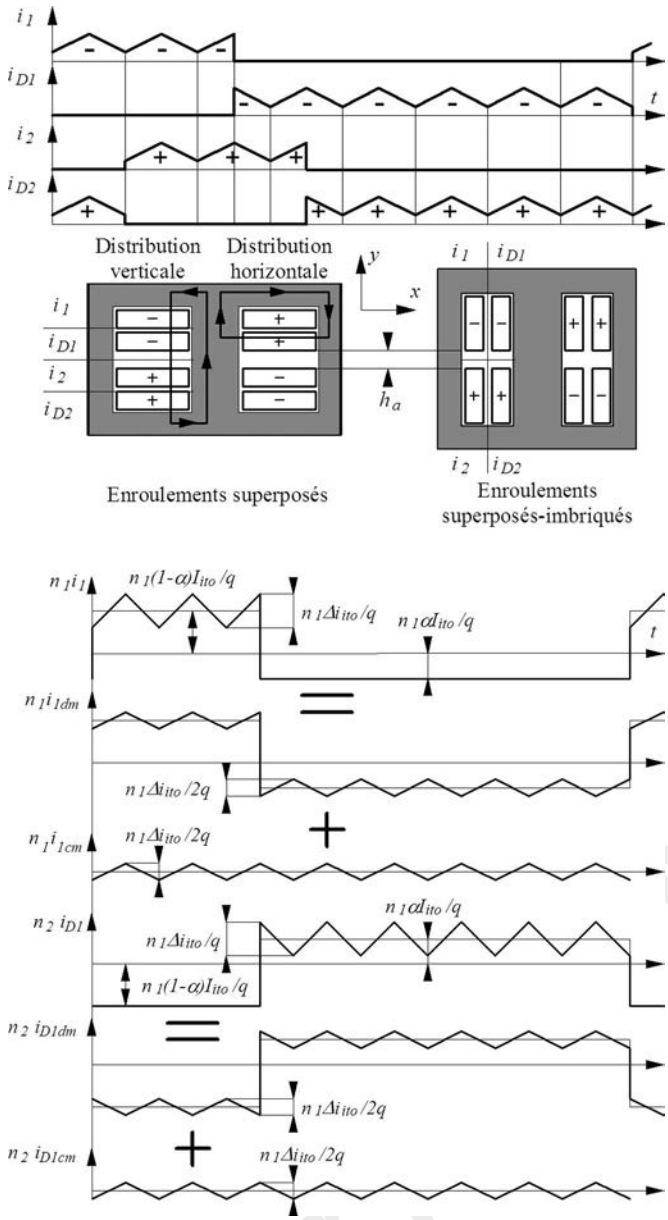

Fig. 5. Current distributions in the windings of ICT.

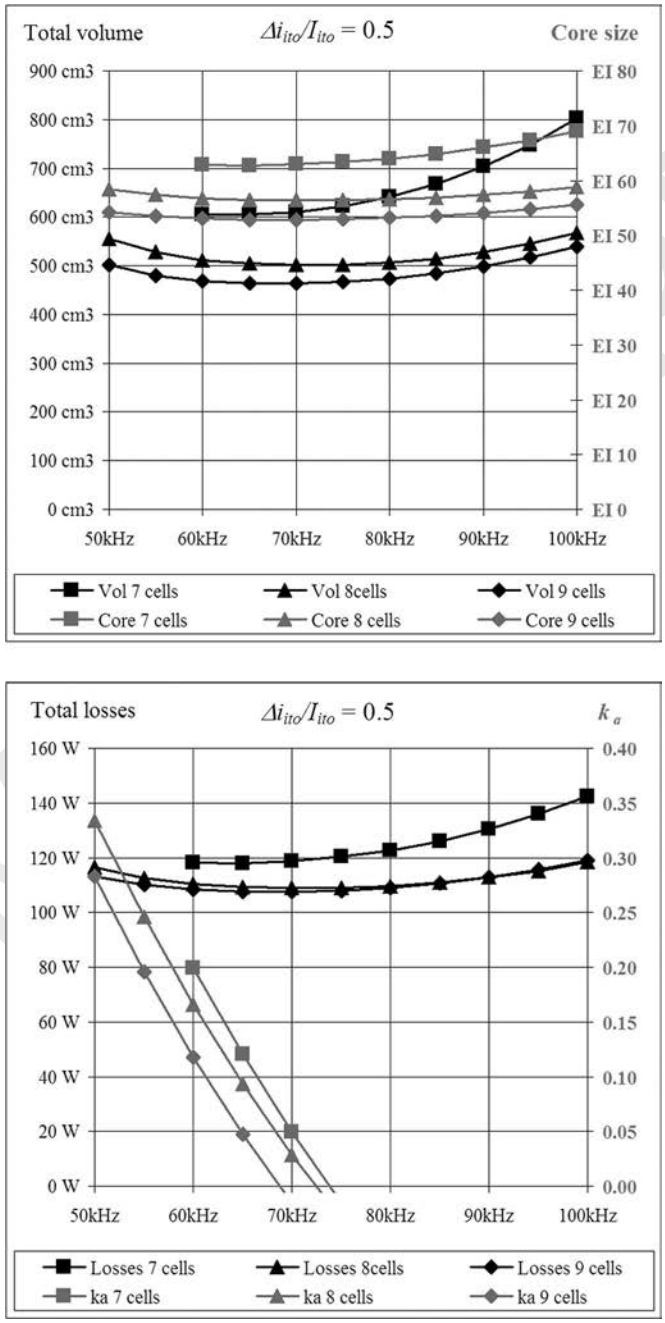

Fig. 6. Influence of the cell number.

secondary windings have been made using a multilayer PCB with a Kapton base [see Fig. 8(b)].

An experimental setup described in [10] made it possible to generate currents with the same characteristics as those of the actual converter and to test the prototype cell. The results obtained confirmed the design and the technology to be used.

B. Primary Switching Stages

The implementation of low voltage high current is never easy. In this case, 150 A needs to be switched under a theoretical voltage of 60 V. Like for the ICT, a switching stage has been designed, implemented, and tested in order to check the final design of the elementary commutation cell.

The aim is not only to minimize the turn-off losses, but also to recover the energy stored in the leakage inductance of the

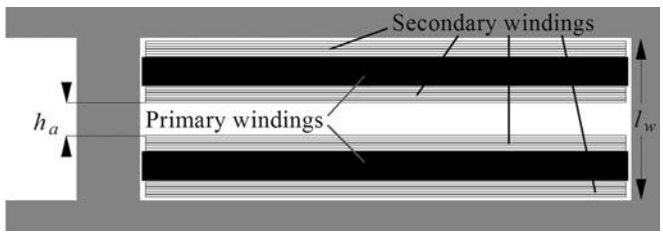

Fig. 7. Winding arrangement.

TABLE I
ICT DESIGN

E+I 58 planar, ferrite N87, ΔT = 60°C			
P = 1.5kW	F = 51kHz	ΔB_M = 0.22T	J_{RMS}=5A/mm²
P_{core} = 4.5W	P_{wind} = 9.5W	k_a = 0.26,	$\Delta i_{ito}/I_{ito}$ = 0.53
primary layer (2 x 1 turn) 19mm x 0.8mm		secondary layers (4 x 6 turns) 19mm x 0.07mm	

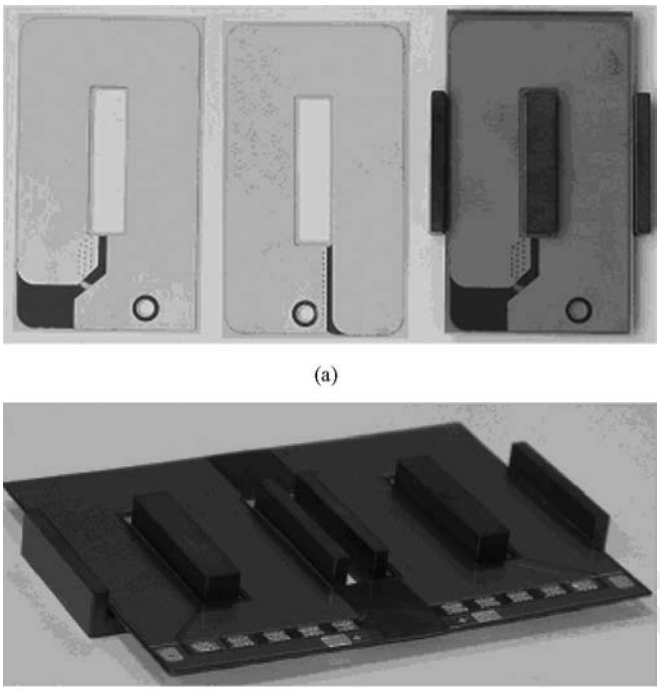

Fig. 8. Secondary windings. (a) Secondary windings of the test ICT. (b) Final secondary windings.

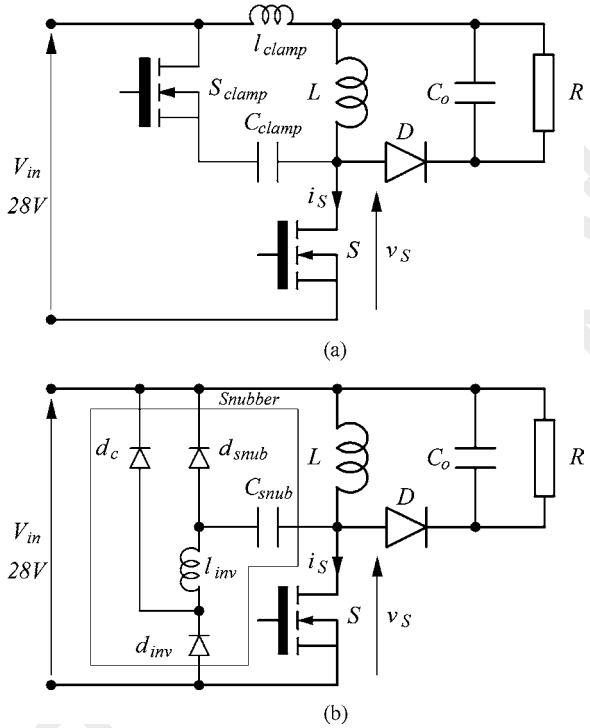

Fig. 9. Switching stages. (a) Active clamp. (b) Nondissipative snubber.

ICT and in the connexions stray inductance. The equivalent inductance is estimated to be 100 nH per cell, which would amount to 60 W of losses per cell if not recovered.

Two options have been considered, the active clamp [see Fig. 9(a)] and the nondissipative snubber [see Fig. 9(b)] [11]–[16]. These solutions have been evaluated in a buck–boost configuration that recreates the conditions of the flyback while making the preliminary test described further on easier. Various simulations and tests have been made to compare these two options.

The first one turns out to be pretty bad fit for low voltage and this switching frequency. The values of the reactive components are quite high; several tens of microfarads for the clamp capacitor when a 1-μH inductor is used, which is a bulky capacitor if we consider the high-rms current. In addition, the clamp switch also flows a very high current.

The main advantage of the nondissipative snubber is that the values of the different components are not related to the switching frequency. A simple 2 μF allows recovering the leakage energy and the inverting inductor (2 μH) flows a current that is way smaller than the switch current. This solution was finally chosen for the complete system. It should be noted that the active clamp becomes attractive again if the switching frequency and the input voltage are increased.

This solution has been tested by simulation in a complete eight-cell converter to measure the influence of the coupling. A result is shown in Fig. 10. Although the snubber slightly modifies the waveforms, we came to the conclusion that it is compatible with the multicell topology.

The circuit shown in Fig. 9(b) has been implemented using the power MOSFET selected for the final converter (IXUN350N10, ISOTOP package, $V_{\mathrm{DSS}} = 100$ V, $I_{\mathrm{dc}}(25^{\circ}\mathrm{C}) = 350$ A, $R_{\mathrm{DSON}}(25^{\circ}\mathrm{C}) = 1.9$ mΩ). Fig. 11 shows the final implantation of a switching cell that gives an idea of the snubber component sizes. Each cell also includes two dc-bus capacitors (2×6.8 μF). Consequently, the total value of the distributed dc-bus capacitor is 109 μF.

This setup was successfully tested using a very compact layout and using ceramic capacitors. An experimental result is shown in Fig. 12.

C. Secondary Rectifier

The first design planed the use of one 1200 V–10 A PIN diode per cell. In fact, this solution leads to unacceptable recovery losses. The current solution uses two series-connected 600 V–12 A diodes associated with parallel *R–C* balancing circuits. PIN diodes and SiC diodes will be tested. Despite the addition of two voltage drops, this second configuration is more efficient due to the drastic reduction of recovery losses (see Table II and Section IV-F).

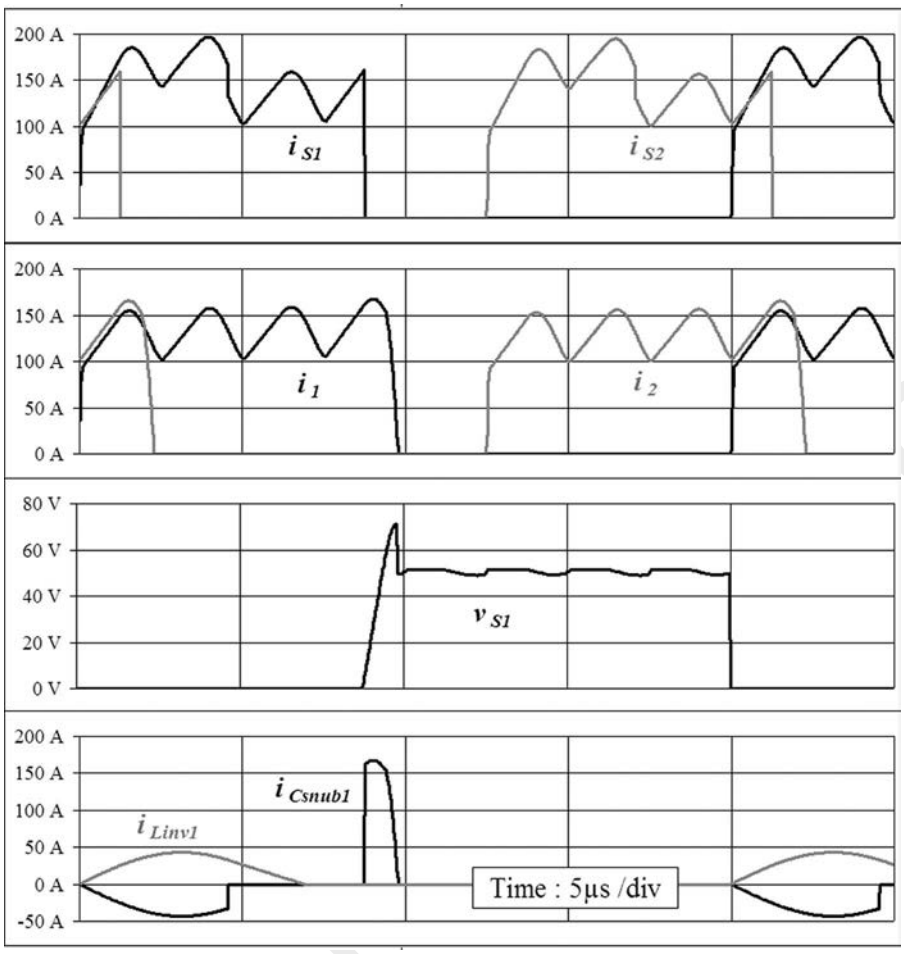

Fig. 10. Simulation of the eight-cell converter with nondissipative snubbers.

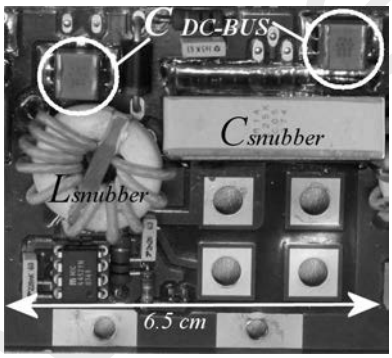

Fig. 11. Top-view of the final switching cell implantation.

D. Mechanical and Thermal Assembly

The mechanical and thermal assembly has been designed in the aim to maximize the power density, mainly by optimizing the positioning of discrete and standard devices [17]–[19]. The eight-cell converter has been built using a liquid-cooled cold plate with a 1 kW handling capability. All semiconductors and ICTs are mounted on this plate. All electrical connections are made using a PCB except for the primary windings and the 28 V busbar.

Fig. 13 shows a preliminary 3-D CAD view and a picture of the actual converter. The overall size is 23 cm × 20 cm × 5 cm, which gives a specific power of 4.5 kW/*l*.

E. Control Stage

Different digital solutions can be used to realize a multicell control stage [20]–[22]. The present one is made using a field-programmable gate array (FPGA) that precisely tunes the duty cycles of the different cells. This is required to balance the currents in the different cells in open loop and allows the validation that is made here. A closed-loop configuration is currently in progress using the same control system. Different techniques exist to realize the current balancing of multiparallel interleaved converters [21]–[23]. For example, VRMs using ICTs, with high number of cells and current-controlled, are now mounted on motherboards to supply the CPU. Therefore, the feasibility of such topologies operating in closed loop has been demonstrated. The aim of the development concerning the ICT flyback converter is to implement the simplest closed-loop solution, especially in regard with the number of sensors.

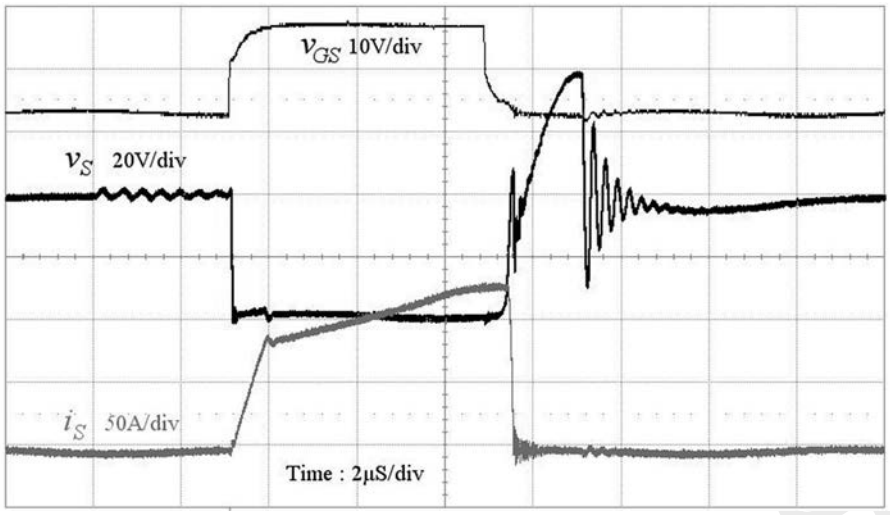

Fig. 12. Nondissipative snubber—experimental results on a buck–boost.

TABLE II
LOSSES ESTIMATION

	Secondary configuration	
Estimated losse parts	**Rectifier Diodes 1 x 1200V-10A**	**Rectifier Diodes 2 x 600V-10A**
On-losses in MOSFETs	300W	300W
Snubber losses	200W	200W
ICT losses (Winding, Core)	120W (80W, 40W)	120W
On-losses in diodes	80W	140W
Recovery losses in diodes	320W	30W
Additionnal losses *	100 to 200W	100 to 200W
Total	1110 to 1210W	880 to 980W
Efficiency	91.5 to 90.85%	93 to 92.5%

* primary connections, stray capacitances

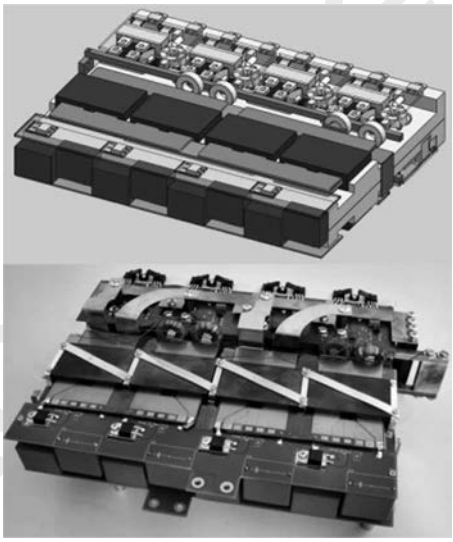

Fig. 13. 3-D design view and real converter.

F. Power Losses Estimation

Estimated losses, deduced from datasheets (semiconductor devices) or from measurements (ICTs) are given in Table II. Two configurations are compared, the first using one high-voltage rectifier diode per cell, and the second using two medium-voltage series-connected diodes (cf., Section IV-C).

This global estimation emphasizes the heavy part of primary losses, consequence of the high current level at the low-voltage side. For example, the snubber losses (diodes and inductor) are significant and cannot be neglected. This drawback should be the same with any switching-aid network.

Additional losses have been approximately estimated to take into account the connections and the effect of stray capacitances [23] resulting in the high transfer ratio of the ICTs.

V. EXPERIMENTAL RESULTS

The results obtained for the 12 kW rated power are shown Fig. 14(a). The waveforms are quite different from the simulated ones, due to the effect of higher stray capacitances of the windings (approximately 50 nF per cell, seen from the primary side) that are resonating with the stray inductances.

This drawback is a consequence of the configuration chosen for the secondary stages: the parallel connection allows getting the maximal benefit from the interleaving on the output capacitor design but needs a high turn ratio.

The waveforms shown in Fig. 14(b) have been obtained with reduced switching frequency (25 kHz) and voltage (14 V), leading to an output power limited to 6 kW, for the output nominal current. This configuration has been chosen for better exhibition of the classical shapes of currents in the ICT topology. In this case, the influence of stray capacitance is lower; therefore, the results are quite similar to those given by the simulations, and clearly show the theoretical $k\,F$ current ripple.

Another topological option can be considered to limit the drawback of high stray capacitances. It consists of a series–parallel association of the secondary stages, as shown Fig. 15. Two groups of four parallelized cells could be series-connected with a reduced turn ratio (1:6). The stray capacitance can be reduced in an 8:1 ratio (2 due to the layer number, 2^2 due to the transfer ratio). Another benefit of this option is the use of

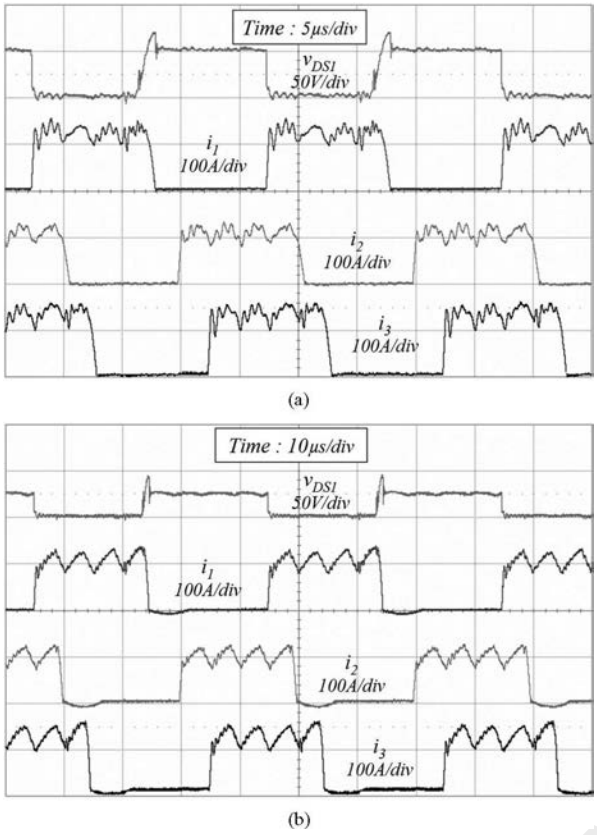

Fig. 14. Experimental waveforms. (a) Experimental waveforms—28 V–50 kHz–12 kW. (b) Experimental waveforms—14 V–25 kHz–6 kW.

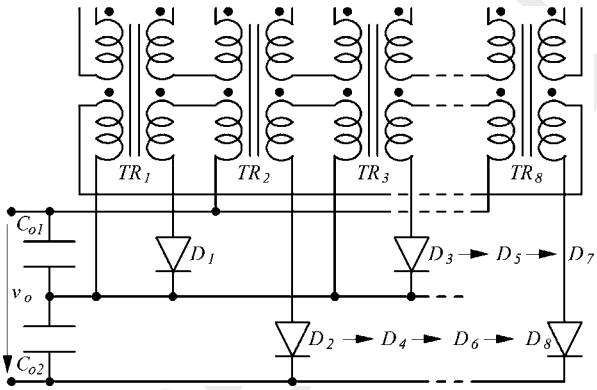

Fig. 15. Configuration with two groups of four cells in series.

600 V diodes without the balancing problem of the previous series connection.

The counterpart is the limitation of the interleaving effect, as the capacitors C_{o1} and C_{o2} are now designed for 4 F and not 8 F as previously. It is not a critical drawback on a 300 V stage.

The measured efficiency (see Fig. 16) is quite lower than the estimated one. An analysis based on the results of parametric measurements (versus input and output voltage, versus input and output current, versus switching frequency) shows that the difference is mainly due to higher losses in the primary connections. It has to be mentioned that each milliohm has a 200 W loss cost for the nominal value of the dc current (450 A).

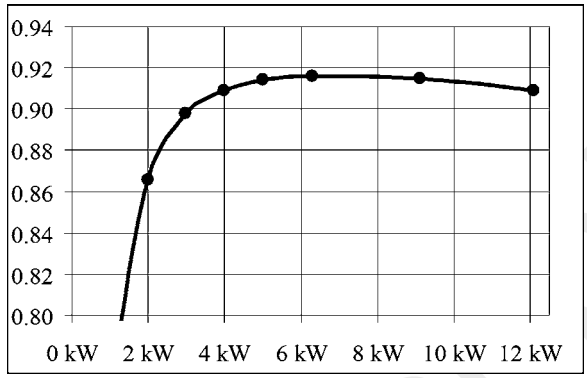

Fig. 16. Efficiency versus output power under 28 V input voltage.

Therefore, the busbar and its connections with the cells have to be significantly improved.

Despite this limitation, which is not attached to this particular topology, these results demonstrate the potential of ICT flyback converter. Estimations give a reachable efficiency close to 93%–94% with the configuration shown in Fig. 15 and the improvement of the low-voltage connections.

VI. Conclusion

The topology and the operating mode of the ICT flyback converter have been first recalled. This structure is an attractive solution for answering to specifications requiring the interleaving of insulated power stages. The ICT flyback converter needs only one magnetic component per cell, and avoids the drawbacks of the single-cell flyback converter. To confirm its interest, the design and the realization of a 28 V–12 kW demonstrator is proposed. The design and the experimental tests of one cell are first made. Then, an advanced packaging of the complete eight-cell converter is defined and realized. The experimental results show the need of some technological improvements, but, above all, show the real viability of the proposed topology. The modular form of the single magnetic stage is one of the most attractive properties of the topology, making of this solution a good candidate to reach high values of power density.

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