Parallel MultiCell Converters for High Current

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Parallel MultiCell Converters for High Current: Design of InterCell Transformers

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***Abstract*- Duality rules show that the multilevel output voltage of series multicell converters transposes in the form of a multilevel input current in parallel converters. However the duality of these families of converter is only partial and parallel converters offer an extra advantage which is multilevel output behavior. When the inductors are coupled together, it is even possible to reduce the ripple of internal quantities, i.e. individual cell currents. The magnetic components at the heart of these converters obey very particular rules and need a specific design procedure. The leakage inductance of this component plays an important part in this design and because it involves flux trajectories in the air it is difficult to predict its value and optimize the design. It is also required to evaluate the core losses, the copper losses and the heat exchange surface to determine which number of cells should be used to minimize total weight. Such a procedure is described and used to compare designs with coupled and uncoupled inductors.**

I. INTRODUCTION

One of the main goals in power electronics is the increase of power density in converters. In recent years, multilevel converters for high power and medium voltage applications (typ. 1-20 MW, 1-10kV$_{dc}$) have been introduced. Obtaining a reliable operation of series connected devices was a first aim, but generating a multilevel voltage waveform across the current source and reducing the filter became the key factor. Applying duality rules to these series multilevel voltage converters, topologies producing a multilevel current waveform through the voltage source are obtained.

As an example, in the series multicell topology of Fig. 1(a) using phase-shifted control signals and a switching frequency of F_s, a four-level voltage waveform at $3.F_s$ can be generated across the current source [1,2], and using the same control signals in the parallel multicell of Fig. 1(b), a four-level current at $3F_s$ is taken from the voltage source [3]. The corresponding waveforms are given for a duty cycle ramping from 0 to 95%.

However, an even better solution for paralleling commutation cells is obtained with star-connected inductors flowing equal currents (Fig. 2). The most obvious advantage of this topology is that it generates four-level waveforms at $3F_s$ on both sides.

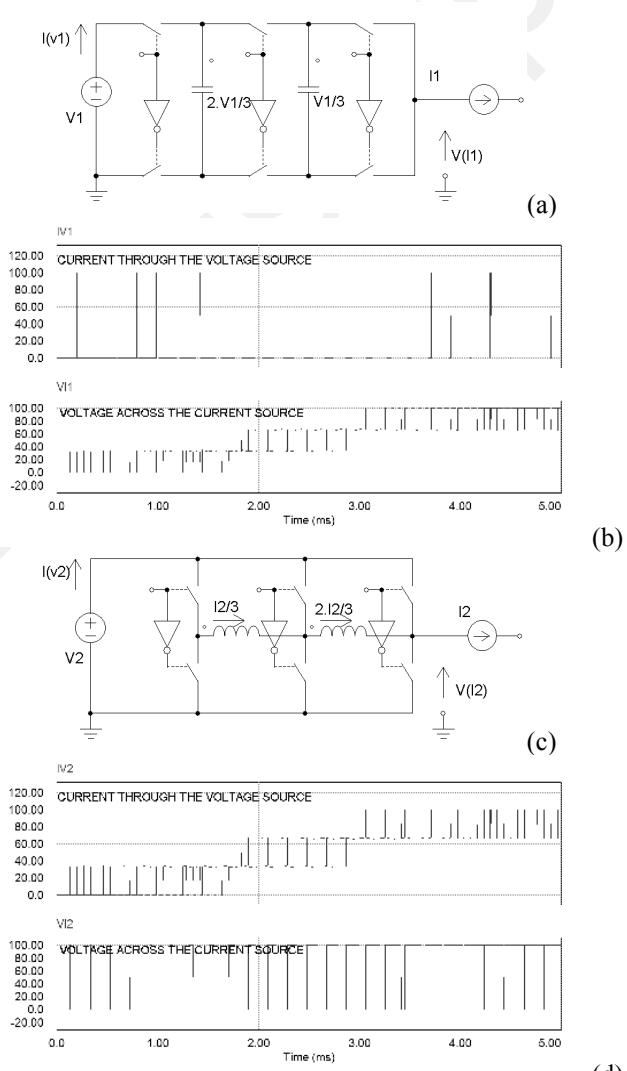


Fig. 1. Two dual multilevel topologies and corresponding waveforms (V_{in}=100V, I_{out}=100A, F_s=5kHz).
Series multicell: (a) topology, (b) input and output waveforms.
Parallel multicell: (c) topology, (d) input and output waveforms.

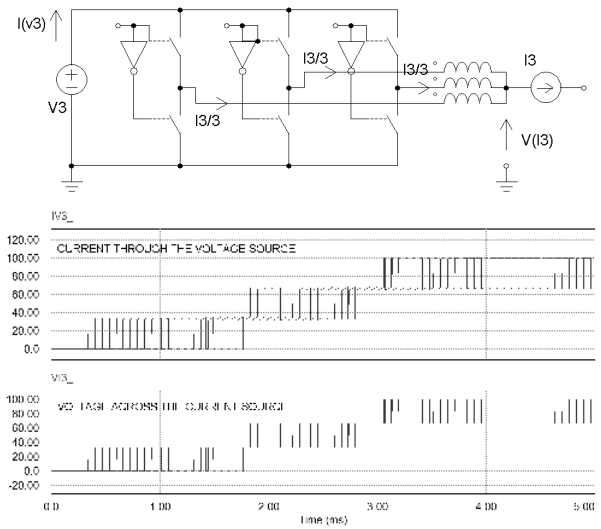


Fig. 2. Parallel multicell converter and corresponding input and output waveforms (V_{in}=100V, I_{out}=100A, F_s=5kHz)

The second advantage is that the energy stored in the star-connected inductors directly contributes to the filtering of the output current. To evaluate this topology in terms of tradeoff between the energy stored in passive components and the quality of the current and voltage waveforms, we give in Fig. 3 and 4 the waveforms obtained with series and parallel three-cell converters equipped with the same input filter, the same energy stored in the output inductors (50µH\100A for the series multicell, 3 times 150µH\33.3A for the parallel multicell), and the same energy in the output capacitor. In this comparison, the energy stored in the flying capacitors appears as an extra price to pay for. As can be seen from the waveforms, the output current ripple is exactly the same in both converters, but the multilevel operation at the input side of the parallel multicell gives a significant reduction of the current ripple.

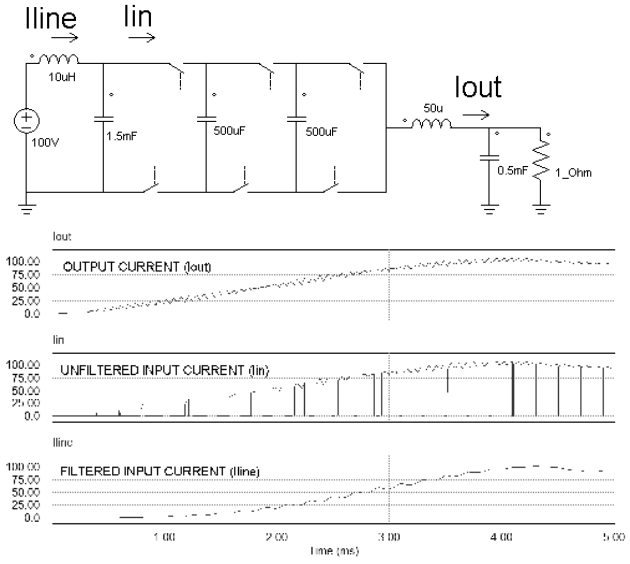


Fig. 3. Series multicell converter and filter waveforms (V_{in}=100V, I_{out}=100A, F_s=5kHz, L_{in}=10uH, C_{in}=1.5mF, L_{out}=50uH, C_{out}=0.5mF)

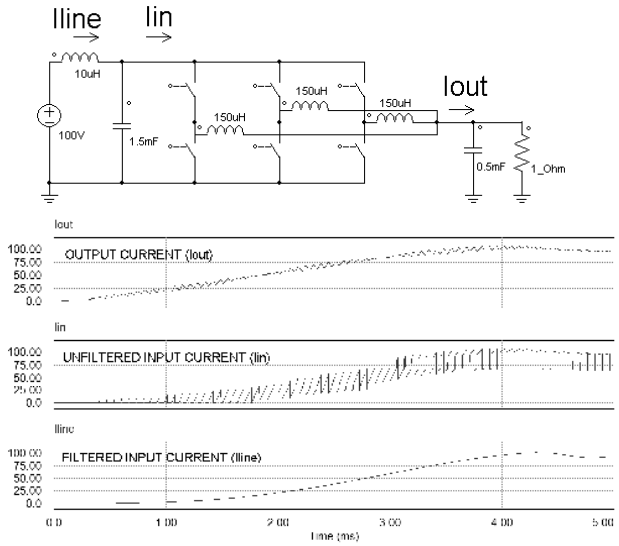


Fig. 4. Parallel multicell converter and filter waveforms (V_{in}=100V, I_{out}=100A, F_s=5kHz, L_{in}=10uH, C_{in}=1.5mF, L_{outeq}=150uH/3=50uH, C_{out}=0.5mF)

In recent years, the interest for parallel multicell converters has grown, and this is also due to the possibility to couple the inductors [4,5,6,7]. Coupling the inductors to form an InterCell Transformer (ICT) does not modify the output current, but it reduces the current ripple in the windings and the flux swing in some region of the core. It can be shown [8] that this brings a reduction of copper losses and iron losses in the ICT. The reduction of the phase current ripple also reduces the difference between turn on and turn off current in the switches, which brings a reduction of switching losses for devices generating more losses at turn-off than at turn-on.

This topology is not new and several variants have been proposed [9], but we think their potential has been underestimated especially as far as cyclic cascade and monolithic ICTs are concerned. The knowledge gained by studying series multicell converters can be transposed to these converters by applying duality rules: for example the natural balance mechanism described in [10] applies to this converter as well, the relevant parameters being dual from each other. In the series multicell converter a faster natural balance is obtained by lowering the impedance of the current source at the switching frequency, while it is obtained by increasing the impedance of the voltage source at the switching frequency in the parallel multicell converter. However, the design of the ICTs at the heart of these attractive converters is a blocker; duality does not help designing them because magnetic coupling has no dual and transformer and inductor design rules do not apply either. The design of these components is very specific and inherent features must be taken into account: flux is mainly AC while currents are mainly DC, leakage inductance is a key parameter because the current waveforms depend strongly on its value, etc. Taking full benefit of the potential advantages of ICTs requires the development of special tools and methods, and it is not straightforward to compare them with conventional filtering inductors, which is the aim of this paper.

II. DESIGN OF A TWO-PHASE ICT

A two-phase ICT is to be used in applications where only two commutation cells are available. The typical diagram is shown in Fig. 5, where a basic DC chopper is used as an example of interleaved converter. In this case, the leakage inductance of the ICT must be high enough to keep the current ripple at a level determined by the designer.

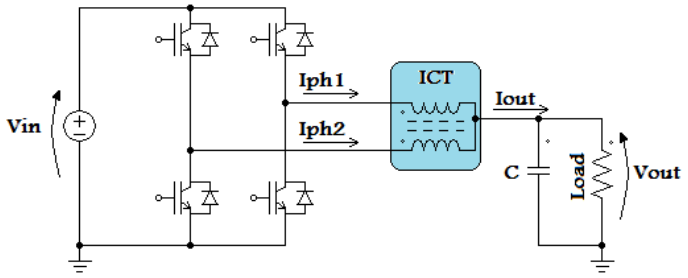


Fig. 5. Two-phase intercell transformer used in an interleaved converter

Since the ICT has only two windings, a variety of core shapes may be used and some of them are shown in Fig. 6. The choice of the core shape depends basically on the availability of the material, size and price. It strongly influences the design process since shapes in Fig. 6(a) and (b) typically result in ICTs with higher leakage inductance values than those in Fig. 6(c) and (d). This is due to the fact that the leakage energy is mainly concentrated in the region between the windings in Fig. 6(c) and (d) while it is spread out in the space around the ICTs of Fig. 6(a) and (b).

The ICT in Fig. 6(d) is not actually considered in the design of a two-phase ICT as its windings are not symmetrical. The outer winding is longer than the inner one, which may cause current unbalance in the final converter. This is not a particular problem for N-phase ICTs in cyclic cascade topology since 2 two-phase ICTs are used in each phase. Thus for each phase we may connect the shorter winding of the first ICT in series with the longer winding of the second ICT, which makes the circuit symmetric.

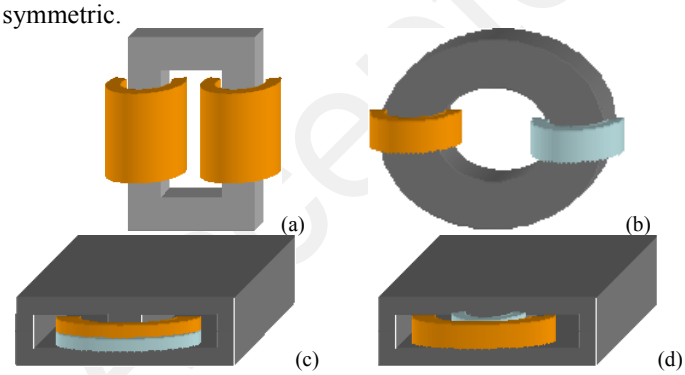


Fig. 6. Two-phase ICTs using different core shapes
(a) UI core. (b) Tore
(c) EE core, stacked windings. (d) EE core, concentric windings

Independently of the core shape, the equivalent magnetic circuit may be represented by Fig. 7 if the core has high permeability and no air gap. Air gap is not usually designed in ICTs because it induces high magnetizing currents, which increases the output current ripple. It may also increase copper losses by means of high frequency currents induced in the conductors of the winding that are close to the air gap. The main advantage of proposing an air gap is to increase robustness against core saturation resulting of current unbalance in the phase currents.

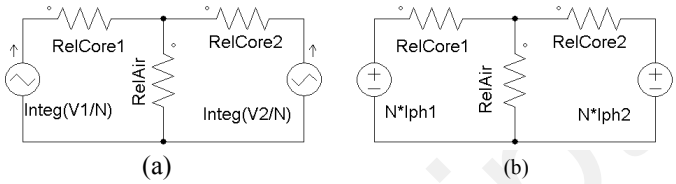


Fig. 7. Simplified model of the ICT magnetic circuit
(a) Equivalent AC model. (b) Equivalent DC model

Reluctance *RelAir* represents the whole leakage energy stored in the air between the windings and outside the ICT. The flux sources (ϕ_1 and ϕ_2) carry a triangular flux which is a result of the voltage applied across each winding. Taking Fig. 5 as an example, we can see that because the output voltage (V_{out}) is practically continuous, we have rectangular voltage waveforms across the windings and the fluxes ϕ_1 and ϕ_2 are both triangular (but phase-shifted of 180° as imposed by the 180° phase-shift of the control signals of the two cells). These fluxes add up through reluctance *RelAir*. If *RelCore1* and *RelCore2* are neglected, the difference of magnetic potential across *RelAir* is imposed across both windings which imposes AC currents I_{ph1} and I_{ph2} to have the same amplitude, same phase and a fundamental frequency equal to twice the switching frequency.

DC flux also exists, but it obeys quite different rules. In normal conditions the DC components of I_{ph1} and I_{ph2} are equal, $RelCore_1$ and $RelCore_2$ can be neglected and the MMF $N.I_{ph1}^{dc}$ (resp. $N.I_{ph2}^{dc}$) generates a flux $N.I_{ph1}^{dc}/2/RelAir$ through winding 1 (resp. winding 2). In case of current unbalance though, $RelCore_1$ and $RelCore_2$, must not be neglected; they are the only factors limiting the DC flux component looping through both windings and this flux is equal to:

$$\Phi_{dc}^{asym}=N.(I_{ph1}^{dc}-I_{ph2}^{dc})/(RelCore_1+RelCore_2) \quad (1)$$

A. ICT Design

Having all these concepts in mind, the magnetic design may be initiated. The goal is to meet the specifications without saturating the core.

Depending on the geometrical parameters of the transformer, the leakage inductance L_{leak} can be either calculated or/and simulated. Reference [11] shows how it can be done for the example given in Fig. 6(a). The fraction of the leakage inductance due to the part of the winding that is inside the core can be analytically calculated as [12]:

$$L_{leak} = l_{av} \cdot \mu_0 \cdot \frac{N^2}{h} \cdot \left[b_2 + \left(\frac{2 \cdot b_1}{3} \right) \right] \quad (2)$$

where b_1 is the winding width, b_2 is the width of the air between windings, h is the core height, l_{av} is the mean length of the conductor inside the core (usually equal to the core depth) and μ_0 is the air permeability. Alternatively, the fraction of the leakage inductance due to the part of the winding outside the core may be estimated using simplified 2D geometry.

Using this leakage inductance, the maximum current ripple in each phase, DC and peak-to-peak AC fluxes are calculated as shown in equations below:

$$I_{ripple\max} = V_{in} / \left(4F_s.N_c.L_{leaktot}\right) \quad (3)$$

$$B_{dc} = N.I_{out}{}^{dc} / \left(2.N_c.A_c.\left(N^2/L_{leak}\right)\right) \quad (4)$$

$$B_{ac\max} = V_{in} / \left(4N.F_s.A_c\right) \quad (5)$$

where N_c is the number of cells (in this case equal to 2), F_s is the switching frequency and A_c is the core section. The total leakage inductace $L_{leaktot}$ is equal to L_{leak} since, in this case, there is only one transformer.

Since the converter has only two phases, usually leakage inductance must be high in order to attain current ripple specifications. We can see by (4) that a high leakage inductance creates a high DC flux. As a consequence, it is better to use core materials with a high magnetic field saturation to reduce the volume and weight of the ICT.

Core losses are calculated by using the most classical model for ferrite materials, which is the simplified Steinmetz Model adjusted according to the temperature [13, 14]. Its analytical form is shown in (6), where C_T is the temperature adjustment and K_{mat}, α and β are parameters related to the specific core material and frequency range of switching frequency.

$$P_{core} = C_T \cdot K_{mat} \cdot F_s^{\alpha} \cdot B_{ac\max}^{\beta} \quad (6)$$

For the two-phase ICT, note that AC flux inside the material has a triangular waveform at the switching frequency and its maximum value occurs when the duty cycle is equal to 0.5.

The current distribution in the conductors of the winding is clearly different inside and outside the core, which can be simulated using a Finite Element (FE) software. As an example, we show in Fig. 8 the current density distribution corresponding to the cross section of an ICT. Because of this uneven and asymmetrical current distribution, equivalent AC resistances inside and outside the core are different as well. In [15], it is shown how these resistances can be simulated and calculated for the example given in Fig. 6(a).

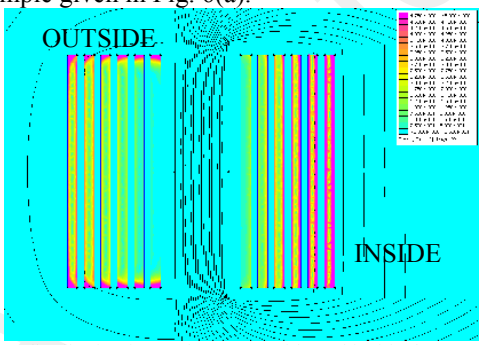


Fig. 8. Current distribution in conductors outside and inside the core of an ICT

It should be noted that not all AC resistances can be calculated using DOWELL's equations [16] because the 1D assumption is irrelevant and FE analysis is required at a certain stage. Each harmonic has its correspondent AC resistance so that the current must then be decomposed in its Fourier series to calculate the contribution of each harmonic to the copper losses inside and outside the core, and finally added up to obtain the total copper losses according to the following equation:

$$P_{copper} = R_{dc}.I_{dc}{}^2 + \sum_{m=1}^{\infty}\left(Rac_m^{in} + Rac_m^{out}\right)I_m{}^2 \quad (7)$$

where $Rac^{in}{}_m$ and $Rac^{out}{}_m$ are, respectively, the AC resistances of the conductors of the winding inside and outside the core at the frequency corresponding to the mth harmonic and I_m is the mth harmonic of the current passing through the windings.

After calculating both copper and core losses, ICT temperature may be estimated. For the moment, a simple model considering a unique temperature for the whole ICT is used. The total heat exchange area (S_{exc}) of the ICT is calculated considering all copper and core surfaces which are in direct contact with the air. A heat exchange coefficient (H_{exc}) based on industrial experience is finally used to calculate the overall ICT temperature rise (ΔT), using the equation below:

$$\Delta T = P_t / \left(S_{exc}.H_{exc}\right) \quad (8)$$

where P_t is the total losses of the ICT.

III. Design and Optimization of N-phase ICTs

There are several topologies of ICT with more than two phases. They are generally divided into two different types: monolithic or separate transformers. Separate ICTs are composed of several two-winding transformers, each of them being connected to a different pair of phases. The number of separate transformers which must be used in an N-phase interleaved converter depends on the topology adopted [9]. If the ICT is monolithic, there are several different topologies to analyze. Some of them are shown in Fig. 9.

The design of monolithic ICTs (such as those in Fig. 9(a) and (d)) and the design of each separate transformer may also be made using the method presented in Section II, noting the following differences:

- the total leakage inductance $L_{leaktot}$ is the sum of the leakage inductance of each separate inductor,
- the flux circulating in the cores is not triangular; it has a complex waveform as explained in [17].

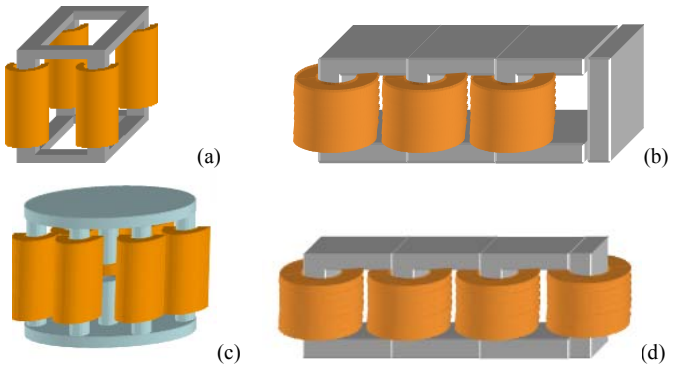


Fig. 9. Different topologies of monolithic intercell transformer
(a) Symmetrical cubic core. (b) Ladder with guided leakage flux.
(c) Symmetric core with central leg. (d) Ladder with distributed leakage flux.

It should be noted that when the number of cells increases a smaller leakage inductance is needed which means smaller DC

flux. Thus, core materials having low saturation flux density (such as ferrite) are adequate for the design of ICTs with a high number of phases. On the other hand, a two-phase ICT may need a core material with a higher saturation flux density.

IV. Design Optimization and Comparison

A. *Design optimization*

In Section II we showed the equations and how to proceed in order to design a two-phase ICT. However, the best ICT for a particular application is the one which is optimized regarding one specific objective related to the application. It is usually the ICT price, volume, weight, losses or a combination of these criteria.

Since there are several parameters which may influence the ICT design at the same time, an optimization algorithm is necessary.

The optimization algorithm we developed has many input variables: geometrical parameters of the conductors and core, number of turns and switching frequency. Also, the possible objectives are the ones mentioned above. Several constraints may be considered such as: maximum current ripple, temperature rise, losses etc.

In this algorithm, the user can choose the conductor and core materials as well as electrical and thermal characteristics of the ICT.

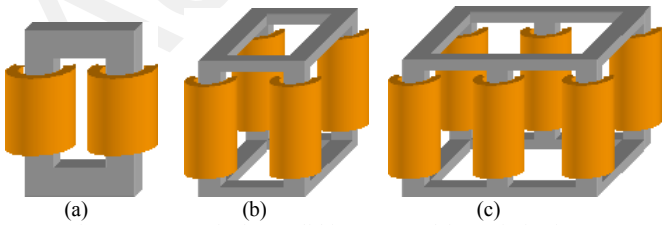
B. *Comparison between N-phase ICTs and separate inductors*

To illustrate the use of the optimization algorithm and the difference of designs for ICTs with a different number of phases, a comparison between 3 ICTs and separate inductors will be presented. The ICTs are all monolithic and symmetrical, and have 2, 4 and 6 cells. Their structures are shown in Fig. 10.

The separate inductors have the structure presented in Fig. 11 and they were also optimized for interleaved converters with 1, 2, 4 and 6 cells. Note that they have 2 windings which are connected in series and the air gap is distributed in 4 different places.

As an example, ICTs and separate inductors are specified to be used in a 100kW DC/DC converter. Design is made for the worst case for each topology, which means that the duty cycle is different from each case.

The objective is to design the ICT and separate inductors with the lowest weight. Specifications of the design are shown in Table I. Note that the maximum output current ripple is not specified since the output voltage ripple specification can be achieved by using an adequate output capacitor, which is usually much smaller than the ICTs and inductors.



(a) (b) (c)

Fig. 10. Symmetrical monolithic ICTs used for optimization
(a) 2-phase ICT. (b) 4-phase ICT. (c) 6-phase ICT

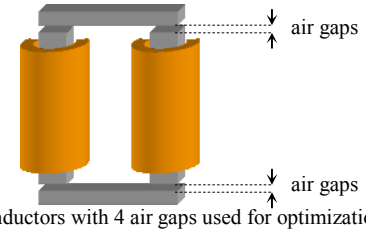


Fig. 11. Separate inductors with 4 air gaps used for optimization

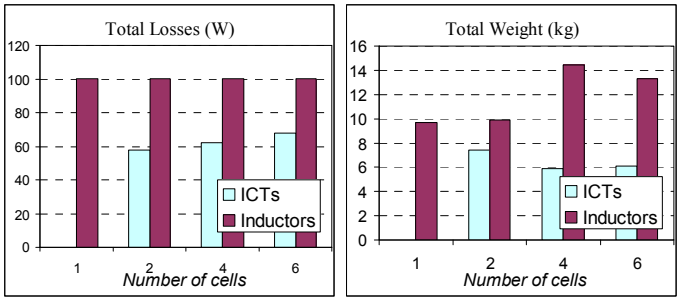
Full results of the ICT optimizations are shown in Table II, those related to separate inductors are shown in Table III, and main results are compared in Fig. 11. Note that, globally, ICTs are much lighter and smaller than separate inductors. For the case of 4 phases, for example, 4 separate inductors result in a magnetic component 144% heavier than a 4-phase ICT. Also, ICTs have fewer losses than separate inductors, which is compatible with the fact that they are smaller.

TABLE I
Specifications for the ICT Design

Parameter	Symbol	Value
Insulation thickness (mm)	e_{ins}	0.2
Input voltage (V)	V_{in}	200
Output current (A)	I_{out}	500
Switching frequency (kHz)	F_s	20
Calculation temperature (°C)	T_c	100
Core material		Ferrite 3C90
Conductor material		copper
Thermal exchange coefficient (W/m²/°C)	H_{exc}	15
Max induction in core (T)	B_{max}	0.25
Max total losses (W)	P_{max}	100
Max RMS current density (A/mm²)	J_{max}	5
Max temperature rise (°C)	ΔT_{max}	30

Given that the switching frequency is the same for all cases, the apparent frequency of the output current is higher for the converters with higher number of phases and also the output current ripple is smaller. As a consequence, smaller filter capacitors are necessary in these cases.

The ICTs and inductors presented here have a high height/width ratio. This is because these components need a high conductor section to allow high DC currents with ripple at a high frequency (>20kHz). As a result, the conductors must be high and thin. Such windings can be made using a copper foil.



(a) (b)

Fig. 11. Performance of ICTs and inductors compared
(a) Total losses. (b) Weight.

TABLE II
COMPARISON OF ICT OPTIMIZATION RESULTS

Parameter	2 phases	4 phases	6 phases
Conductor weight (kg)	1.38	2.17	2.32
Core weight (kg)	6.08	3.75	3.79
Total weight (kg)	7.46	5.92	6.11
DC conductor losses (W)	13.13	9.63	7.09
AC conductor losses (W)	8.65	0.47	0.19
Core losses (W)	14.17	21.53	24.45
Total losses (W)	57.72	61.94	68.13
Temperature rise (°C)	29.78	30	30
Output current ripple (A)	638.70	122.84	62.82
Core width (every 2 windings)(mm)	53.55	66.82	64.48
Core height (mm)	213.62	229.39	170.45
Core depth (mm)	114.29	20.98	20.08
Core leg width (mm)	24.36	27.55	25.72

TABLE III
COMPARISON OF SEPARATE INDUCTORS OPTIMIZATION RESULTS

Parameter	1 phase	2 phases	4 phases	6 phases
Conductor weight (kg)	3.44	3.41	5.95	4.05
Core weight (kg)	6.26	6.48	8.49	9.24
Total weight (kg)	9.70	9.89	14.44	13.29
DC conductor losses (W)	55.86	53.73	52.16	53.90
AC conductor losses (W)	19.60	20.74	15.58	18.90
Core losses (W)	24.54	25.53	32.25	27.20
Total losses (W)	100	100	100	100
Temperature rise (°C)	30.00	29.56	16.98	21.84
Output current ripple (A)	660.21	331.22	162.08	93.14
Core width (mm)	94.72	61.12	56.88	57.00
Core height (mm)	693.32	350.70	326.84	143.40
Core depth (mm)	31.89	35.98	28.62	43.74
Core leg width (mm)	27.94	26.04	22.56	23.65

V. CONCLUSION

Multicell converters allow fractioning the power to be handled and the use of semiconductors with smaller ratings. They deliver multilevel waveforms at higher frequencies and help reducing the size of the filters, and to this extent, using high number of cells seems promising.

However, it is well known that increasing the number of cells in series multicell converters requires a high amount of energy stored in capacitors and 3-cell is generally considered a maximum. Parallel multicell converters with star-connected inductors or with intercell transformers do not suffer from the increase of stored energy with increasing number of cells. They seem a priori better adapted to the high number of cells.

However, the amount of stored energy is not the best measure of the weight of passive components, and a more accurate design of passive components including loss and thermal estimation is needed to determine the evolution of the weight of passive components vs number of cells. The example described in this paper shows that the total weight of inductors tends to increase with the number of cells when uncoupled inductors are used (minimal weight for 1 or 2 cells), while the weight of ICTs is minimized for 4- or 6-cell configurations. It is also found that the lightest ICT is 40% lighter than the lightest inductor, and that the 4-cell ICT-based design requires an output capacitor that is roughly 20 times smaller than with a 1-cell design.

As a conclusion, parallel multicell converters with InterCell Transformers seem to be a good choice when a high power density is desired and offers interesting perspectives for isolated converters [18].

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