A High Voltage Programmable Input Interface for Avionic Equipment

Antoine Canu, Philippe Benabes, David Faura, Patrice Toillon, Marc Gatti

A High Voltage Programmable Input Interface for Avionic Equipment

Antoine Canu, Philippe Bénabès
Signals and Electronic Systems Department
Supélec
Gif-sur-Yvette, France
{antoine.canu, philippe.benabes}@supelec.fr

David Faura, Patrice Toillon, Marc Gatti
Computer Competence Center
Thales Avionics
Meudon-la-Forêt, France
{antoine.canu, david.faura, patrice.toillon, marc-j.gatti}@fr.thalesgroup.com}

***Abstract*—Avionic computers are required to sense their environment or interact with other devices through the use of various sensors or communication buses. Currently, these sensors and buses use dedicated interfaces, which limits the functionalities that can be implemented in the computer. In this paper, we propose a programmable interface meant to interface most common sensors found in avionics, which could facilitate the designand reuse of avionic computers. The architecture of the interface is presented, with a focus on the programmable analog signal conditioning stage which is able to withstand the high voltages present in the harsh avionic environment.**

Keywords; avionics,harsh environment, high-voltage techniques,reconfigurable architectures.

I. INTRODUCTION

For the last forty years, safety and performance requirements for avionic equipment have constantly increased. To answer to these new requirements, avionics have known important changes. Federated Architectures, in which one computer performs only one specific function (e.g. fuel management or brake monitoring), have been replaced by Integrated Modular Avionics (IMA)[1], in which a single computer is able to embed and process several functions. Each of these functions needs to acquire data from a specific set of sensors. For example, a fuel management function will need to acquire temperatures or pressures, whereas a flight command function will require flaps position or angle to be acquired. All these different sensors have their own output signal characteristics, and currently, each sensor is interfaced by a dedicated interfacing circuit, embedded within the computer (see Fig. 1). This means that the functions which can be implemented in a computer directly depend on which interfaces it embeds.

We propose to remove this hardware limitation thanks to a reconfigurable acquisition system, called versatile input interface (see Fig.1), dedicated to the most common sensors found in avionics.Most of these sensors feature high voltage ranges. Furthermore, sensor interfaces have to be able to withstand the superimposition of high voltage common-mode noise to the signals provided by the sensors, which increases the difficulty of designing a programmable interface with conventional techniques.

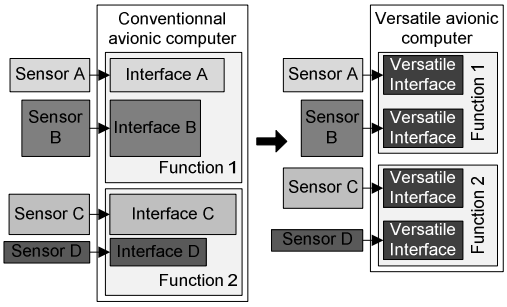

Figure 1. Comparison between computers using conventional interfaces and versatile interfaces

The output characteristics of these sensors are detailed in section II, while section III exposes some state of the art techniques used for programmable interfaces. Section IV exposes proposed architecture for the avionic reconfigurable interface, and section V focuses on itshigh voltage programmable analog front end (AFE).

II. CHARACTERISTICS OF AVIONIC SENSORS AND INPUTS INTERFACES

Discrete Ground/Open, Discrete Vdd/Open, ARINC429 [2], DC analog acquisitions and Variable Differential Transformers (VDT) acquisitions represent up to 80% of the total input interfaces embedded in IMA computers. TABLE 1 lists the main characteristics of these input interfaces. Globally, it is worth noticing that all these signals occupy a very low bandwidth, typically less than 1 MHz, but feature rather high voltage ranges: from -22V to +50V. Thus, the difficulty of designing a versatile interface for these signals comes from their high voltage range and from the high amplitude common mode noises which can be superimposed to the useful signal. The signal processing to apply are very various, and can be really simple, such as a simple comparison for discrete sensors, as well as more complex, such as the demodulation algorithm for VDT sensors.More details about these input interfaces and their characteristics can be found in [3].

TABLE 1. CHARACTERISTICS OF THE FIVE MOST PRESENT INPUTS IN AVIONICS

Sensor/ Interface name	Signal type	Common mode voltage range	Differential Voltage range	Input Impedance Required	Bandwidth	Precision required	Processes to apply
Discrete GND/OPEN	Single Ended	[-22V; +22V]	N/A	30k□	[0; 200Hz]	Low (1%)	Low pass filter. Hysteresis comparison.
Discrete VDD/OPEN	Single Ended	[0V; +50V]	N/A	30k□	[0;200Hz]	Low (1%)	Low pass filter. Hysteresis comparison.
A429	Differential	[-30V; +30V]	[-13V; +13V]	>8k□	[0; 750kHz]	Low (1%)	Hysteresis comparison .Timing control. Frame retrieval. Frame integrity control.
DC Analog Acquisition	Differential	[-30V; +30V]	[-10V; +10V]	>100k□	[0; 200Hz]	Medium (0.1%)	Low pass filter.Data extraction.
VDT Acquisition	Differential	[-30V; +30V]	[-10V; +10V]	>100k□	[0; 10kHz]	High (0.05%)	Demodulation algorithm (e.g. [4][5])

III. STATE OF THE ART OF PROGRAMMABLE INTERFACES

Signal acquisition usually requires analog as well as digital processing. Therefore, most of the times, developing a truly reconfigurable signal acquisition system requires to have programmable analog and programmable digital capabilities.

Programmable digital electronics is not really a challenge anymore, thanks to the development of PLD's and PGA's technologies. The programmable capability of these devices has already been used for reconfigurable interfaces. For example, Aibe and Yasunaga[6] have proposed a reconfigurable interface called Meta-I/O, meant to standardize various digital I/Os, such as PS/2 or I²C bus. Nevertheless, the Meta I/O does not embed any AFE and thus is not intended for analog or high voltage signal acquisition, and therefore could not be used for most common avionic inputs.

On the other hand, programmable analog electronics has been much more of a challenge. The field of programmable analog electronics provides several solutions which seem at a first glance perfectly adapted to the design of a generic, reconfigurable interface. FPAAs for instance allow the reconfiguration of analog cells for rapid prototyping. Emerging in the late 90's, these FPGA analog equivalents have been faced with numerous issues, including a low interconnectivity and thus weak possibilities [7] and their future is now uncertain [8].The main target of these programmable circuits is essentially programmable filtering [9], but under low voltage conditions only, making them incompatible with the avionic requirements.

Nowadays, programmable analog electronics can essentially be found in the Actel Fusion® and Smart-Fusion® [10] mixed signal FPGA, which propose interesting features for voltage and current monitoring, but are still insufficient for our application , again because of their low integration and low voltage range.

Finally, some work has been done in the field of intelligent or generic analog interfaces. For example, Souza [11] has proposed a custom design for a programmable interface dedicated to low voltage biomedical sensors. This work has been followed by Catundaet. al. [12], who proposed an improvement by using the programmability of the circuit to calibrate the analog front end of their circuit. This calibration can compensate the imperfect matching of analog components, which is responsible of imprecisions in most analog measurement applications. This interface has the same purpose as our programmable avionic interface, and shares some of our limitations –imprecisions in measurement due to analog matching for example–; however, the avionic interface is faced with the challenge of measuring high potentials.

All these different works or commercial solutions are incompatible with the high voltages present in avionics, which is why we decided to develop our own high-voltage programmable interface.

IV. VERSATILE INPUT INTERFACE ARCHITECTURE

Every conventional avionic interface contains the same functional blocks: a signal is fed to the interface through a one or two pins connector (depending on the signal type: single-ended or differential). A Transient Voltage Suppressor (TVS) or equivalent device is used for lightning protection. Then, an analog front end formats the signal thanks to gain and dc level shifting and an analog to digital conversion is done. Depending on the sensor, this conversion can be a high resolution conversion as well as a simple one bit comparison. Raw digital data is then processed in order to retrieve the original and useful data.

The versatile input interface is built on the same skeleton (see Fig. 2), but contrary to a conventional interface where every function is fixed, the versatile interface has the capability to change some of its characteristics. These parameters constitute what we have called programmable resources. These resources can be analog as well as digital. By changing these resources, the versatile input interface can adapt for example its input voltage range, the cutoff frequency of filters or the type of digital processing applied to the data. Ultimately, this enables to interface various types of inputs, sensors or buses.

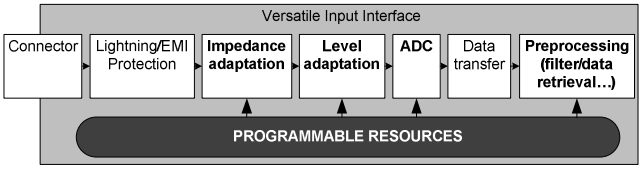

Figure 2. Functional description of the versatile input interface

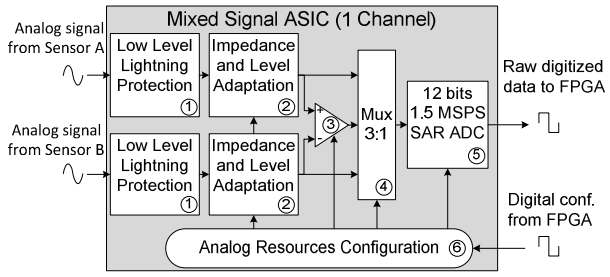

Figure 3a) Architecture of the Mixed-Signal ASIC.

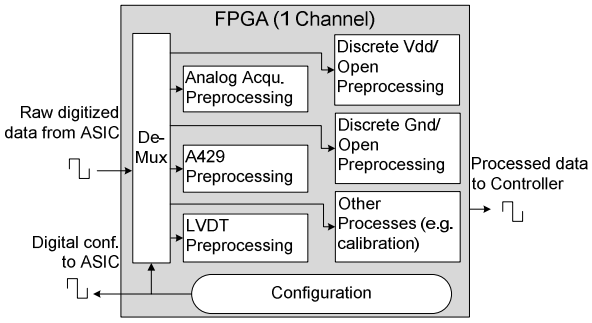

Figure 3b) Architecture of the FPGA

The architecture is based on two electronic chips: one mixed signal ASIC, and one programmable digital chip, such as a FPGA. They both contain some of the programable resources previously described.

A. Mixed Signal ASIC

The mixed signal ASIC contains the analog programmable resources which are essentially dedicated to the formatting of the analog signals for a further analog to digital conversion. The ASIC embeds the AFE of the interface, and as a consequence, is directly exposed to the raw signals provided by the different sensors present in the aircraft. The high voltages present in avionics (see TABLE 1) have led us to consider only High VoltageASIC technologies such as [13] or [14].

The ASIC contains several differential channels which can also be independently programmed as two single-ended subchannels, for discrete interfacing.Each channel of the ASIC is composed of the following subfunctions (see Fig. 3a):

1) An integrated low level lightning protection protects the ASIC against low level induced transients, up to DO160F first level [15]. This protection also acts as an EMI filter.

2) A programmable impedance and level adaptation stage reduces and offsets the high voltage input voltage so that it matches the more conventional [0V; 3.3V] range used by the low voltage core of the ASIC. This stage is detailed further in section V.

3) For differential signals, a conventional programmable differential stage similar to the one used in[12] rejects common mode and outputs the useful signal on the range ADC input range thanks to a programmable amplification gain.

4) A 3:1 multiplexing stage directs the differential output or one of the two single ended outputs towards the ADC.

5) A 1.5MSPS, 12 bits successive approximation register ADC is in charge for analog to digital conversion.

6) A configuration stage communicates with the FPGA during the configuration process, and commands the various parameters of the ASIC, i.e. impedances, gains, offsets, multiplexor channels or ADC speed.

B. FPGA

A FPGA, shared byseveral channels, is responsible for signal processing, data extraction and ASIC configuration (see Fig.3b). It contains the digital programmable resources, i.e. the different digital treatments adapted to every kind of inputs, and processes the raw data provided by the ADC within the ASIC. The parameters of these processes (filters parameters, comparison thresholds) can be changed to fit the specifications of the aircrafts manufacturers, making the interface scalable.

V. PROGRAMMABLE IMPEDANCE AND LEVEL ADAPTATION STAGE

The purpose of the programmable and level adaptation stage is to ensure that for any sensor from TABLE 1, the interface has the required input impedance, and the correct gain and offset to reduce the sensors output voltages to the [0V; 3.3V] input range of the ADC. Catunda[16] showed that using a programmable conditioning circuit usually leads to either a loss of measurement range or a loss of resolution, because of the inherent discrete nature of digital programming. Considering the relatively low precision required for our avionic signals, we decided to ensure the full measurement range even if this reduces the total resolution of the system. Catundaalso details how this can be done by under-dimensioning the gain and the offset of the acquisition chain.

As Fig.3a suggests, before the common-mode rejection stage of the ASIC, differential signals are treated as two single-ended signals. From the dynamic of these single ended signals, we can deduce the required gains and offsets to ensure full measurement range, and notice that because of their relatively close dynamic, they can be grouped in only three categories, each of them needing a specific gain, offset and impedance.

TABLE 2. REQUIRED AFE PARAMETERS FOR THE VARIOUS SENSORS

Name	Voltage range per line	Required Gain	Required Offset	Required Impedance
Discrete GND/OPEN	[-22V; +22V]	□0.075	1.65V	30k□
Discrete 28V/OPEN	[0; +50V]	□0.066	0V	30k□
A429/ DC/ VDT	[-36.5V; 36.5V]	□0.045	1.65V	>100k□

To achieve these different gains, offsets and impedances, it is possible to use switched resistors. This method is often used for exampleto program gains in differential amplifiers [12] or in digital potentiometers.Usually, these applications use

conventional analog switches [17], built from a NMOS and a PMOS transistor connected in parallel(see Fig.4).These analog switches cannot operate with voltages which exceed their own power supplies[17], which make them unusable for our application. Various analog switches manufacturers have proposed different methods for fault protection, such as series-connected MOSFETs [18] or addition of diodes on power supplies [17].

Figure 4. Conventional switch (left) and in-series switch (right) [18]

These methods allow the switches to be protected in case of overvoltage condition, but don't ensure their normal operation. Nevertheless, we propose to use the series-connected method in a novel yet simple way to design a high voltage programmable AFE.

The in-series connection of two MOSFETs (see Fig.4)is usually neither recommended nor acceptable for conventional analog switching applications (e.g. analog multiplexing) because of the poor performances of such switches in the closed state. Indeed, their R_{on} resistance is four times higher than that of a switch using parallel connected MOSFETs, which is not suitable in most switching applications. Furthermore, the closed state of a series-connected switch is ensured on a shorter input voltage range, typically$\pm(Vg-V_{th})$, where V_{th} is the threshold voltage of the MOSFETs used in the switch. However, the in-series switch is able to remain opened (high impedance) even when over-range voltages are applied to its terminals, whereas in this condition the impedance of a parallel-connected switch drops because of the forward biasing of the substrate junctions[18].Consequently, it is possible to take advantage of the excellent behavior of the series-connected switch in the open state, as long as we can ensure that an overvoltage condition will never occur in the closed state.

The proposed AFE is based on the switching of two voltage dividers(see Fig.5) by three in-series-connected switches S_1, S_2 and S_3.

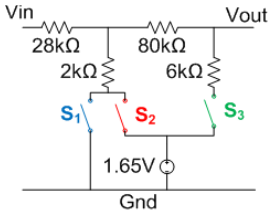

Figure 5. Proposed High Voltage AFE using in-series connected MOSFETs as switches

By connecting one terminal of the switches to either ground or to the low voltage 1.65V source used for DC level shifting, we ensure that in the closed state, there will always be a low voltage (less than 3.3V) on any of their terminals, which fits the recommendations stated before. As seen in Fig.6b, by switching on S_1, S_2 or S_3, respectively for discrete 28V/Open, discrete Gnd/Open, or DC Acquisition, the AFE effectively reduces the corresponding sensors output ranges to the [0; 3.3V] ADC input span. Fig. 6a shows that in the DC Acquisition operation, the same circuit using conventional switches is no longer able to effectively reduce the input voltages, because S_1 and S_2 are faced with overvoltage conditions.

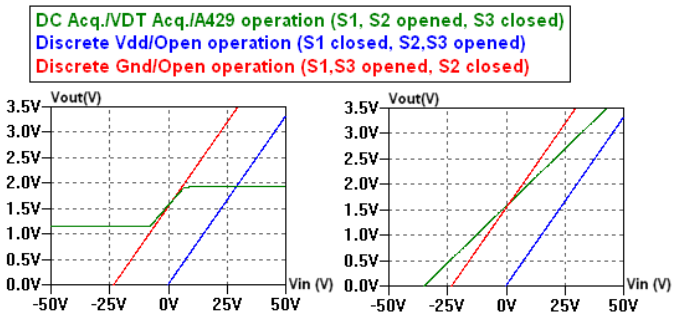

Figure 6a)(left) Transfer function of the AFE with conventional switches
Figure 6b)(right) Transfer function of the AFE with in-series MOSFETs based switches

Depending on which switch is closed, the input impedance of the AFE switches between 30k□ and 114k□, which fits all the requirements from TABLE 1. This principle can of course be repeated in order to obtain more DC level shift or gain values, for improved flexibility.

The main limit of this interface is technological: the specific analog switches used in the AFE should be implemented preferably in high voltage SOI technologies [18], which are usually not intended for high precision analog applications.

The second limitation comes from the imperfect matching of analog parameters. The two impedance and level adaptation stages shown in Fig. 3a don't perfectly match.This strongly degrades the common-mode rejection ratio of the whole interface, which results in degrading the precision of the measurement. To limit the impact of the unmatching, the interface has to be calibrated, using specific methods such as [11], at the cost of an increased complexity in the measurement process.

VI. CONCLUSION

A new concept of reconfigurable interface for avionic equipment is presented. Such an interface can greatly simplify the design of future avionic computers, and allow two identical computers to be used for different applications, thanks to a flexible hardware. An architecture for this interface has been proposed, built on a mixed signal ASIC used as an analog signal conditioning circuit and a FPGA for signal processing. The analog front-end is based on a simple switched resistors circuit. Such circuits usually cannot operate at voltages higher than their own power supplies. A method using specific analog switches has been proposed to overcome this problem and allow the analog front-end to be programmed with different gains, offsets and impedances, under the high voltage signals and high voltage common-mode noises which can be found for example in avionic or automotive applications. This interface

has been simulated with Cadence Spectre Circuit Simulator, and a prototype interface will soon be produced and tested.

REFERENCES

[1] R. Fuchsen, "Preparing the next generation of IMA: A new technology for the scarlett program," in IEEE/AIAA th Digital Avionics Systems Conference, 2009.

[2] ARINC (Aeronautical Radio Inc.), "Mark33 Digital Information Transfer System (Part1). ARINC SPECIFICATION 429P1," 1995.

[3] A. Canu, P. Benabes, D. Faura, P. Toillon et M. Gatti, «A Versatile Input Interface for Avionic Computers,» chez *IEEE/AIAA 30th Digital Avionics System Conference*, Seattle, Washington, USA, 2011.

[4] A. Flammini, D. Marioli, E. Sisinni and A. Taroni, "Least Mean Square Method for LVDT Signal Processing," IEEE Transactions on Instrumentation and Measurement, vol. 56, no. 6, pp. 2294-2300, 2007.

[5] D. Crescini, A. Flammini, D. Marioli and A. Taroni, "Application of an FFT-based algorithm to signal processing of LVDT position sensors," in IEEE Instrumentation and Measurement Technology Conference, St Paul, Minnesota, USA, 1998.

[6] N. Aibe and M. Yasunaga, "Meta I/O Interface using Reconfigurable LSIs," in IEEE 42th Midwest Symposium on Circuit and Systems, 2004.

[7] P. Gulak, "Field Programmable Analog Arrays: Past, Present and Future Perspectives," in IEEE International Conference on Microelectronics, 1995.

[8] A. Aubert and C. Ruby, "FPAA: Commercial Offer (Offre Commerciale)," Techniques de l'Ingenieur, vol. E2, no. 516, 2004.

[9] M. Kucic, «Programmable and Adaptative Analog Filters using Arrays of Floating-Gate Circuits,» chez *Proceedings of the Advanced Research in VLSI Conference*, Salt Lake City, 2001.

[10] Actel, 11 2011[Online]. Available: http://www.actel.com/documents/SmartFusion_DS.pdf.

[11] I. S. Souza, "Mixed Signal Reconfigurable Inteface for Medical Instrumentation Applications", PhD Thesis, ENST, Paris, 2003.

[12] S. Catunda, J.-F. Naviner, R. Freire and G. Pinheiro, "Programmable gain and DC level shift analog sgnal conditioning circuit: microcontroller based implementation," in *IEEE Instrumentation and Measurement technology Conference*, 2005.

[13] ON Semiconductor, 11 2011. [Online]. Available: http://www.onsemi.com/PowerSolutions/content.do?id=16697.

[14] XFab, 11 2011. [Online]. Available: http://www.xfab.com/en/technology/soi.html.

[15] EUROCAE (The European Organisation for Civil Aviation Equipment), "DO160-F. Environmental Conditions and Test Procedures for Airborne Equipment," 2008.

[16] S. Catunda, J.-F. Naviner, G. Deep and R. Freire, "Designing a Programmable Analog Signal Conditioning Circuit Without Loss of Measurement Range," *IEEE Transactions on Instrumentation and Measurement*, vol. 52, no. 5, pp. 1482-1487, 2003.

[17] Intersil, "Common Questions Concerning CMOS Analog Switches," Application Note AN532.1, 2005.

[18] Vishay Siliconix, "Overvoltage Protection for CMOS Switches and Multiplexers," Application Note AN205, 2003