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# A gm/ID-Based Noise Optimization for CMOS Folded-Cascode Operational Amplifier

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noise parameter. According to this model,  $\gamma$  approaches 1 when the drain-to-source voltage ( $V_{DS}$ ) approaches zero and decreases to 2/3 when the device enters the saturation regime [2]. A procedure for extracting  $\gamma$  as a function of  $g_m/I_D$ ,  $V_{SB}$ ,  $V_{DS}$ , and  $L$  was described in [4]. If we divide (1) by  $g_m^2$ , we have the thermal noise present at the gate

$$\overline{v_{ng,th}^2} = \frac{4kT\gamma}{g_m}. \quad (2)$$

## B. Flicker Noise

Since MOSFETs are surface-conduction devices, flicker noise is important at low frequencies. The flicker noise at the drain terminal is [2]

$$\overline{i_{nd,fn}^2} = \frac{K_f}{C_{ox}WL} \frac{g_m^2}{f} \quad (3)$$

where  $K_f$  is a process parameter that depends on the  $W$  and  $L$  of a transistor [1],  $C_{ox}$  is the oxide capacitance,  $W$  is the width, and  $L$  is the length. At the device noise corner frequency ( $f_{co}$ ), the thermal noise is equal to the flicker noise

$$\overline{i_{nd,th}^2} = 4kT\gamma g_m = \frac{K_f}{C_{ox}WL} \frac{g_m^2}{f_{co}} = \overline{i_{nd,fn}^2}. \quad (4)$$

We solve (4) to get an expression for  $f_{co}$ . Similar to  $\gamma$ ,  $f_{co}$  is a function of  $g_m/I_D$ , as well as  $V_{SB}$ ,  $V_{DS}$ , and  $L$ , through its dependence on the current density [4]

$$f_{co} = \frac{K_f}{C_{ox}L} \frac{g_m}{I_D} \frac{I_D}{W} \frac{1}{4KT\gamma}. \quad (5)$$

Multiplying  $\overline{i_{nd,fn}^2}$  in (4) by  $f_{co}$ , we have

$$\overline{i_{nd,th}^2} f_{co} = \frac{K_f}{C_{ox}WL} g_m^2. \quad (6)$$

Substituting (6) into (3), we have a simple equation that relates the thermal noise current to the flicker noise current

$$\overline{i_{nd,fn}^2} = \overline{i_{nd,th}^2} \frac{f_{co}}{f}. \quad (7)$$

Dividing (7) by  $g_m^2$ , we have the gate-referred flicker noise

$$\overline{v_{ng,fn}^2} = \overline{v_{ng,th}^2} \frac{f_{co}}{f}. \quad (8)$$

## C. Gate-Referred Noise Voltage

The total noise at the gate terminal consists of the thermal noise as well as the flicker noise. Using (8) and (2), the total noise at the gate terminal is

$$\overline{v_{ng}^2} = \overline{v_{ng,th}^2} + \overline{v_{ng,fn}^2} = \frac{4kT\gamma}{g_m} \left( 1 + \frac{f_{co}}{f} \right). \quad (9)$$

Equation (9) shows that, once  $I_D$  is fixed,  $\overline{v_{ng}^2}$  (the gate-referred noise) depends on  $g_m/I_D$  parameters such as  $\gamma$  and  $f_{co}$ .

## III. ANALYSIS OF A FOLDED-CASCODE OTA

The noise at the output of the OTA in Fig. 1 is contributed mostly by  $M_1 - M_2$ ,  $M_3 - M_4$ , and  $M_9 - M_{10}$ . Assuming that each transistor contributes noise independently, the output-referred noise is

$$\overline{v_{n,out}^2} = 2 \left( A_o^2 \overline{v_{n1}^2} + R_{out}^2 \frac{g_{m5}^2}{(g_{m5} + g_{ds1} + g_{ds3})^2} g_{m3}^2 \overline{v_{n3}^2} + R_{out}^2 \frac{g_{m7}^2}{(g_{m7} + g_{ds9})^2} g_{m9}^2 \overline{v_{n9}^2} \right). \quad (10)$$

We drop “g” from the subscript of the gate-referred noise to simplify the notation.  $\overline{v_{n1}^2}$ ,  $\overline{v_{n3}^2}$ , and  $\overline{v_{n9}^2}$  are the gate-referred noise of  $M_1$ ,  $M_3$ , and  $M_9$  as indicated by (9).  $A_o$  is the differential gain of the folded cascode, and  $R_{out}$  is the output resistance into  $M_5$  and  $M_7$

$$A_o = g_{m1} R_{out} \frac{g_{m5}}{g_{m5} + g_{ds1} + g_{ds3}}. \quad (11)$$

The input-referred noise of the folded-cascode OTA can be obtained by dividing (10) by  $A_o^2$

$$\overline{v_{n,in}^2} = 2 \left( \overline{v_{n1}^2} + \alpha_3^2 \overline{v_{n3}^2} + \alpha_9^2 \overline{v_{n9}^2} \right) \quad (12)$$

where  $\alpha_3 = g_{m3}/g_{m1}$  and  $\alpha_9$  is

$$\alpha_9 = \frac{g_{m9}}{g_{m1}} \frac{g_{m5} + g_{ds1} + g_{ds3}}{g_{m5}} \frac{g_{m7}}{g_{m7} + g_{ds9}}. \quad (13)$$

Since  $M_1$ ,  $M_3$ ,  $M_5$ ,  $M_7$ , and  $M_9$  are designed to operate in the saturation region, the self-gain ( $g_m/g_{ds}$ ) values of these transistors are large, and  $\alpha_9 \approx g_{m9}/g_{m1}$ .

## IV. DESIGN CONSIDERATIONS

### A. Design Specifications

We design a low-noise folded-cascode amplifier to demonstrate the tradeoffs using the  $g_m/I_D$  design flow. A 130-nm CMOS process with a 1.2-V power supply is used. The specifications are as follows: a slew rate of 7.5 V/ $\mu$ s, a load capacitance of 100 pF, a unity bandwidth of 10 MHz, an input/output common mode voltage of 0.6 V, a current consumption of 75  $\mu$ A, and a small signal gain in excess of 40 dB. The circuit shown in Fig. 1 required a common-mode feedback (CMFB) circuit (not shown) with a bias current of 37.5  $\mu$ A. The maximum device noise corner frequency is 20 kHz. The current ratio ( $I_{D3}/I_{D1}$ ) is 2.

### B. Input Differential Pair

The bias current of  $M_1$  is constrained by the product of the slew rate and the load capacitance. The transconductance of  $M_1$  is constrained by the product of the unity gain bandwidth and the load capacitance.  $g_{m1}/I_1$  is therefore proportional to the ratio of the unity bandwidth and the slew rate [9]. Using the slew rate of 7.5 V/ $\mu$ s and the load capacitance of 100 pF, the  $g_{m1}/I_1$  is 16.75 S/A.

The aspect ratio of  $M_1$  is chosen to maximize the gain and minimize the input-referred noise of the OTA while keeping  $W_1$  less than 100  $\mu$ m.  $L_1$  was initially set to 4  $\mu$ m to maximize  $g_{m1}/g_{ds1}$  [see Fig. 2(a)] and minimize  $\overline{v_{n1}^2}$  [see Fig. 2(c)].

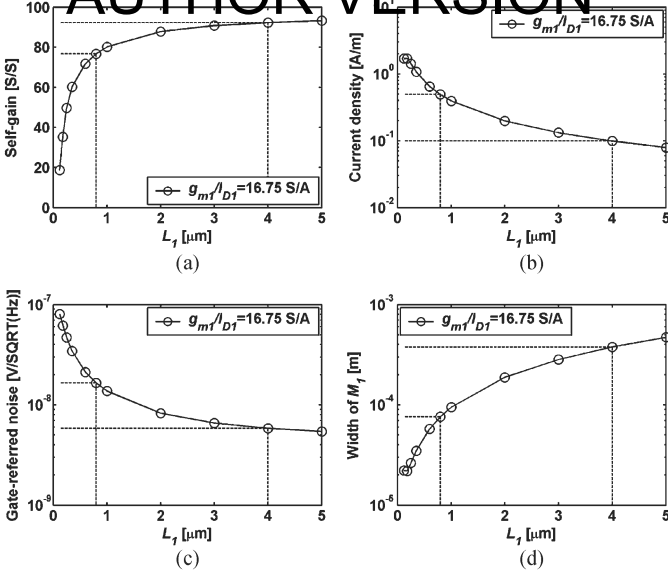


Fig. 2. Tradeoffs of the input differential pair. (a) Self-gain ( $g_{m1}/g_{ds1}$ ). (b) Current density ( $I_{D1}/W_1$ ). (c) Gate-referred noise ( $\sqrt{v_{n1}^2}$ ). (d) Width ( $W_1$ ) of  $M_1$  as a function of  $L_1$ , the length of  $M_1$ .  $g_m/I_D$  parameters were extracted and interpolated from transistor-level simulations.  $I_{D1} = 37.5 \mu\text{A}$ .  $g_{m1}/I_{D1}$  is fixed at 16.75 S/A.

Setting  $L_1$  equal to 4  $\mu\text{m}$ , however, increases  $W_1$  beyond 100  $\mu\text{m}$  [see Fig. 2(d)]. To keep  $W_1$  less than 100  $\mu\text{m}$ , the current density of  $L_1$  is increased [see Fig. 2(b)] by reducing  $L_1$  to 0.8  $\mu\text{m}$  at the expense of a slightly lower  $g_{m1}/g_{ds1}$  and higher  $\sqrt{v_{n1}^2}$ . Using  $L_1 = 0.8 \mu\text{m}$  and  $g_{m1}/I_1 = 16.75$  S/A,  $W_1$  is set to 76.20  $\mu\text{m}$ .

### C. Cascode Transistor

The aspect ratio of  $M_5$  is designed to maximize  $g_{m5}/g_{ds5}$  (and hence  $A_o$ ) while keeping  $W_5$  less than 100  $\mu\text{m}$ . The gate-referred noise is negligible since  $M_5$  is in a cascode configuration. The design variables are  $g_{m5}/I_{D5}$  and  $L_5$ .

The minimum channel length is rarely used in analog design. A reasonable starting point for  $L_5$ , the length of  $M_5$ , is  $L_5 = 5L_{\min}$  [10]. The exact starting point for  $L_5$  is not critical. To explore the design space of  $g_{m5}/I_{D5}$  and  $L_5$ , the self-gain of  $M_5$  ( $g_{m5}/g_{ds5}$ ) is plotted in Fig. 3(a) as a function of  $g_{m5}/I_{D5}$  at  $L = 5L_{\min}$  and  $L = 25L_{\min}$ .  $L_{\min}$  is equal to 120 nm. Fig. 3(a) reveals that  $g_{m5}/g_{ds5}$  is maximum for  $g_{m5}/I_{D5}$  between 20 and 30 S/A. Therefore,  $20 \text{ S/A} \leq g_{m5}/I_{D5} \leq 30 \text{ S/A}$  is used to explore the design space for  $L_5$ .

Fig. 3(c) shows that  $g_{m5}/g_{ds5}$  increases with  $L_5$  for  $L_5 \leq 0.8 \mu\text{m}$  and saturates for  $L_5 > 0.8 \mu\text{m}$ .  $L_5$  is set to 0.8  $\mu\text{m}$  to maximize  $g_{m5}/g_{ds5}$  without increasing  $W_5$  excessively [see Fig. 3(d)].  $g_{m5}/I_{D5}$  is set to 20 S/A to increase the current density [see Fig. 3(b)] and minimize  $W_5$  without a substantial decrease in  $g_{m5}/g_{ds5}$ . The  $W/L$  ratio for  $M_5$  is equal to 17.2  $\mu\text{m}/0.8 \mu\text{m}$ .

### D. Load Transistor

The aspect ratio of  $M_3$  is designed to maximize  $g_{m3}/g_{ds3}$  and minimize the gate-referred noise of  $M_3$ . The design variables are  $g_{m3}/I_{D3}$  and  $L_3$ .

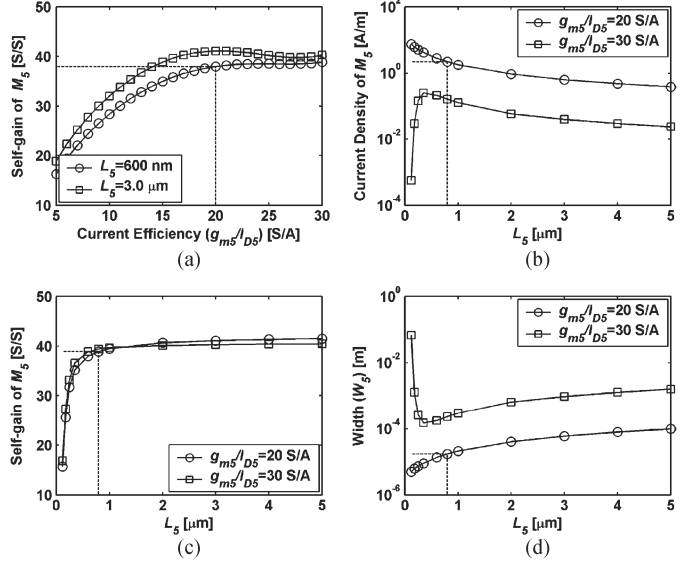


Fig. 3. Tradeoffs of the cascode transistor ( $M_5$ ). (a) Self-gain of  $M_5$  as a function of  $g_{m5}/I_{D5}$ . (b) Current density ( $I_{D5}/W_{D5}$ ). (c) Self-gain ( $g_{m5}/g_{ds5}$ ). (d) Width of  $M_5$  as a function of  $L_5$ , the length of  $M_5$ .  $I_{D5} = 37.5 \mu\text{A}$ .  $g_m/I_D$  parameters were extracted and interpolated from transistor-level simulations.

The design space for  $g_{m3}/I_{D3}$  is derived as follows. First, according to (5),  $f_{co}$  is inversely proportional to  $L$ ; therefore, a sufficiently long transistor should be used to minimize  $f_{co}$ . Second, as  $g_m/I_D$  increases, the current density decreases at a rate faster than the rate at which  $g_m/I_D$  increases; therefore,  $f_{co}$  decreases with  $g_m/I_D$ . (This point is explored further in Section V-B.) Consequently, the minimum  $g_{m3}/I_{D3}$  is determined by the  $f_{co3}$  requirement. Fig. 4(a) shows that, to keep  $f_{co3}$  less than 20 kHz,  $g_{m3}/I_{D3}$  must exceed 19 S/A for  $L_3 = 3 \mu\text{m}$ . A shorter channel length, such as  $L_3 = 600$  nm, fails to meet the minimum  $f_{co}$  requirement for  $g_{m3}/I_{D3}$  less than 30 S/A. Third, the maximum  $g_{m3}/I_{D3}$  is determined by the minimum  $g_{m3}/g_{ds3}$  and the maximum  $W_3$  since both  $W_3$  [see Fig. 4(c)] and  $g_{m3}/g_{ds3}$  [see Fig. 4(e)] increase with  $g_{m3}/I_{D3}$ . A current efficiency ( $g_{m3}/I_{D3}$ ) of 25 S/A is chosen as a compromise. For  $L = 3 \mu\text{m}$ , the design space for  $g_{m3}/I_{D3}$  is  $19 \text{ S/A} \leq g_{m3}/I_{D3} \leq 25 \text{ S/A}$ .

The design space for  $L_3$  is determined as follows. For a  $f_{co3} = 20$  kHz, the minimum  $L_3$  is 2  $\mu\text{m}$  for  $g_{m3}/I_{D3} = 25$  S/A and 3  $\mu\text{m}$  for  $g_{m3}/I_{D3} = 19$  S/A according to Fig. 4(b). To keep  $W_3$  less than 300  $\mu\text{m}$ , the maximum  $L_3$  is 2.5  $\mu\text{m}$  for  $g_{m3}/I_{D3} = 25$  S/A and 8.0  $\mu\text{m}$  for  $g_{m3}/I_{D3} = 19$  S/A according to Fig. 4(d). Fig. 4(f) shows that  $g_{m3}/g_{ds3}$  is higher for  $g_{m3}/I_{D3} = 25$  S/A. We set  $g_{m3}/I_{D3} = 25$  S/A to get a higher  $g_{m3}/g_{ds3}$ . Based on the discussion so far, we deduce that the design space for  $L_3$  is  $L_{3,\min} = 2.0 \mu\text{m} < L < L_{3,\max} = 2.5 \mu\text{m}$ . We set  $L_3$  equal to 2.0  $\mu\text{m}$  in order to minimize  $W_3$ . The  $W/L$  ratio for  $M_3$  is equal to 248.5  $\mu\text{m}/2.0 \mu\text{m}$ .

### E. Aspect Ratios of the Remaining PMOS Transistors

The remaining PMOS transistors in Fig. 1 are designed using the same method described in Sections IV-C and IV-D. The aspect ratio for  $M_7$  and  $M_9$  are 89.00  $\mu\text{m}/0.35 \mu\text{m}$  and 48.4  $\mu\text{m}/0.60 \mu\text{m}$ , respectively. The  $g_m/I_D$  values for  $M_7$  and  $M_9$  are 20 and 15 S/A, respectively.

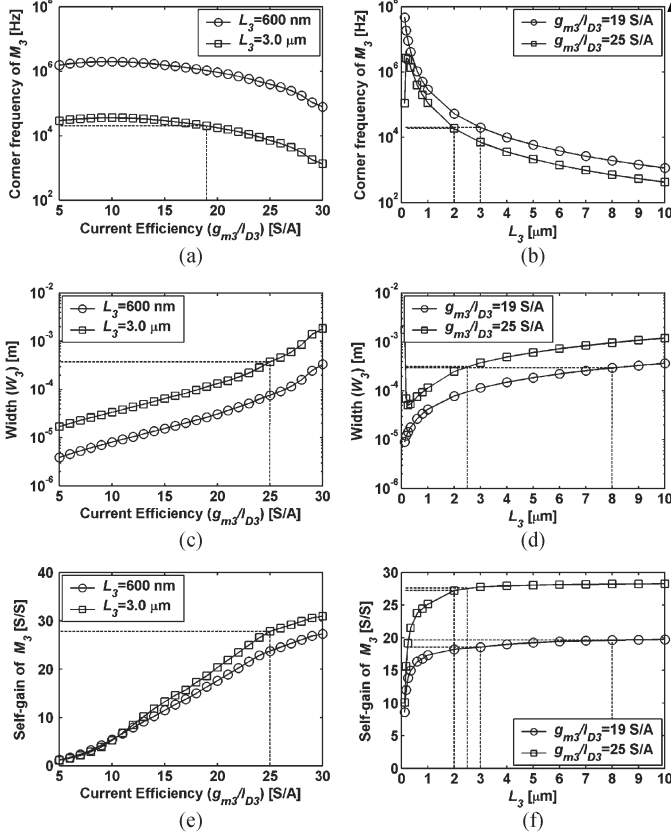


Fig. 4. Tradeoffs of the load transistor ( $M_3$ ). (a) Corner frequency ( $f_{co3}$ ), (c) width, and (e) self-gain ( $g_{m3}/g_{d3}$ ) of  $M_3$  as a function of  $g_{m3}/I_{D3}$  of  $M_3$ . (b) Corner frequency, (d) width, and (f) self-gain of  $M_3$  as a function of  $L_3$ , the length of  $M_3$ .  $I_3 = 75 \mu\text{A}$ . The  $g_m/I_D$  parameters were extracted and interpolated from transistor-level simulations.

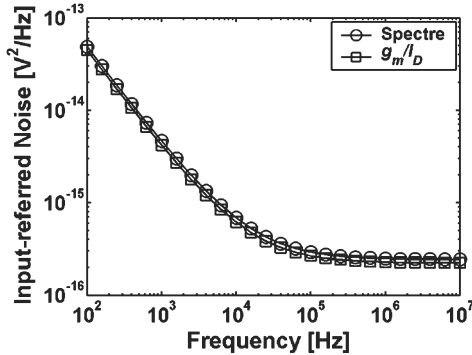


Fig. 5. Comparison of  $\overline{v_{n,in}^2}$  simulated using Spectre and  $\overline{v_{n,in}^2}$  calculated using the  $g_m/I_D$  method.

### F. Simulation

Fig. 5 shows the comparison between the input-referred noise of a folded-cascade OTA obtained using Spectre and the input-referred noise calculated with (12). The transistors are modeled using BSIM 4.4. At frequencies lower than the noise corner frequency of the amplifier ( $f_{co,ota}$ ),  $\overline{v_{n,in}^2}$  is dominated by the flicker noise of  $\overline{v_{n1}^2}$ ,  $\overline{v_{n3}^2}$ , and  $\overline{v_{n9}^2}$ . At frequencies higher than  $f_{co,ota}$ ,  $\overline{v_{n,in}^2}$  is dominated by the thermal noise of  $\overline{v_{n1}^2}$ ,  $\overline{v_{n3}^2}$ , and  $\overline{v_{n9}^2}$ . Using Spectre as the standard of comparison, the percentage error from 100 Hz to 10 MHz is less than 10.5%.

### A. Derivation

In this section, we derive an expression for  $f_{co,ota}$  that corresponds to  $\gamma$  and  $f_{co}$  of the transistors in the folded-cascade amplifier. We start by rewriting (12) to separate the thermal noise from the flicker noise

$$\overline{v_{n,in,th}^2} = 2 \left( \overline{v_{n1,th}^2} + \alpha_3^2 \overline{v_{n3,th}^2} + \alpha_9^2 \overline{v_{n9,th}^2} \right) \quad (14)$$

$$\overline{v_{n,in,fn}^2} = 2 \left( \overline{v_{n1,fn}^2} + \alpha_3^2 \overline{v_{n3,fn}^2} + \alpha_9^2 \overline{v_{n9,fn}^2} \right). \quad (15)$$

At  $f = f_{co,ota}$ ,  $\overline{v_{n,in,th}^2} = \overline{v_{n,in,fn}^2}$ . We set (14) equal to (15), replace the gate-referred flicker noise of each transistor using (8), and obtain

$$\overline{v_{n1,th}^2} + \alpha_3^2 \overline{v_{n3,th}^2} + \alpha_9^2 \overline{v_{n9,th}^2} = \overline{v_{n1,th}^2} \frac{f_{co1}}{f_{co,ota}} + \alpha_3^2 \overline{v_{n3,th}^2} \frac{f_{co3}}{f_{co,ota}} + \alpha_9^2 \overline{v_{n9,th}^2} \frac{f_{co9}}{f_{co,ota}}. \quad (16)$$

Solving (16) for  $f_{co,ota}$  produces

$$f_{co,ota} = \frac{f_{co1} + \alpha_3^2 \frac{\overline{v_{n3,th}^2}}{\overline{v_{n1,th}^2}} f_{co3} + \alpha_9^2 \frac{\overline{v_{n9,th}^2}}{\overline{v_{n1,th}^2}} f_{co9}}{1 + \alpha_3^2 \frac{\overline{v_{n3,th}^2}}{\overline{v_{n1,th}^2}} + \alpha_9^2 \frac{\overline{v_{n9,th}^2}}{\overline{v_{n1,th}^2}}}. \quad (17)$$

Recall from (2) that  $\overline{v_{ng,th}^2} = 4kT\gamma/g_m$ . Therefore,  $\overline{v_{n3,th}^2}/\overline{v_{n1,th}^2}$  and  $\overline{v_{n9,th}^2}/\overline{v_{n1,th}^2}$  in (17) can be simplified to

$$\frac{\overline{v_{n3,th}^2}}{\overline{v_{n1,th}^2}} = \frac{\gamma_3 g_{m1} I_3}{\gamma_1 I_1 g_{m3} I_3} \quad (18)$$

$$\frac{\overline{v_{n9,th}^2}}{\overline{v_{n1,th}^2}} = \frac{\gamma_9 g_{m1} I_9}{\gamma_1 I_1 g_{m9} I_9}. \quad (19)$$

Using (18) and (19), as well as the definition for  $\alpha_3$  and  $\alpha_9$ ,  $f_{co,ota}$  can be associated with each transistor's  $f_{co}$

$$f_{co,ota} = c_1 f_{co1} + c_3 f_{co3} + c_9 f_{co9} \quad (20)$$

where  $c_1$ ,  $c_3$ , and  $c_9$  are defined as

$$c_1 = \frac{1}{1 + \frac{\gamma_3 g_{m3} I_1 I_3}{\gamma_1 I_3 g_{m1} I_1} + \frac{\gamma_9 g_{m9} I_1 I_9}{\gamma_1 I_9 g_{m1} I_1}} \quad (21)$$

$$c_3 = \frac{\frac{\gamma_3 g_{m3} I_1 I_3}{\gamma_1 I_3 g_{m1} I_1}}{1 + \frac{\gamma_3 g_{m3} I_1 I_3}{\gamma_1 I_3 g_{m1} I_1} + \frac{\gamma_9 g_{m9} I_1 I_9}{\gamma_1 I_9 g_{m1} I_1}} \quad (22)$$

$$c_9 = \frac{\frac{\gamma_9 g_{m9} I_1 I_9}{\gamma_1 I_9 g_{m1} I_1}}{1 + \frac{\gamma_3 g_{m3} I_1 I_3}{\gamma_1 I_3 g_{m1} I_1} + \frac{\gamma_9 g_{m9} I_1 I_9}{\gamma_1 I_9 g_{m1} I_1}}. \quad (23)$$

### B. Discussion

The ratio of  $c_3$  and  $c_1$  and the ratio of  $c_9$  and  $c_1$  are given by

$$\frac{c_3}{c_1} = \frac{\gamma_3 g_{m3} I_1 I_3}{\gamma_1 I_3 g_{m1} I_1} \quad (24)$$

$$\frac{c_9}{c_1} = \frac{\gamma_9 g_{m9} I_1 I_9}{\gamma_1 I_9 g_{m1} I_1}. \quad (25)$$

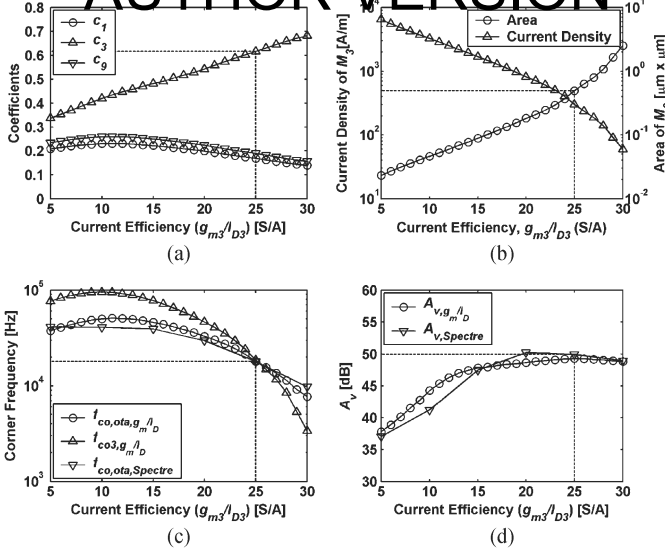


Fig. 6. Tradeoffs of the OTA. (a) Corner frequency coefficients ( $c_1$ ,  $c_3$ , and  $c_9$ ). (b) Area and current density. (c) Contribution of  $f_{co3}$  to  $f_{co,ota}$ . (d) Voltage gain of the OTA as a function of  $g_{m3}/I_{D3}$ .  $L_3 = 2.0 \mu\text{m}$ .  $I_3 = 75 \mu\text{A}$ .

Using results from Section IV, i.e.,  $\gamma_3/\gamma_1 = 1.245$ ,  $g_{m3}/I_{D3} = 25$ ,  $g_{m1}/I_{D1} = 16.75$ , and  $I_3/I_1 = 2$ ,  $c_3/c_1$  is 3.65. Using  $\gamma_9/\gamma_1$ ,  $g_{m9}/I_{D9} = 15$ , and  $I_9/I_1 = 1$ ,  $c_9/c_1$  is 1.125. Since  $c_3/c_1 = 3.65$  and  $c_9/c_1 = 1.125$ , we conclude that  $c_3 > c_9 > c_1$ .

Since  $g_{m1}/I_{D1}$  is determined by the unity gain bandwidth and the slew rate,  $c_3/c_1$  is controlled by  $g_{m3}/I_{D3}$  and  $I_3/I_1$  according to (24). We explore the use of  $g_{m3}/I_{D3}$  and the current ratio ( $I_{D3}/I_{D1}$ ) as the design variables next.

The current efficiency of  $M_3$  ( $g_{m3}/I_{D3}$ ) appears in the denominator of (21) and (23); therefore, both  $c_1$  and  $c_9$  decrease slightly while  $c_3/c_1$  remains constant as  $g_{m3}/I_{D3}$  is increased according to Fig. 6(a). According to (24),  $c_3/c_1$  is proportional to  $g_{m3}/I_{D3}$ , suggesting that, as  $g_{m3}/I_{D3}$  increases,  $f_{co,ota}$  becomes increasingly determined by  $f_{co3}$ .

The noise corner frequency ( $f_{co}$ ) of each transistor depends on its  $g_m/I_D$ ,  $V_{SB}$ ,  $V_{DS}$ , and  $L$ . Changing  $g_{m3}/I_3$ , for example, changes  $f_{co3}$ , but not  $f_{co1}$  and  $f_{co9}$ . As  $g_{m3}/I_{D3}$  increases, the current density of  $M_3$  is reduced [see Fig. 6(b)] at a rate faster than the increase in  $g_{m3}/I_{D3}$  [see (5)]; therefore,  $f_{co3}$  is reduced. The decrease in the corner frequency of  $M_3$  as a function of  $g_{m3}/I_{D3}$  is shown in Fig. 6(c), as well as the resulting change in the corner frequency of the OTA. As a comparison, we show both the calculated OTA corner frequency ( $f_{co,ota,g_m/I_D}$ ) and simulated OTA corner frequency ( $f_{co,ota,Spectre}$ ) in Fig. 6(c).

The gain of the OTA depends on  $g_{m3}/g_{ds3}$ . As  $g_{m3}/I_{D3}$  increases, the change in  $g_{m3}/g_{ds3}$  observed in Fig. 4(e) results in the saturation of  $A_V$  at  $g_{m3}/I_{D3} = 20$  in Fig. 6(d). The decrease in current density as  $g_{m3}/I_{D3}$  increases results in a corresponding increase in  $W_3$  and, hence, an increase in the

area observed in Fig. 6(b). Fig. 6 confirms our earlier selection of  $g_{m3}/I_{D3}$  as the optimum value for noise, gain, and area.

Equation (24) suggests that  $f_{co,ota}$  is a function of the current ratio ( $I_3/I_1$ ). Our calculation shows that  $f_{co,ota}$  is, at most, a weak function of the current ratio since  $I_3/I_1$  appears in both the numerator and the denominator of (22). For a  $I_3/I_1 = 2$ ,  $f_{co,ota}$  is 17.99 kHz. For a  $I_3/I_1 = 1.5$ ,  $f_{co,ota}$  is 17.63 kHz. In other words, a reduction of  $I_3/I_1$  by 25% only leads to a reduction of  $f_{co,ota}$  by 2%.

## VI. CONCLUSION

Leveraging on the insight gained from our previous work in  $g_m/I_D$ -based noise analysis with  $\gamma$  and  $f_{co}$ , we use  $g_m/I_D$  noise parameters to explore the design space systematically and make transistor-level tradeoff decisions based on requirements for transistor area, noise, and gain. We identify the design bottleneck for the folded-cascode amplifier by developing a closed-form formula for the noise corner frequency of the OTA. The method described in this brief is general and can be applied to design a wide variety of low-noise circuits. Moreover, the noise equations derived in this brief can be integrated in a computer-aided design tool to simplify nanoscale MOSFET circuit design.

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