Mismatch calibration methods for high-speed time-interleaved ADCs

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Abstract—**Time Interleaved ADCs (TIADCs) are a good solution to implement high sampling rate converters at a moderate hardware cost. However, they suffer from mismatches between the ADC channels, such as offset, gain, timing skew and possibly bandwidth mismatches. These mismatches have to be corrected in order to get sufficient performances from the converter. This paper presents the classical calibration methods and focuses on the blind ones. Among those, both mixed analog-digital methods and fully digital methods are overviewed. By considering the state-of-the-art of published chips, a comparison between those methods is provided.**

Keywords—*time-interleaved, ADC, mistatch calibration, blind methods, mixed calibration*

I. Introduction

Time Interleaved ADCs (TIADC) are an increasingly used solution to implement high sampling rate ADCs at a moderate hardware cost [1]. They are comprised of M single converters operating in parallel at a frequency F_s/M, where F_s is the sampling frequency of the overall TIADC. However, due to the manufacturing process, the sub-converters have slightly different characteristics causing mismatches. Offset mismatch occurs when the sub-ADCs have different offset values whereas gain mismatch happens when the sub-ADCs have different gain values. Timing skew mismatch is due to the fact that the sub-ADCs sample the signal with a small timing offset with respsect to their ideal sampling time. Finally, bandwidth mismatch happens when the sub-ADC sampling front-ends have different frequency responses, for example different cut-off frequencies.

The mismatches deteriorate the TIADC output signal by creating mismatch noise, a sum of spurious tones and aliased versions of the input signal. They consequently become a limiting factor in the design of high-speed TIADCs as they reduce the SNDR and the SFDR of the converter. For that reason, it has long been a challenge to correct these mismatches and several approaches have been proposed. They can be classified into different categories.

Foreground calibration techniques require a known signal, for example a sinewave, at the input of the TIADC during an offline phase [2]. They are not suitable for applications where the converter is always 'on', for example communications sytems. Indeed, temperature variations and aging may require the calibration to be done frequently or even continuously.

These techniques can however find their application in high-end measurement systems where the equipment can often be sent to calibration.

The alternative is background calibration. In that case, the mismatch calibration is performed during the normal operation of the converter, in the background. Background calibration techniques can be subdivided into *blind* and *non blind* techniques.

Non-blind background calibration techniques require to slightly modify the input signal in the analog domain in order to calibrate for the mismatches. For example offset and gain mismatch calibration can be performed by generating a random signal that can either be added to the analog input signal [3] or, multiplied with it [4]. The technique published in [5] performs bandwidth mismatch estimation by adding a known sinewave to the TIADC input signal.

In this special session, we focus on blind background calibration for offset, gain and timing skew mismatches. Blind background calibration techniques are probably the most challenging ones because they need to work with the actual input signal only. In most, if not all blind techniques, the calibration of the mismatches is controlled in the digital domain. If the calibration entirely takes place in the digital domain, we speak about *fully digital calibration* (Fig. 1(a)). When the calibration is done with the help of a feedback to the analog front-end, we talk about *mixed signal calibration* or *mixed calibration* (Fig. 1(b)). In reality none of these methods is fully blind as they require some information about the input signal, for example in terms of spectral content or statistical properties.

Throughout this paper, we aim at providing the reader with a background on blind mismatch calibration techniques. We then analyze the performance of state-of-the-art published chips implementing such techniques and derive some trends and guidelines for the future of TIADC mismatch calibration. Section II focuses on blind *estimation* techniques. Section III analyzes mixed calibration methods while section IV focuses on fully digital mismatch *correction* techniques. Section V provides a comparison of existing chips implementing blind background mismatch calibration.
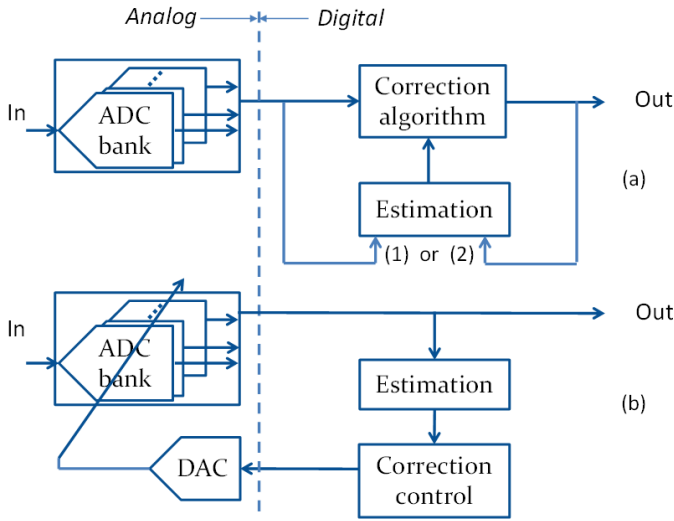
Fig. 1. Classification of TIADC mismatch calibration techniques. (a) Fully digital mismatch calibration. Depending on the technique, the calibration operates in a feedforward manner (1) or in an feedback manner (2) – (b) Mixed mismatch calibration

II. BLIND MISMATCH ESTIMATION TECHNIQUES

A. Offset mismatch estimation

The goal of offset mismatch estimation is to estimate the offsets of the sub-ADCs. We denote o_m the offset of the sub-ADC m and $\hat{o}_m$ its estimated value.

A simple way of performing the estimation is to calculate the average of each sub-ADC output and subtract from it the average of a reference sub-ADC output, e.g. sub-ADC 0 [6]. Assuming that the input signal is Wide-Sense-Stationary (WSS), an estimate of the offset is given by:

$$\hat{o}_m = \frac{1}{N} \sum_{k=0}^{N-1} \tilde{x}[kM + m] - \frac{1}{N} \sum_{k=0}^{N-1} \tilde{x}[kM + 0] \quad (1)$$

where $(\tilde{x}[0] \cdots \tilde{x}[N-1])$ is a batch of samples coming out of the TIADC. More generally, trying to equalize the average of the sub-ADC outputs is a common way of performing offset mismatch calibration [7] [8].

This technique can be implemented at low hardware cost as it only requires one adder per sub-ADC.

B. Gain mismatch estimation

Similarly to offset mismatch estimation, the purpose of gain mismatch estimation is to estimate the relative gains of the sub-ADCs with respect to a reference ADC. This can be done looking at the output power of the signal coming out of each sub-ADC [7].

The estimated relative gain of sub-ADC m, denoted $\hat{g}_m$, can be obtained by calculating the ratio between the average power of sub-ADC m and the average power of a reference sub-ADC, e.g ADC 0:

$$\hat{g}_m = \sum_{k=0}^{N-1} \tilde{x}[kM + m]^2 \bigg/ \sum_{k=0}^{N-1} \tilde{x}[kM + 0]^2 \quad (2)$$

For simplicity, we assume that the offset mismatch is already corrected and that the signal coming out of sub-ADC m has a mean of 0.

Again, this technique can be implemented at a moderate hardware cost. The cost per sub-ADC is only one adder and one multiplier running at the sub-ADC frequency. The division can be done at a lower frequency once the sub-ADC powers are calculated. Plus, it is possible to get rid of the multiplier by replacing the squared value by the absolute value of the samples in Eq. 2 [6].

Alternatively, it is possible to estimate the gain mismatch in the frequency domain by minimizing the mismatch noise created in a frequency band free of signal [9].

C. Timing-skew mismatch estimation

The purpose of timing-skew mismatch estimation is to estimate the relative sampling delay of each sub-ADC with respect to a reference ADC. The estimation can either be performed in the time domain or in the frequency domain. Most methods assume that the input signal is bandlimited to one Nyquist band.

The frequency-based method proposed in [9] requires that the signal is spectrally full except for a small band that must be free of signal. In presence of skew mismatch, this out-of-band contains mismatch noise. The timing offsets are adaptively estimated by minimizing the power in this out-of-band. The techniques described in [7] and [10] are time-based ones. The timing offsets are estimated through the minimization of a cost function calculated from cross-correlations between adjacent channels. In [6] the average of the cross-product between each sub-ADC output samples and its derivative samples is shown to be linearly dependent on its relative timing offset, which enables a direct estimation of the skew mismatch.

III. MIXED CALIBRATION TECHNIQUES

Most mixed calibration methods require the use of one or more redundant sub-ADCs. In the mixed calibration methods, especially skew mismatch calibration, only part of the calibration is done in the digital domain. The techniques presented in [11], [12], [13] randomly reorganize the sampling order of the channels in order to spread the mismatch noise across the entire spectrum.

In [14], the channel offset mismatches are calibrated through digital-controlled corrective current sources embedded in the track-and-hold amplifiers of the sub-ADC. In [15], the timing skew is detected in the digital domain by minimizing the cross-correlation between each sub-ADC and any additional calibration ADC. Then, the timing offsets are adjusted in the analog domain by driving adjustable delay lines. In [16], the offset mismatch is spread out by randomly connecting together unit differential pairs in the comparator preamplifier. The skew mismatch calibration is performed in two phases. First, a time-to-digital signature is stored by inputting to a reference ADC a known binary signal generated by a DAC. Then the sub-ADC to be calibrated are disconnected from the array one after an other and replaced by the reference ADC. Their sampling time is adjusted in the analog domain by comparing their output to the reference ADC signature

with the same binary signal at the input. In [17], the timing delays are adjusted through programmable delay lines by comparing the output of the sub-ADCs to the output of a flash ADC running at the TIADC overall sampling frequency. The technique presented in [8] requires two redundant sub-ADCs, one that serves as a reference and an other that is slightly delayed. The difference between the delayed reference ADC and the reference ADC gives a coarse approximate of the signal derivative, which is used in a correlation-based adaptive algorithm to adjust the timing offsets through a bank of capacitors.

The mixed calibration technique presented in [18] does not require an additional ADC but assumes that the signal is WSS to adaptively estimate the timing skews through a correlation-based algorithm.

IV. Pure digital correction techniques

Pure digital correction of the mismatches is also an alternative and can be used in place of analog trimming.

Offset mismatch can be corrected by subtracting the estimated offset from each sub-ADC digital samples, which only requires an adder per sub-ADC [6]. Similarly, gain mismatch can be corrected by multiplying the output of each sub-ADC by the inverse of its estimated gain, which only requires one multiplier per sub-ADC [6].

Digital skew mismatch correction requires more filtering in order to recover the samples with the correct sampling times. The skew mismatch correction technique implemented in [6] is inspired from the technique presented in [9]. It uses the fact that the timing offset of each ADC is small as compared to the sampling period. In this particular case, the samples can be recovered by doing a first-order Taylor approximation of the skew mismatch error. This requires the use of the signal derivative, obtained by passing the TIADC samples through a digital differentiating FIR filter.

An other possibility is to reconstruct the signal with the help of fractional delay filters as explained in [19]. However, similarly to the derivative-based technique, this method requires a significant amount of digital filtering.

V. Comparison of designed chips

This section aims at comparing the efficiency of mixed calibration techniques and fully digital calibration techniques. For that matter, we consider recent published chips with moderate resolution in the sampling frequency range of 1 to 3 GS/s for which mismatches are performance limiting [6] [8] [17]. Specifically, at these high sampling frequencies, the timing skew mismatch is not negligeable and deteriorates the overall performance.

In [8], 24 SAR ADCs are interleaved to achieve a 2.8 GS/s ADC with 8 effective bits. Skew and offset mismatch calibration are performed adaptively as described in section III.

In [17], 8 SAR ADCs are interleaved to achieve a 1GS/s ADC with 8 effective bits. Adaptive mixed calibration of skew mismatch is performed as explained in section III.

In [6], 12 SAR ADCs are interleaved to achieve a 1.62 GS/s ADC with 8 effective bits. Offset, gain and timing skew
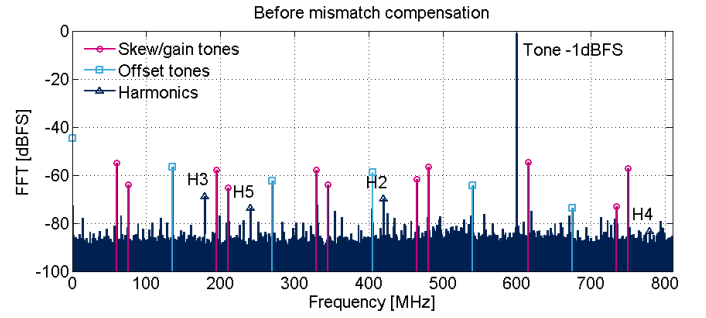

Fig. 2. Output spectrum of the TIADC of [6] before mismatch calibration with a sine input at 600 MHz
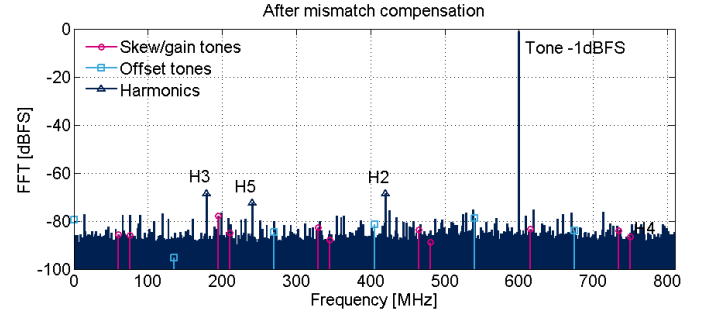

Fig. 3. Output spectrum of the TIADC of [6] before mismatch calibration with a sine input at 600 MHz

mismatch calibrations are fully done in the digital domain. Also, the calibration is done in a feedforward manner, which alleviates the stability issues potentially encountered in adaptive methods. Fig. 2 and 3 illustrates the efficiency of the later solution. Fig. 2 shows the mismatch tones that are present in the output spectrum of the TIADC. As shown in Fig. 3, the mismatch tones are reduced by more than 20 dB after calibration.

Table I summarizes the performance of the cited chips. As explained above, the main difference between them is that [8] and [17] use mixed mismatch calibration whereas [6] uses fully digital mismatch calibration. The fully digital calibration implemented in [6] achieves better performance in reducing the mismatch tones than the mixed calibration techiques implemented in the two other chips. Indeed, it is easier to implement an accurate delay in the digital domain than with an analog delay line. Plus, digital mismatch correction has the advantage of being reusable for any TIADC design, as opposed to analog correction techniques that must be customly designed. The counterpart is that, because of the intensive digital filtering needed to reconstruct the signal, the Figure of Merit (FOM) is worse in [6].

Other chips with blind mismatch calibration exist in other frequency ranges. For example, the TIADC demonstrated in [20] achieves a 800 MS/s by interleaving 2 sub-ADCs and in [16], a sampling frequency of 20 GS/s is reached by interleaving 8 sub-ADCs. However, these chips are not included in the comparison either because of the lack of data about the mismatch calibration performance [20] or because the sampling frequency is not comparable [16].

TABLE I.   PERFORMANCE COMPARISON BETWEEN TIADC CHIPS
WITH PURE DIGITAL MISMATCH CALIBRATION [6] OR MIXED MISMATCH
CALIBRATION [8] [17]

	[8]	[17]	[6]
Technology	65nm	65nm	40nm
Sampling rate [GS/s]	2.8	1.0	1.62
Mismatch tones [dBFS]	60	60	70
SFDR [dBFS]	55	60	62
SNDR [dB]	48	51.4	48
Power [mW]	44.6	19.8	93
FOM [fJ/conv]	62.3	76	283

VI.   CONCLUSION

Blind mismatch calibration for TIADCs has been an extensively treated topic for many years. Throughout this paper, we showed that mixed mismatch calibration techniques are predominant in TIADC chips today. Although purely digital calibration techniques have been studied theoretically, it is only recently that chips implementing this feature have been published. Fully digital calibration of the mismatches is attractive because it requires no custom redesign of the analog front-end of the ADC. Plus, it is easily adaptable to any number of sub-ADCs with higher flexibility and scalability. This is particularly interesting to reduce the time-to-market and the design cost of new generations of TIADCs. The drawback is that the digital power/area overhead which, even if it is expected to slightly decrease with CMOS technology improvement, will likely cause a worse FOM as compared to mixed mismatch calibration techniques. On the other hand, mixed calibration techniques require a more complex design on the analog front-end but can lead to a better FOM than the fully digital calibration.

Therefore, the choice between each of these techniques should be driven by the final application. It depends on the tradeoff between the development cost on one side and the power consumption/area on the other side. Also, it is important to make sure that the requirements of the chosen calibration technique regarding the input signal are compatible with the application. For example, the wide-sense stationarity hypothesis made in [6] is relevant for a communication system but not necessarily for a high-end measurement equipement.

Finally, the TIADCs that have been designed so far in the frequency range of 1 to 3 GS/s do not achieve more that 8 effective bits. In the future, if higher resolutions are targeted the digital calibration techniques may stand an advantage over the mixed calibration methods. Indeed, reaching a fine correction accuracy in the analog domain is more complicated than in the digital domain.

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