Optimization Methodology for a 460-MHz-GBW and 80-dB-SNR Low-Power Current-Mode Amplifier

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ABSTRACT

Biomedical circuits and systems are a forthcoming field in more than Moore integrated circuits. Majority of published works are interested in voltage-mode sensor instrumentation. In voltage-mode operation, design trade-off is known and design optimization tools available. In contrast, current-mode sensor instrumentation have proved low-power and high-speed signal processing. This work addresses a single-objective optimization of a current-mode instrumentation amplifier (IA), including multi-constraints: area, power consumption, gain, speed, noise, and linearity. Post-layout simulation results have proved optimal IA assessments in CMOS 180 nm, achieving power consumption of 1.5 μW, gain of 40 dB using minimal transistor area. Optimized current-mode IA has gain-bandwidth product (GBW) of 459.8 MHz, SNR of 80 dB and THD of -47 dB. Proposed optimization achieves voltage-mode competitive performance, overcoming in low-power and high-speed due to current-mode assets.

Categories and Subject Descriptors

B.7.2 [**Integrated Circuits**]: Design Aids—*Layout,Simulation*

General Terms

Design

Keywords

bio-electronics, optimization methodology, current-mode amplifier, low-power, high-performance

1. INTRODUCTION

Bio-electronics has become a key research application to healthcare improvement. Sensors have been applied to instrument physiological properties of biological materials, ranging from lab-on-chip to medical imaging [1]. Bio-instrumentation is increasing considerably in importance as a method of monitoring and stimulation [17]. Bio-impedance spectroscopy [18], biomedical application [7], biopotential measurements [9], cardiac and neural stimulation [11, 13] have highlighted emergent bio-electronics circuitry.

Instrumentation amplifier (IA) has an important role in a bio-sensor system as it is the first block in an analog front-end. Voltage-mode IA is largely discussed in the state-of-the-art exploring design trade-offs to achieve dynamic range and speed while keeping a low power consumption. Besides intuitive voltage-mode operation, current-mode IA presents several advantages in the state-of-the-art. Increased dynamic range, high speed, and low-power consumption are distinguished characteristics of current-mode circuitry [10, 14]. Moreover, current-mode signal processing presents lower implementation costs in adders (circuit node), gains (current-mirrors) [15], multipliers [19], and comparators [7].

Besides current-mode potentials, only few works addresses the problem: how to find optimal performance and balance design trade-offs. E. Brun [2] has presented analytical equations to express the linearity of current-mode IAs using the total harmonic distortion (THD). Mian et al. [12] have highlighted noise and bandwidth trade-off in current-mode IAs. Ferreira et al. [5] have revealed noise and linearity trade-off in current-mode IAs. To the best of our knowledge, there is no work addressing design optimization in current-mode IA which includes a single-objective with the multi-constraints: area, power consumption, gain, speed, noise, and linearity.

Motivated by advantageous current-mode assets for bio-electronic instrumentation and signal processing, this work presents a low-power high-performance IA design optimization. To clarify current-mode IA trade-offs, a single-objective design optimization is carried on in terms of speed, area, power consumption constraints for a dynamically regulated cascode current mirror (DRCCM) [5]. Analytical expressions are also presented for gain, bandwidth, noise, and linearity. This paper proposes a single-objective cost function assembling aforementioned criteria. A low-power high-performance DRCCM is proposed in CMOS 180 nm. Post-layout simulations are presented to verify optimal DRCCM design in terms of process and temperature variations.

The rest of this paper is organized as follows. Section 2 describes the current-mode IA interest for biomedical applications. Section 3

highlights the state-of-the-art in voltage- and current-mode IA. Section 4 addresses a single-objective multi-constraints optimization. A complete performance analysis is presented establishing design trade-offs for DRCCM characteristics of area, power consumption, gain, speed, noise, and linearity. Section 5 shows post-layout simulation results of the optimum-designed IAs. Moreover, outstanding results of proposed amplifier are compared to the state-of-the-art of voltage- and current-mode IAs. Finally, conclusions are presented.

2. IA INTEREST FOR BIOMEDICAL APPLICATIONS

Medical applications that take advantage of integrated systems are classified in two main categories: body signals monitoring and stimulation. In both cases, biomedical signal have distinguishing features of other signals; they are low voltage and low frequency [4]. Shrinking power consumption specifications urges optimized embedded circuits and systems. For example, this requirement imposes IAs to be able to operate under low voltage, which current-mode IAs are a prominent solution.

Biomedical signals monitoring, such as EEG and ECG signals, is characterized by a low detection-levels (i.e. 1 to 100 μV) and very low frequencies (few Hertz). Unfortunately, these signal also contains DC component of several millivolts due to electrodes. The first building block of a biomedical monitoring system is an IA. The IA must present a very low input-referred noise and high CMRR. In a classic topology of voltage-mode IA, CMRR greatly depend on the resistor network matching. Thus, a solution based on current-mirroring amplifiers is more suitable according to [11] and [20].

Neural stimulation is a treatment for many neurological disorders. Neural stimulation sensors requires current-mode stimulation signals using a direct current control [17]. However, voltage-mode stimulation delivers higher output current to the tissue for a given supply voltage; which may induce permanent damage [6]. That's why, current-mode stimulators are extensively employed. An interesting application for current-mode IAs is the transcranial Direct Current Stimulation (tDCS). The tDCS method consists of a direct injection of modulated low amplitude current (few mA), that allows the stimulation and monitoring of a wide spectrum of neurological function (e.g. perceptual, motor, cognitive and affective) [13].

The tDCS method achieves high level of effectiveness and safety for the human being. This stimulation required a high SNR (at least 80 dB) and a minimum of ten electrodes [3]. This number can quickly increase within in-brain stimulation (about 192). Using an IA per electrode, the silicon area grows accordingly. Thus, a solution to overcome this drawback is using a unique IA with larger bandwidth, associating a temporal multiplexing method. For example, neural stimulation using few hundreds of few-kHz channels each one [17], leads to a bandwidth of few MHz for a single IA.

3. VOLTAGE- AND CURRENT-MODE IA BACKGROUND

The IA discussed in this work has been targeted for sensor instrumentation in bio-electronics. A conceptual system-level front-end includes: IA, analog signal processing blocs (filters, mixers), and analog-to-digital converter. Most of bio-sensors are designed to respond by a charge variation. Over-time this charges are integrated in parasitic capacitances inducing a bio-potential or a bio-impedance variation. Similarly, image sensors convert photon signals into charges. Thus, sensors are essentially source of charges that can be instrumented in voltage- or current-mode.

In voltage-mode, Hassan and Lee have presented a wide linear output range bio-potential amplifier in [9]. Pini and McCarthy have proposed a low-power bio-potential IA in [16] validating noise requirements. Zhao et al. have innovated in IAs for bio-impedance spectroscopy in [21], optimizing to a total equivalent input noise reduction with low-power consumption.

In current-mode, Silverio et al. have proposed and measured a low-power IA based on a differential voltage current conveyor [18] suitable for bio-impedance spectroscopy. Widely explored in image sensors, current-mode IA have demonstrated high-speed, low-power consumption [1], and low-cost implementation of complex signal processing circuitry [15]. Mian et al. have demonstrated noise and speed trade-off in current-mode IA in [12]. However, these results are not targeted for bio-electronics applications. Focused to bio-electronics, Gupta and Gamad have presented an current-mode comparator in [7]. Besides, Haaheim and Constandinou have demonstrated a sub-1μW 8-bits SAR-ADC [8] for single-neuron spike recording.

In the state-of-the-art, current-mode IA design trade-off are not established and neither characteristics compromise addressed. Some essays [12, 5] have published analytical equations for characteristics estimation. The lack of design optimizations hinder bio-electronic instrumentation in current-mode, where low-power, high-speed, and complex signal processing could be explored. To address characteristics compromise, this work choses the dynamically regulated cascode current mirror (DRCCM) published in [5].

4. IA CURRENT-MODE OPTIMIZATION METHODOLOGY

In this section, a current-mode IA is considered and analytic expressions are carried through a low-power high-speed design optimization. Considering the DRCCM of Figure 1, the expression of current gain is

$$A_i = \frac{I_O}{I_{IN}} = \frac{W_{N2}/L_{N2}}{W_{N1}/L_{N1}} \frac{1+\lambda V_{DS_{N2}}}{1+\lambda V_{DS_{N1}}}, \quad (1)$$

where W_i/L_i are the aspect-ration of the transistor i and λ models the channel length modulation. In order to cancel λ-effect, N3 transistor is biased with I_B to obtain $V_{GS_{N3}} = V_{DS_{N1}}$. Thus, $V_{DS_{N1}}$ variations due to a time-variant I_{IN} are reflected in $V_{DS_{N2}}$ variation, guaranteeing a dynamical regulation of the cascode current mirror. In steady-state regime, a high linearity is achieved with a power consumption of

$$P_{bias} = 2 \cdot I_B \cdot V_{DD}. \quad (2)$$

4.1 DRCCM Characteristics Analysis

To achieve low-power, DRCCM bias current should be minimum which degrades performance in terms of linearity and gain. A high gain-bandwidth product and linearity with a minimum noise, area and power consumption is achievable under a considered compromise. To address these design trade-offs, aforementioned DRCCM characteristics are analyzed.

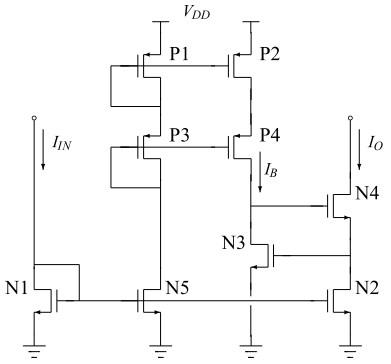

Figure 1: Dynamic regulated cascode current mirror (DRCCM): illustration [5].

Noise. DRCCM input noise current is obtained using

$$I_{n,in}^2 = \frac{I_{n,N}^2 + I_{n,P}^2}{A_i}, \text{ where} \tag{3}$$

$$I_{n,N}^2 = I_{N2}^2 + I_{N4}^2 + \frac{gm_{N2}^2}{gm_{N1}^2} I_{N1}^2 + \frac{gm_{N2}^2}{gm_{N5}^2} I_{N5}^2 + \frac{gm_{N4}^2 r_{o3}^2 I_{N3}^2}{r_{o2}(gm_{N4} + 1/r_{o4}) + 1}, \text{ and} \tag{4}$$

$$I_{n,P}^2 = \frac{gm_{N4}^2 r_{o3}^2}{r_{o2}(gm_{N4} + 1/r_{o4}) + 1} \left(I_{P2}^2 + I_{P4}^2 + \frac{gm_{P2}^2}{gm_{P1}^2} I_{P1}^2 + \frac{gm_{P4}^2}{gm_{P3}^2} I_{P3}^2 \right). \tag{5}$$

$I_{n,N}^2$ is the noise power from N1-N5 transistors (see Equation (3)), and $I_{n,P}^2$ is the noise power from P1-P4 transistors. DRCCM noise analysis details have been published in [5]. DRCCM noise analysis shows that the most important noise source comes from N1 transistor flicker noise. Circuit noise is improved by and optimal choice of gm_1, which has consequences for high-speed operation. $I_{n,in}^2$ is integrated for the DRCCM bandwidth (BW). A maximum signal-to-noise (SNR) is established by

$$\text{SNR} = 10 \cdot \log \left(\frac{I_{IN_{max}}^2}{I_{n,in}^2 \cdot 0.5\pi BW} \right), \text{ where} \tag{6}$$

$I_{IN_{max}}$ is the maximum input current.

Gain-bandwidth product. DRCCM bandwidth is estimated using a method of open-circuit time constants. The dominant pole,

$$\omega_{P1} = \frac{gm_1}{C_{GS1} + C_{GS2} + C_{GS5}}, \tag{7}$$

is influenced by the transconductance (gm) of N1 and the input-node capacitance. ω_{P1} is strongly affected by N2 transistor sizing due to high-gain specification (i.e. larger C_{GS2}) . In order to analyze the intrinsic poles of the IA, the sensor is modeled by an equivalent-Norton current source with a non-capacitive output impedance. The secondary pole,

$$\omega_{P2} = \frac{gm_3}{C_{GS3}}, \tag{8}$$

is affected by N3 transistor sizing and high-linearity specification. The gain-bandwidth product (GBW) is analytically calculated using the DRCCM gain (see Equation (1)), neglecting the channel length modulation, and considering ω_{P1} (see Equation (7)) in a single-pole modeling. To maximize

$$GBW = A_i \cdot BW = \frac{3K}{C_{ox}} \frac{V_{ov}}{L^2}, \tag{9}$$

DRCCM optimization should consider a minimum length (L) for N transistors, which would also minimize the area consumption. In Equation (9), K is the process transconductance parameter and C_{ox} the oxide capacitance. The DRCCM overdrive voltage ($V_{ov} = V_{GS_{N1}} - V_{th}$) is imposed by I_{IN} dynamic range, since N1 is diode-connected. Maximum GBW design choice influence noise performance, which is subjected to transistor sizing.

Linearity. A current mirror linearity is evaluated by its total harmonic distortion (THD). E. Bruun [2] has presented analytical expressions for current mirrors THD. Ferreira et al. [5] has highlighted DRCCM THD using analytical and simulated methods. This work focuses on linearity optimization for a maximum GBW. According to Equation (9), technology L_{min} should be considered to N transistors. Thus, non-linearity issues will take place in short-channel N1-N5 current mirror due to channel length modulation. If $V_{DS_{N5}} \neq V_{DS_{N1}}$, dynamic regulation may fail degrading DRCCM linearity. To consider this effect in design trade-off, current mirroring error in bias circuit is modeled as

$$\frac{I_B}{I_{IN}} = (1 + w_N) \frac{1 + \lambda V_{DS,N5}}{1 + \lambda V_{DS,N1}}, \tag{10}$$

where $1 + w_N$ is proportional to the regulator amplifier gain. If a large enough gain is chosen to the regulator amplifier then $V_{DS_{N1}} \approx V_{DS_{N2}}$, improving DRCCM linearity. However, a gain increase implies in power consumption increase. An optimum w_N is able to minimize power consumption constrained to a THD specification. Using a cascode topology, P1-P2 current-mirror guarantees a negligible impact in linearity if sized with $L > 4 \cdot L_{min}$.

4.2 Low-power High-speed Optimization

For implantable bio-electronic applications, low-power is mandatory. To achieve low-power and high-performance devices, the presented design optimization maximizes speed (improving DRCCM's GBW), minimizes power consumption constrained to a linearity target (evaluated by IA's THD). DRCCM characteristics analysis reveal that: (a) area is minimal for a maximum GBW (see Equation (9)); (b) linearity is improved in spent of power consumption (see Equation (10)). In this case, a cost function (CF) is

$$CF = \varepsilon \cdot \frac{2I_B}{I_{IN}}, \tag{11}$$

where ε is the DRCCM gain error due to non-linearity, being

$$\varepsilon = \frac{I_O - A_i I_{IN}}{A_i I_{IN}}. \tag{12}$$

A_i is the current gain specification, and so $A_i I_{IN}$ the expected value of I_O. DRCCM design optimization is stated: (a) find w_N for a minimum CF, (b) constrained to power consumption, gain, speed, noise, and linearity. DRCCM constraints are $P_{bias} < 30\ \mu$W, $A_i = 100$, $GBW \geq 100$ MHz, SNR ≥ 62 dB, and THD ≤ -40 dB. In comparison to previous DRCCM design [5], power consumption is ten times smaller for a ten times bigger gain. DRCCM BW is also improved. DRCCM linearity and noise are in agreement to Ferreira's work.

A simulation-based design optimization is carried out using Cadence Spectre Circuit Simulator with CMOS 180 nm technology;

and it has been executed in an Intel Core i7-3770 3.1 GHz. To determine optimal w_N, parametric-sweep DC simulation was settled in: $I_{IN} = 120$ nA, 27 ^{o}C, and $V_{DD} = 1.8$ V. While N1 is minimum sized, N2 is A_i times bigger than N1. N4 transistor has equal sizing as N2 to save area. P1 and P2 transistors aspect ratio (W/L) is two, while P3 and P4 cascode aspect ratio is eight. PMOS current mirror uses a conservative length of 1 μm. Since P current mirror has a unity gain, N3 and N5 transistors have the same sizing from Equation (10). An optimum sizing is found after 300-points simulation; the execution time lasted about five minutes.

Figure 2 reveals a minimum CF of $4.7 \cdot 10^{-3}$ when $w_N \approx 3$. At optimum, bias has $2 \cdot I_B = 122$ nA for a $\varepsilon = 0.47\%$. Both estimated characteristics minimize power and validate linearity requirements. Since N1 is minimum sized, area is minimized and speed is maximized. Further criteria will be confirmed by specific simulation results depicted in Section 5. IA optimal sizing is presented in Table 1, and IA final layout is illustrated in Figure 3. The DRCCM area consumption is 25 μm per 41 μm.

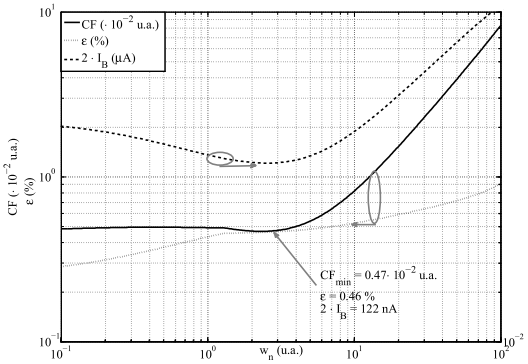

Figure 2: Simulation-based optimization result: $I_{IN} = 120$ nA, and $V_{DD} = 1.8$ V.

Table 1: IA optimum design: transistors sizing.

Transistor	W (μm)	L (μm)
N_1	0.22	0.18
N_2	22	0.18
N_4	22	0.18
N_3, N_5	0.88	0.18
P_1, P_2	2.0	1.0
P_3, P_4	8.0	1.0

5. POST-LAYOUT SIMULATION RESULTS

In accordance to a single-objective with multi-constraints, the optimal designed current-mode IA has its performance post-layout simulated. Constrained to THD ≤ -40 dB, IA spurious-free dynamic range (SFDR) is estimated at 37 ^{o}C aiming in-vivo bio-electronics. Figure 4 highlights a SFDR of 47 dB achieving a maximum $P_{bias} = 2.5$ μW. Post-layout result confirms optimal design in terms of linearity and power consumption.

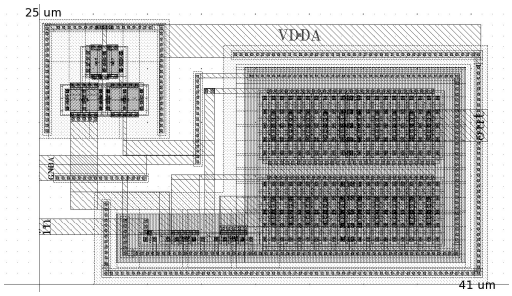

Figure 3: IA layout according optimized sizing: area is 25 μm per 41 μm.

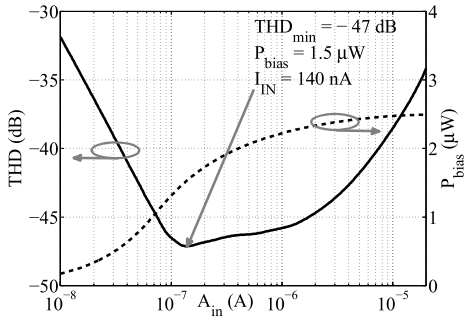

Figure 4: IA post-layout transient simulation: linearity and power consumption characteristics at 37 ^{o}C ($I_{IN} = 140$ nA sine-wave at 10 kHz).

IA's gain and noise characteristics are post-layout simulated at 37 ^{o}C. Figure 5 validates gain, speed and noise characteristics. IA input noise $I^2_{n,in}$ integrated in the noise frequency band is $I_{n,in} = 1.98$ nA. IA noise characteristic points out a SNR = 80.0 dB at $I_{IN_{max}}$ (see Fig. 4). IA presents a GBW= 459.8 MHz, being $A_i = 40$ dB.

Post-layout IA performance under temperature variation is estimated for military range (from -55 ^{o}C to 125 ^{o}C) at $I_{IN} = 7$ μA (worst-case input current regarding linearity constraint, see Fig. 4). To evaluate performance losses under temperature variation, IA characteristics are normalized to bio-electronics in-vivo temperature reference as Γ/Γ_{37^oC}. Figure 6 shows a worst-case gain of 39.2 dB and worst-case noise of 2 nA. Linearity and speed are degraded in high temperatures as depicted in Figure 6. In low temperature, linearity and speed are improved, but gain and noise remains close to typical value. As long temperature increases power consumption increases, achieving a maximum of 5.5 μW.

Post-layout IA performance under process variability is verified by a 1k-points Monte Carlo simulation at $I_{IN} = 7$ μA (worst-case input current regarding linearity constraint, see Fig. 4). IA linearity presents THD $= -33.67$ dB and $\sigma_{\text{THD}} = 7.7$ dB. IA power consumption shows $P_{bias} = 2.47$ μ W and $\sigma_{P_{bias}} = 0.32$ μW. IA gain presents $A_i = 39.27$ dB and $\sigma_{A_i} = 1.25$ dB. IA gain-bandwidth product presents GBW = 460 MHz and $\sigma_{\text{GBW}} = 203$ MHz. IA input noise $I^2_{n,in}$ integrated in the noise frequency band presents $I_{n,in} = 1.945$ nA and $\sigma_{I_{n,in}} = 0.048$ nA.

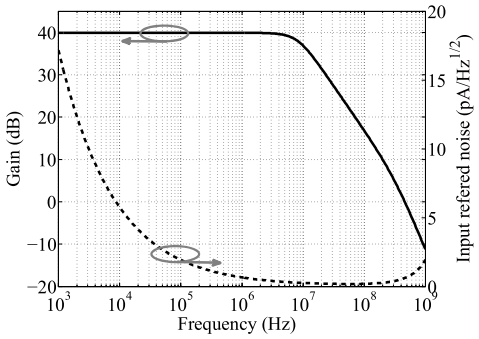

Figure 5: IA post-layout AC simulation: gain and noise characteristics at 37 ^{o}C.

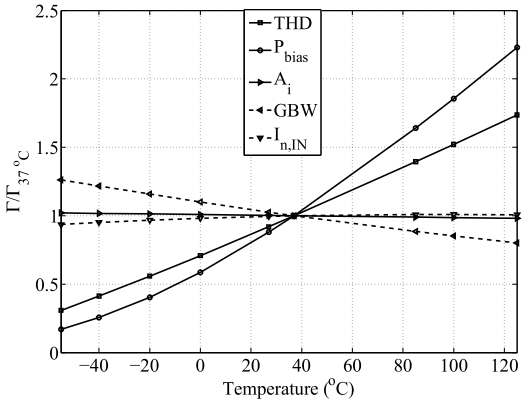

Figure 6: IA post-layout performance under temperature variation.

Table 2 compares post-layout simulated results of the proposed current-mode IA with the state-of-the-art of IAs, including current-mode and voltage-mode examples. The proposed IA has remarkable low-power consumption with an increased speed in comparison to the literature. Linearity and gain characteristics are in agreement with the state-of-the-art. IA noise characteristic is also improved to more than twelve effective bits. Post-layout simulated performance ensures bio-electronics in-vivo application requirements.

6. CONCLUSIONS

This paper shows a single-objective with multi-constraint optimization of a current-mode IA suitable for bio-electronic applications. Analytical expressions were demonstrated for a DRCCM. This work proposed a cost function joining gain error due to non-linearity and power efficiency. Constrained to area minimization, signal-to-noise ratio and speed increase, N1-N5 stage was sized in minimum length ($L = L_{min}$). Current-mode IA was implemented using CMOS 180 nm technology. Post-layout simulations reported: power consumption of 1.5 μW, gain of 40 dB, GBW of 459.8 MHz, SNR of 80 dB, and THD of -47 dB. According to published current- and voltage-mode IAs, the optimal IA designed in this paper has competitive performance exploring low-power, low-noise and high-speed. Therefore, this work has established a design trade-off in current-mode addressing characteristics compromise. Forthcoming improvements in DRCCM topology could be: complementary mirror for differential-mode signals, frequency peaking, and feedback.

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Table 2: Performance comparison with respect to previously reported current-mode and voltage-mode IAs.

	This work	[18]	[9]	[5]	[16]	[21]
Power (μW)	1.5	290	18.5	30.0	1.5	420
Gain (dB)	39.9	62.8	46	20.0	39.0	20.0
GBW (MHz)	459.8	1.44	1.00	2.3	0.03	10.0
SNR (dB)	80.0	32.6	69.0	79.0	64.0	65.3
THD (dB)	-47.0	-41.8	-68.0	-70.0	-32.0	N/A
Mode	current	current	voltage	voltage	current	voltage
Technology	180 nm	0.35 μm	0.35 μm	0.35 μm	0.35 μm	0.35 μm

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