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Abstract:	There are currently two competing transconductance-to-drain current based noise analysis techniques in the literature: one based on the thermal coefficient and device corner frequency and another based on the normalized noise power. This letter presents a unified explanation of transconductance-to-drain current based noise analysis. Analytical expressions are presented to clearly show the dependence of thermal noise coefficient and device corner frequency on the transconductance-to-drain current ratio of a transistor, as well as their relationship to the normalized noise power technique. Finally, this letter highlights a potential advantage of the thermal noise coefficient and device corner frequency technique in circuit noise optimization.
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A Unified Explanation of g_m/I_D Based Noise Analysis

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There are currently two competing transconductance-to-drain current (g_m/I_D) based noise analysis techniques in the literature: one based on the thermal coefficient (γ) and device corner frequency (f_{co}) and another based on the normalized noise power. This letter presents a unified explanation of transconductance-to-drain current (g_m/I_D) based noise analysis. Analytical expressions are presented to clearly show the dependence of thermal noise coefficient (γ) and device corner frequency (f_{co}) on the g_m/I_D of a transistor, as well as their relationship to the normalized noise power technique. Finally, this letter highlights a potential advantage of the thermal noise coefficient (γ) and device corner frequency (f_{co}) technique in circuit noise optimization.

Keywords: noise analysis; g_m/I_D; design methodology.

1. Introduction

Nanoscale Metal Oxide Field Effect Transistor (MOSFET) circuit design is driven by power consumption constraints. The minimal power consumption is achieved when transistors are operated in the weak inversion region.[1] In the absence of a model suitable for back of envelope calculations, designers often explore design space using arduous circuit simulations. Over-reliance on circuit simulator can be problematic, potentially luring inexperienced designers to dive into simulation without understanding basic trade-offs in a properly optimized circuits.

In 1996, Silveira *et al.* proposed a powerful transconductance-to-drain current (g_m/I_D) technique to help designers size up transistors quickly.[1] The so called "g_m/I_D design approach" was originally developed to calculate parameters such as small signal gain and bandwidth,[1] and later extended to noise.[2] In the formulation that was published by Ou[2] in 2011, bias dependent thermal noise coefficient (γ) and

device noise corner frequency (f_{co}) were introduced. A procedure for determining γ and f_{co} from simulation was described. In 2012, Alvarez *et al.* published an alternative formulation of g_m/I_D based noise analysis which used normalized noise power.[3,4] The normalized power formulation was first confirmed using simple noise equations,[3] and later with BSIM noise equations.[4]

What remains unknown at the present are: first, a unified explanation of two seemingly unrelated g_m/I_D noise analysis techniques presented by Ou[2] and Alvarez *et al.*,[3] second, a physical explanation that clearly shows the dependence of γ and f_{co} on g_m/I_D,[2] and third, circumstances under which each technique can be used.

In this letter, starting from basic principles in device physics, we provide a unified explanation of g_m/I_D noise analysis. We provide analytical expressions to clearly show the g_m/I_D dependence of f_{co} and γ, and in doing so addressing the concern raised by Alvarez *et al.*[3] Finally, we provide insights on the application of each noise analysis technique.

2. Theory

The g_m/I_D principle is applicable to parameters which are independent of the width (W) of a transistor. Figure 1 shows a transistor with a transconductance (g_m), a drain-to-source conductance g_{ds}, and a current (I_D) biased at a gate-to-source voltage (V_{GS}) and a drain-to-source (V_{DS}). If an identical device is connected in parallel so both devices are biased at the same V_{GS} and V_{DS}, both devices have the same g_m, g_{ds} and the same I_D. Since the devices are connected in parallel, they can be treated as one device with an aspect ratio of $2W/L$. The effective transconductance over current ratio is g_m/I_D for both the merged device and the stand alone device because g_m and I_D are doubled. The drain-to-source conductance is also doubled for the merged device. Therefore the intrinsic gain (g_m/g_{ds}) is identical for both the stand alone device and the merged device. As long as transistors are biased at the same g_m/I_D, they will have the same g_m/g_{ds}. This observation is true for any two parameters whose ratio depend solely on the g_m/I_D and not on the width of a transistor. Once a transistor of a given W is characterized over a range of g_m/I_D, the g_m/I_D based parameters can be generalized to a transistor of an arbitrary W, *assuming that L remains constant.* The g_m/I_D methodology will hold as long as the parameter of interest scales with W.

3. g_m/I_D Dependent Thermal Noise

We present in this section a unified explanation of g_m/I_D based thermal noise analysis techniques presented by Ou[2] and Alvarez *et al.*.[3] Starting from basic device noise equation, we show the dependence of γ on g_m/I_D. We conclude the section by showing the link between the method proposed by Ou[2] and Alvarez *et al.*.[3]

The MOSFET noise arises from thermal noise fluctuations in the channel. It can be shown that the thermal noise at the drain terminal is,[5]

$$\overline{i_{n,id}^2} = 4kT\gamma g_{do}, \tag{1}$$

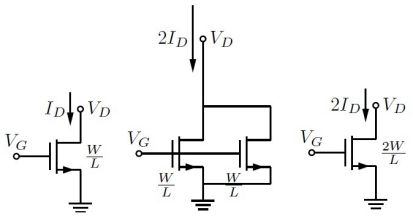

Fig. 1. Transistors biased at the same g_m/I_D.

where k is the Boltzmann constant, T is the temperature, g_{do} is the drain conductance at zero drain-to-source voltage, and γ is the bias-dependent noise parameter. According to this model, the γ approaches 1 when the drain-to-source voltage (V_{DS}) approaches zero and decreases to 2/3 when the device enters the saturation regime. The saturation value of $\gamma = 2/3$ is valid for long-channel MOS devices built on lightly doped substrates. Early studies have reported γ values between 2/3 and 4,[6] but recent studies have shown that by accounting for parasitic resistances, γ is approximately 2/3 for channel lengths equal or greater than 100 nm.[7]

At a more fundamental level, the thermal noise ($\overline{i_{n,id}^2}$) at the drain terminal of a MOS transistor is

$$\overline{i_{n,id}^2} = 4kT\frac{\mu}{L^2}(-Q_I), \tag{2}$$

where Q_I is the total inversion layer charge underneath the gate oxide, L is the length of the transistor, and μ is the mobility. Equation 2 is valid for all regions of operation[5]. The total inversion layer charge (Q_I) is obtained by integrating the inversion charge per unit length ($Q_I'(x)$) over the length of the channel,

$$Q_I = \int_0^L Q_I'(x)W\mathrm{d}x, \tag{3}$$

where $Q_I'(x)$ is a function of V_{GS} and V_{DS}, as well as V_{SB}, and consequently a function of transistor's g_m/I_D. Since Q_I is proportional to W (see Eq. (3)), $\overline{i_{n,id}^2}$ is proportional to W according Eq. (2). Since g_m is proportional to W, $\overline{i_{n,id}^2}/g_m$ becomes independent of W. Equation (2) also shows that $\overline{i_{n,id}^2}$ is inversely proportional to L^2. Even though the transconductance of a transistor also depends on the L, it is not inversely proportional to L^2. Therefore, $\overline{i_{n,id}^2}/g_m$ remains a function of L. Once $\overline{i_{n,id}^2}/g_m$ of a transistor for a given (W/L) is characterized over a range of g_m/I_D; $\overline{i_{n,id}^2}/g_m$ of the transistor can be generalized to a transistor of arbitrary W as long as L and the g_m/I_D are constant. This width-independent property is the crucial link to the g_m/I_D design methodology described earlier.

The $\overline{i_{n,id}^2}/g_m$ is directly related to γ of a transistor since the thermal noise of an MOS transistor is modeled by a current source ($\overline{i_{n,id}^2}$) connected between the drain

terminal and the source terminal with a spectral density of

$$\overline{i_{n,id}^2} = 4kT\gamma g_m, \tag{4}$$

where k is the Boltzmann constant, and T is the temperature.

If we divide $\overline{i_{n,id}^2}$ by $4kTg_m$, we obtain a closed expression for γ.

$$\frac{\overline{i_{n,id}^2}}{g_m} = 4kT\gamma, \tag{5}$$

The right side of the Eq.(5) represents the g_m/I_D dependent γ used in the noise analysis technique proposed by Ou.[2] *If we divide* $\overline{i_{n,id}^2}$ *by* I_D*, instead of* g_m*, we have the normalized noise power formulation proposed by Alvarez et al.*[3] *Similar to* $\overline{i_{n,id}^2}/g_m$*,* $\overline{i_{n,id}^2}/I_D$ *is also width-independent since both* g_m *and* I_D *are proportional to* W*.*

Figure 2 illustrates γ as a function of g_m/I_D for an NMOS transistor with a $V_{DS} = 0.6$V,$V_{SB} = 0.2$V, a bias current of 10 μA, and a length of 0.18μm.[2] The $\overline{i_{n,id}^2}$ is estimated by noise simulation in Cadence Spectre with transistors modeled using BSIM 4.4. The unified physical model is used to model the flicker noise (`fnoimod=1`) and the charge based model is used to model thermal noise (`toimod=0`). g_m is determined by DC simulation. No curve fitting technique is used in our analysis (see Fig. 2).

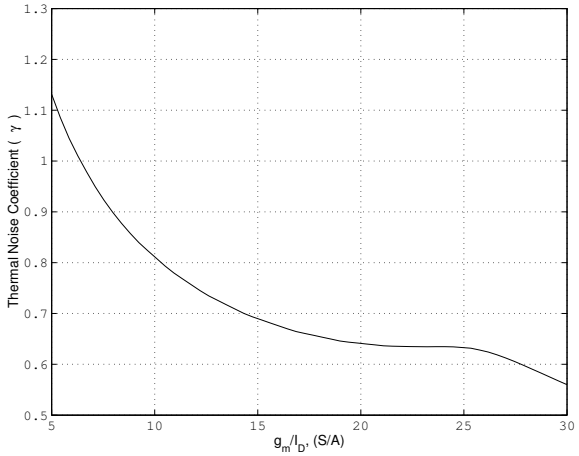

Fig. 2. Simulated thermal noise coefficient (γ) of NMOS transistor with a $V_{DS} = 0.6$V,$V_{SB} = 0.2$V, a bias current of 10 μA, and a length of 0.18μm.

4. Flicker Noise

Since MOSFETs are surface-conduction devices, flicker noise is important at low frequencies. The flicker noise at the drain terminal of a transistor is

$$\overline{i_{nd,fn}^2} = \frac{K_f}{C_{ox}WL}\frac{g_m^2}{f}, \tag{6}$$

where K_f is a process dependent parameter, C_{ox} is the oxide capacitance, W is the width and L is the length. If we divide both sides of Eqn.(6) by g_m, we have

$$\frac{\overline{i_{nd,fn}^2}}{g_m} = \frac{K_f}{C_{ox}WL}\frac{g_m}{f}, \tag{7}$$

We see that $\overline{i_{nd,fn}^2}/g_m$ is also width-independent since g_m is proportional to W. Both Eqn. (7) and Eqn. (5) are instances of normalized noise power proposed by Alvarez et al..[3]

Rather than introducing an all inclusive g_m/I_D dependent normalized noise parameter as was done by Alvarez *et al.*,[3] the g_m/I_D dependent flicker noise was separated from the g_m/I_D dependent thermal noise in order to identify transistor specific noise bottleneck at the circuit level.[2] Device noise corner frequency was chosen to represent the flicker noise. At the device noise corner frequency (f_{co}), the thermal noise is equal to the flicker noise (i.e. $\overline{i_{nd,th}^2} = \overline{i_{nd,fn}^2}$). Setting Eq.(4) equal to Eq.(6), we have

$$4kT\gamma g_m = \frac{K_f}{C_{ox}WL}\frac{g_m^2}{f_{co}} \tag{8}$$

Using Eqn. (8), *f_{co} can be solved in order to explicitly show the dependence on* g_m/I_D and current density (I_D/W), which also depends on g_m/I_D.

$$f_{co} = \frac{K_f}{C_{ox}L}\frac{g_m}{I_D}\frac{I_D}{W}\frac{1}{4KT\gamma} \tag{9}$$

We wish to point that K_f is a geometry dependent coefficient.[8] At $f = f_{co}$, the Eq.(6) becomes

$$\overline{i_{nd,fn}^2} = \frac{K_f}{C_{ox}WL}\frac{g_m^2}{f_{co}} = \overline{i_{nd,th}^2}, \tag{10}$$

Multiplying Eq.(10) by f_{co}, we get,

$$\overline{i_{nd,th}^2}f_{co} = \frac{K_f}{C_{ox}WL}g_m^2. \tag{11}$$

Using Eq.(11) and Eq.(6), we have a simple equation that relates thermal noise current to flicker noise current,

$$\overline{i_{nd,fn}^2} = \overline{i_{nd,th}^2}\frac{f_{co}}{f}. \tag{12}$$

We showed in that similar to γ, f_{co} is also a function of g_m/I_D, as well as V_{SB}, and L.[2] Figure 3 shows the dependence of f_{co} as a function of length at $V_{DS} = 0.2V$ and $V_{SB} = 0.2V$.

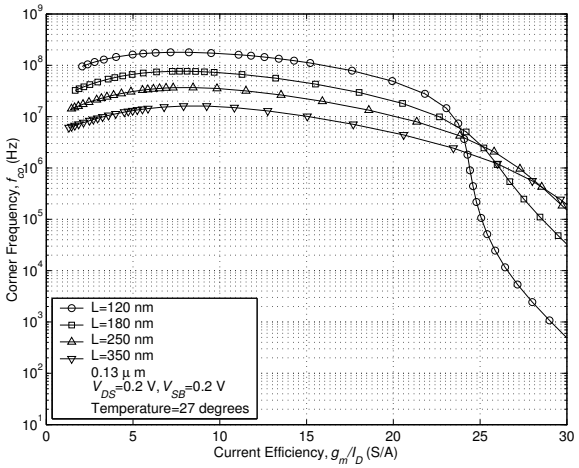

Fig. 3. Corner frequency as a function of device length and current efficiency.

The total noise at the output of the drain terminal of an MOS transistor includes both the thermal noise as well as flicker noise.

$$\overline{i_{nd}^2} = \overline{i_{nd,th}^2} + \overline{i_{nd,fn}^2} = \overline{i_{nd,th}^2}(1 + \frac{f_{co}}{f}). \tag{13}$$

We can gate-referred the drain noise current $\overline{i_{nd}^2}$ by dividing $\overline{i_{nd}^2}$ by g_m^2.

$$\overline{v_{ng}^2} = \frac{\overline{i_{nd,th}^2}}{g_m^2} = \frac{4kT\gamma}{\frac{g_m}{I_D} I_D}(1 + \frac{f_{co}}{f}). \tag{14}$$

Equation 14 shows that once I_D is fixed, the gate-referred noise $\overline{v_{ng}^2}$ depend on γ and f_{co}, both of which are also dependent on g_m/I_D. It was shown in [2] that the input-referred noise can be contributed to the gate-referred noise of each transistor, and therefore the γ and f_{co} of each transistor.

5. Applications

Both noise analysis techniques proposed by Ou[2] and by Alvarez *et al.*[3] can be applied to analyze noise (e.g. the folded-cascode amplifier[2] and the charge amplifier[4]). There are, however, two **additional** benefits of using γ and f_{co} approach in an analysis. *First*, by choosing the g_m/I_D of each transistor carefully, noise at the circuit level can be optimized by tracing the transistor-noise constraint at the circuit level (e.g. input-referred noise) to γ and f_{co} of each transistor in the schematic. *This unique ability to express noise as a fundamental quantity such as f_{co} facilitates noise analysis well as enhance designers' understanding of the fundamental noise limitation in a circuit. Second*, different from the normalized power approach, which expresses the sum of thermal and flicker noise as one parameter, *the γ and*

f_{co} approach keeps flicker noise separate from thermal noise, and thereby enabling thermal-noise/flicker-noise specific sizing optimization in circuits where one noise is more dominant than the other. For example, in biomedical applications, f_{co} is often larger than f, the first term in the parenthesis of Eqn. (14) can be neglected in the analysis in order to perform a flicker noise specific sizing optimization.

6. Conclusion

Starting from basic principles in device physics, this letter provides a unified explanation of g_m/I_D based noise analysis. Normalized noise power analysis was shown to be equivalent to the noise analysis based on γ and f_{co}.The analytical expressions in this letter clearly show the dependence of γ and f_{co} on the g_m/I_D of a transistor. The use of two noise parameters (γ and f_{co}) allows designers to trace the transistor-noise constraint at the circuit level to the noise parameters of each transistor and perform thermal noise/flicker noise specific sizing optimization.

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