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Tiny companion testchips for 56 Gbaud applications based on microring resonators



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Objective: To address 56G external I/Os issues

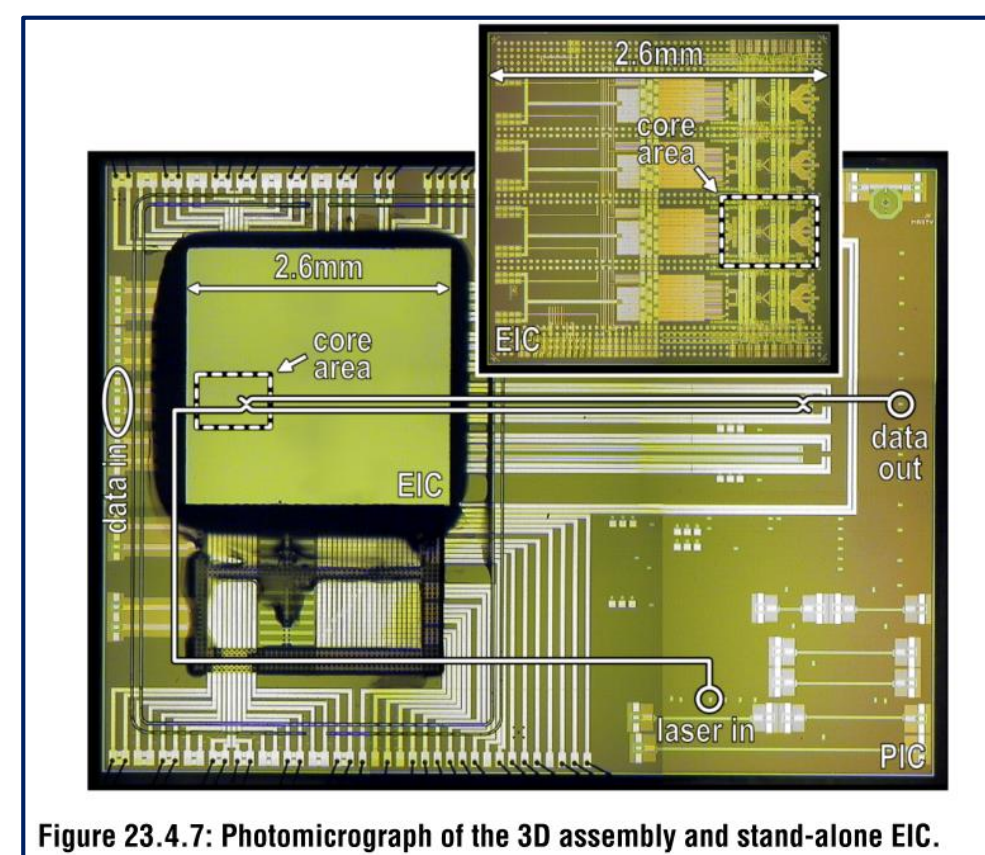
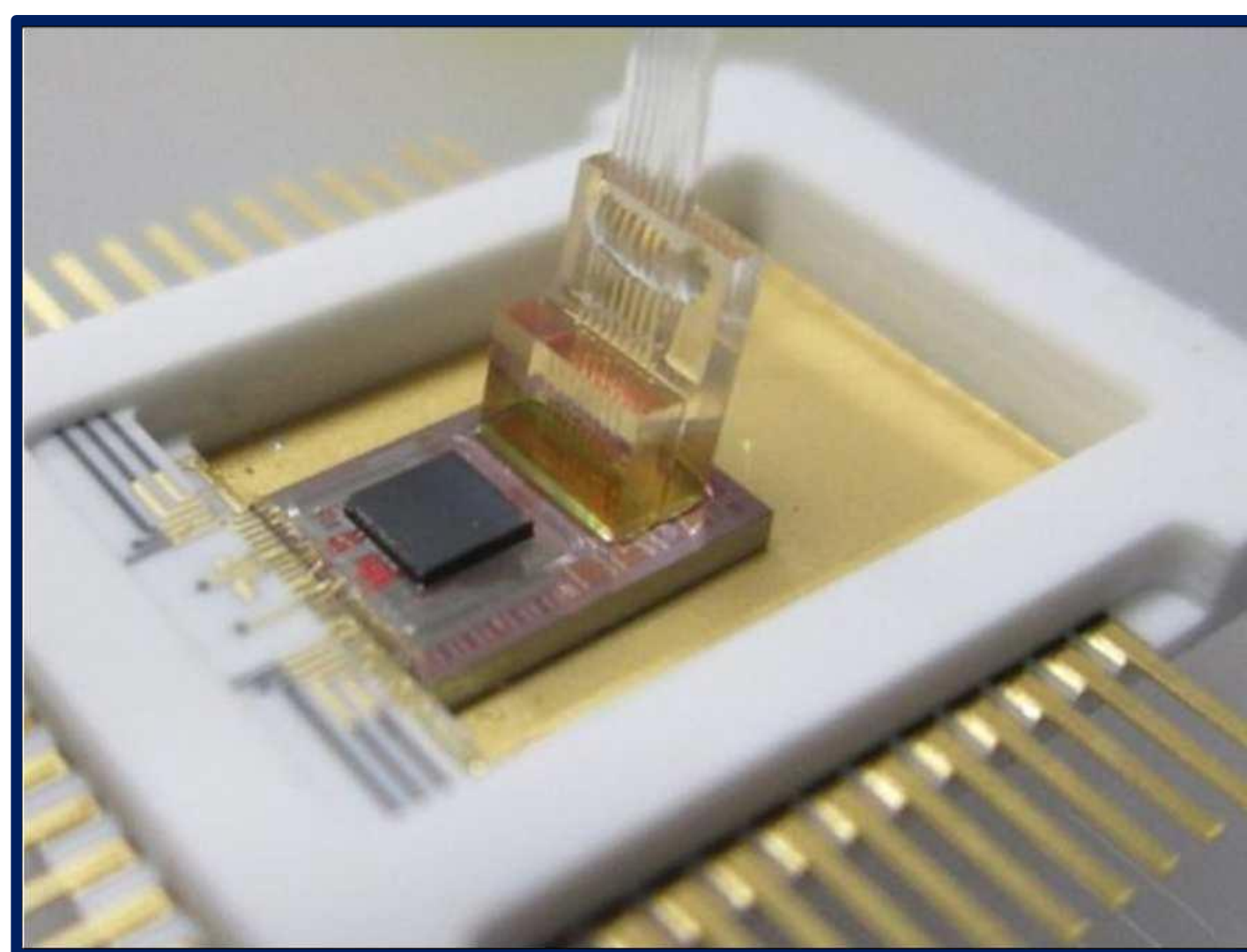
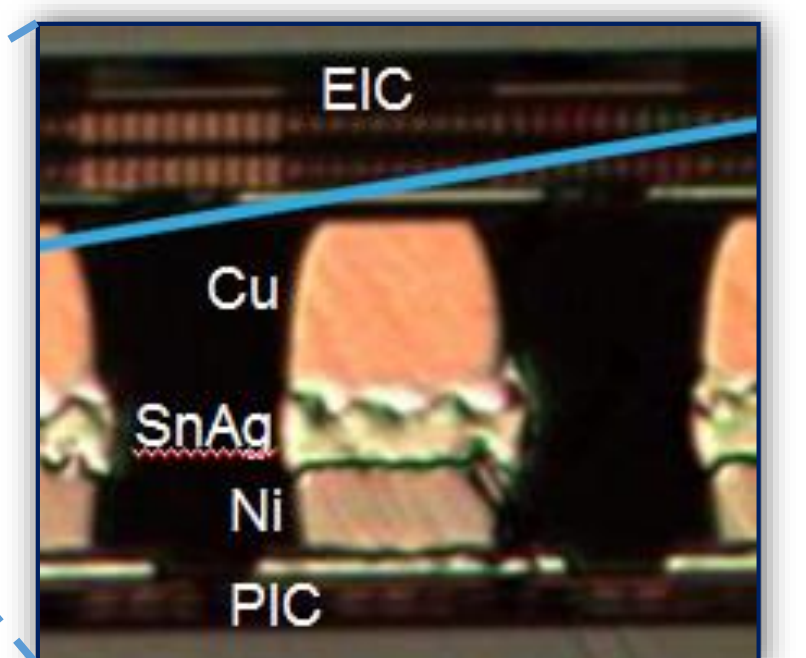
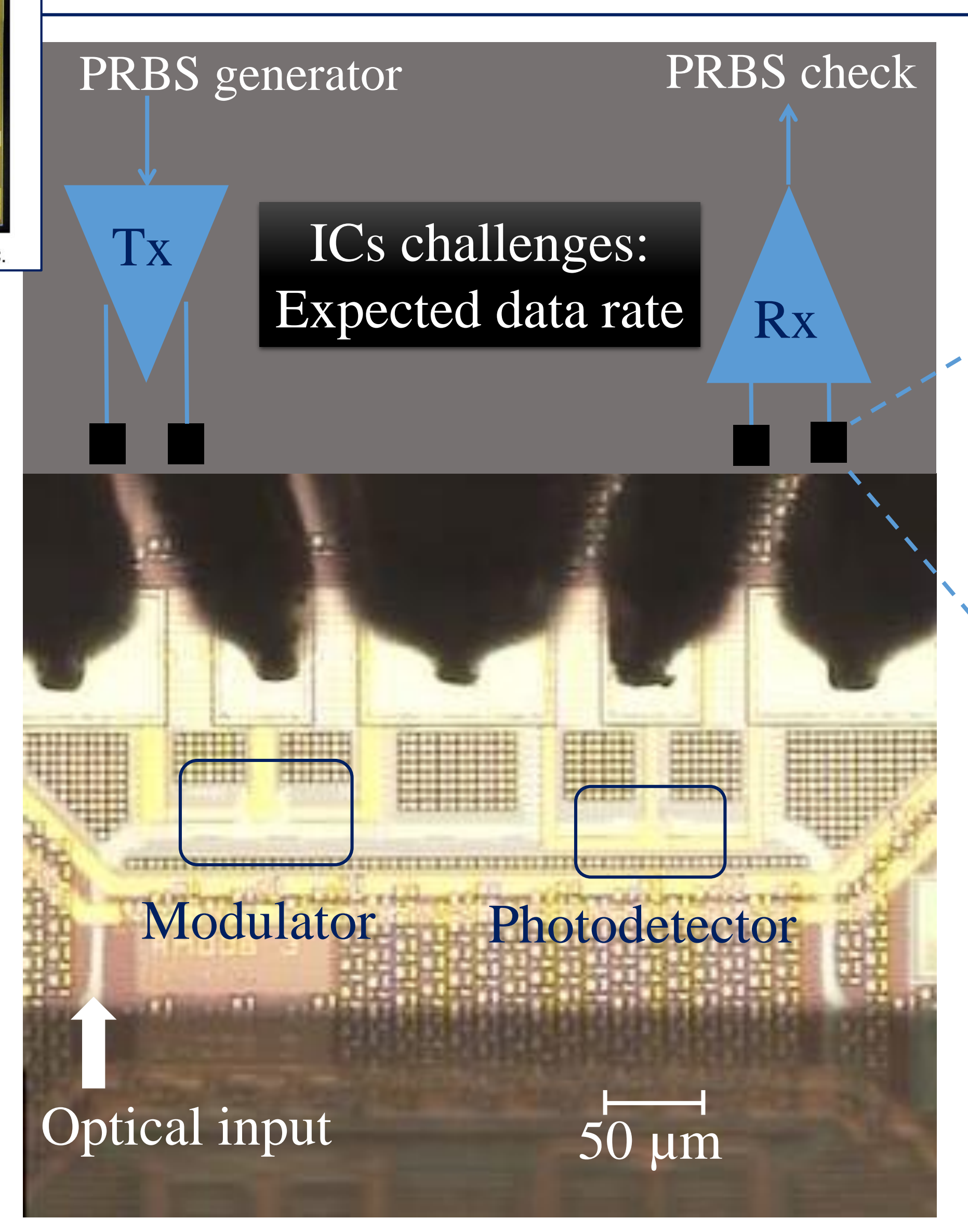


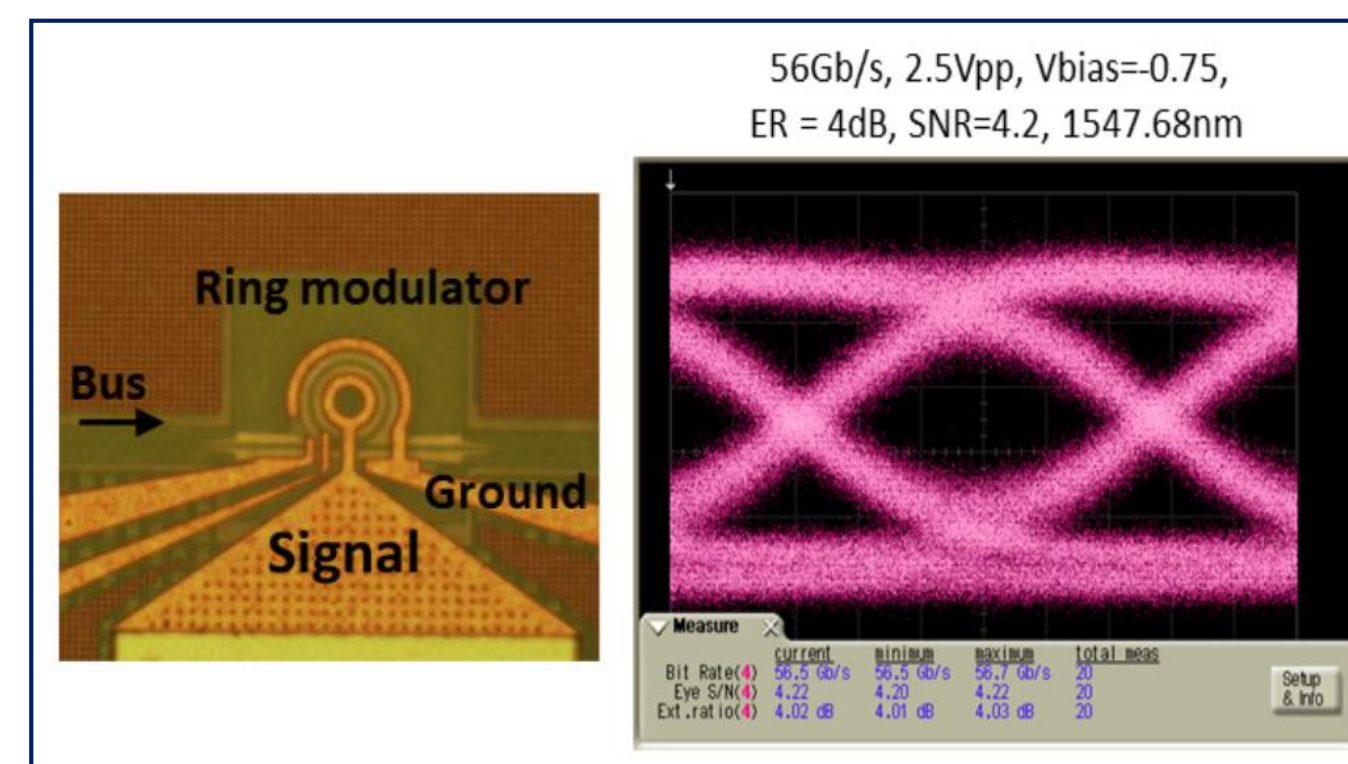
Figure 23.4.7: Photomicrograph of the 3D assembly and stand-alone EIC.

Driver + MZM demonstrated at 56 Gb/s
STMicroelectronics, "A 56 Gb/s 300mW Silicon-photonics transmitter in 3D-integrated PIC25G and 55nm BiCMOS technologies", ISSCC 2016



Fine pitch copper pillar flip-chip for connection between photonic interposer and electronic chip

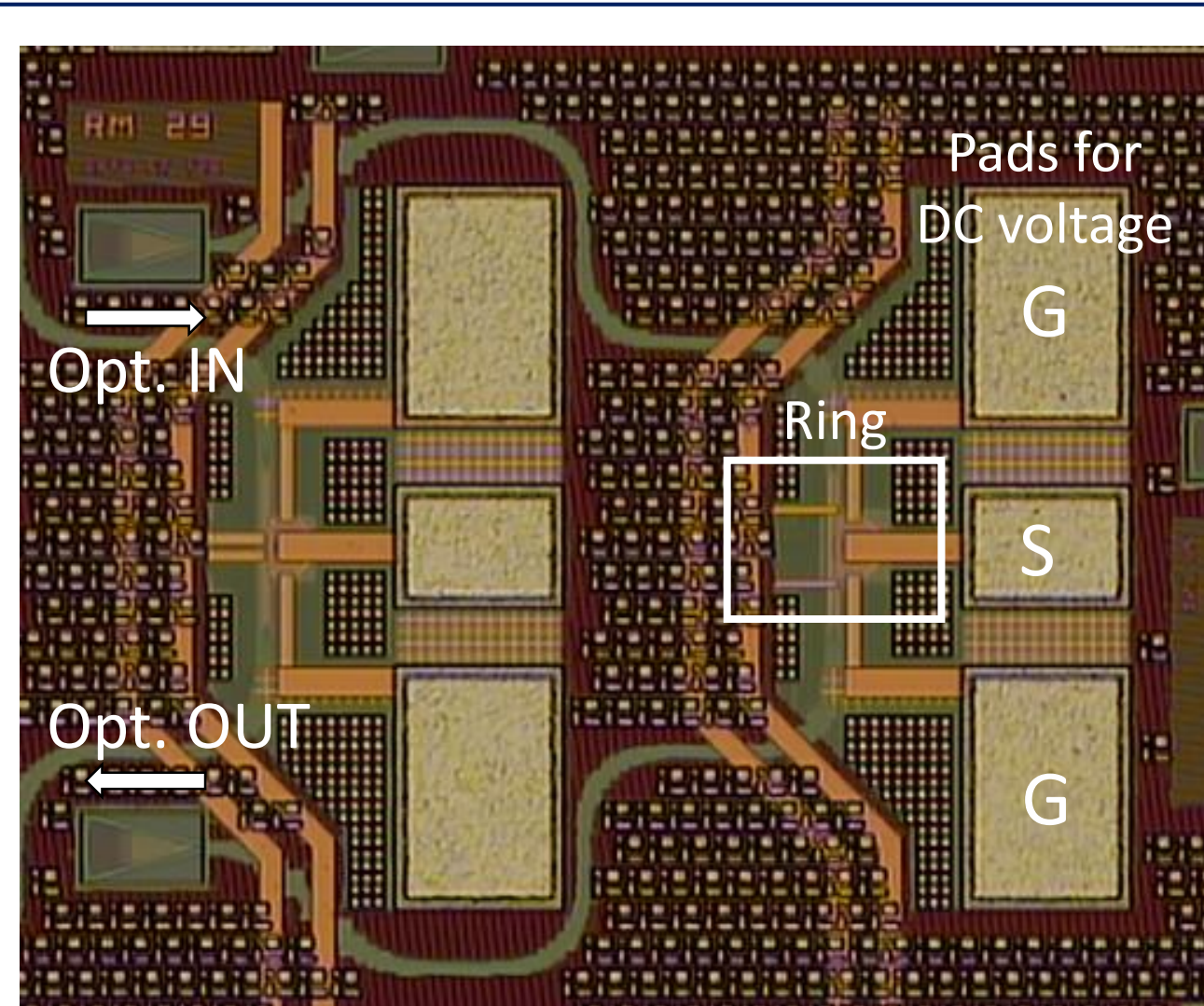
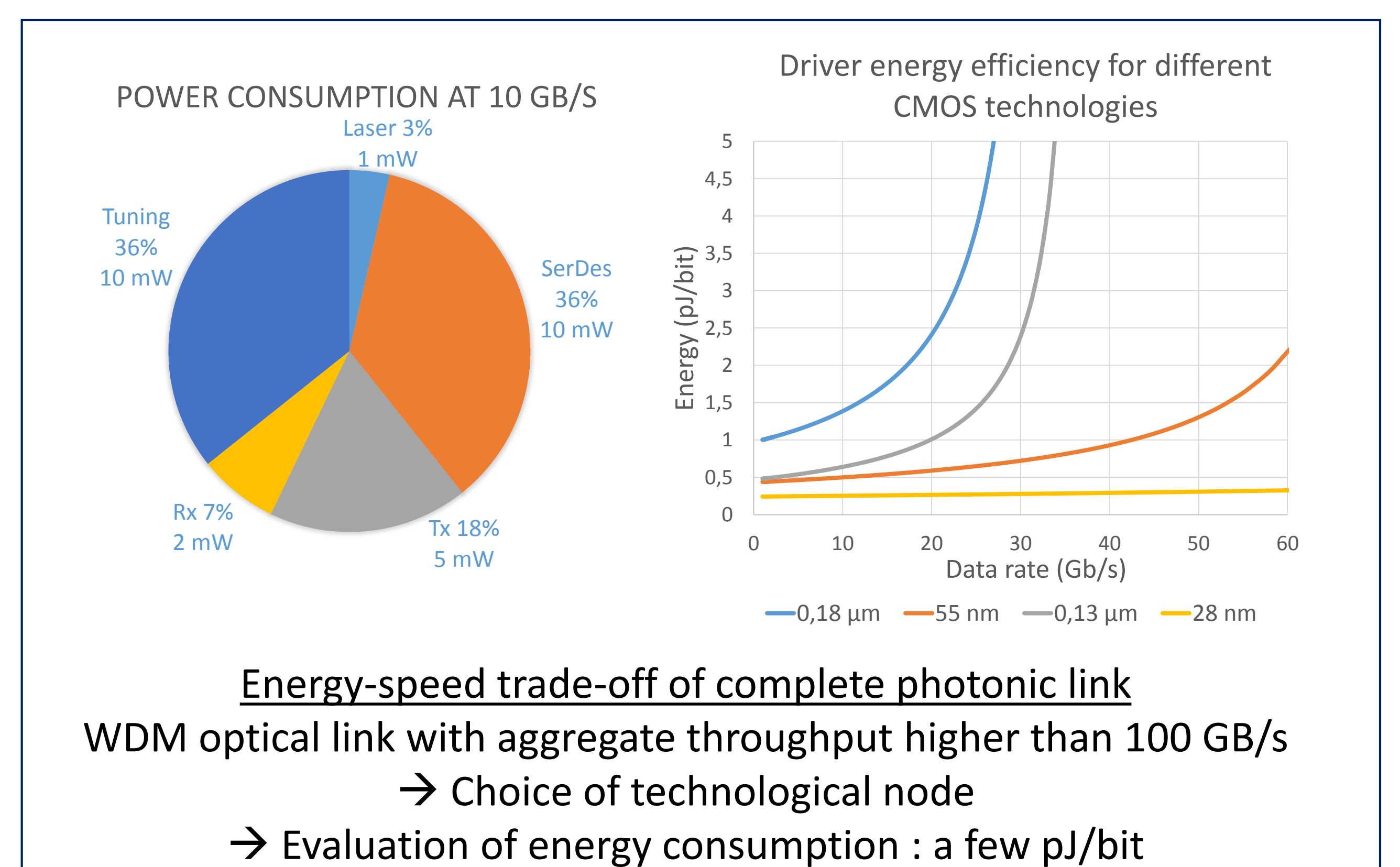
- Purpose: IP core for customer at packaging level
- Tiny & configurable companion testchips
- 3D assembly validation
- Passive & active components of PIC25G + BiCMOS/CMOS



Ring modulator demonstrated at 56 Gb/s
IMEC, "56 Gb/s Ring modulator on 300nm silicon photonics platform", ECOC 2015

Thesis schedule: Dynamic testchip at wafer-level with 3D assembly

- CMOS driver in B55 at 10 - 25 Gbps
 - Optimal data rate for on-chip links (most energy efficient solution)
 - Learning phase for future 56G driver
- Ring resonator modeling
 - Model required for electro-optical co-simulations
 - Impact of 3D assembly on static characteristics
- Qualification testchips based on microring resonators for 56 Gbps applications
 - Demonstration of 3D integration at 25 Gbps
 - Circuit study : Driver @ 56G
 - Device study : Ring @ 56G



PN ring resonator, 8μm radius

Measurement of static and dynamic characteristics
→ Transmission spectrum: modeling of plasma dispersion effect and self-heating due to TPA & FCA
→ Small-signal model: RC values extraction from S-parameters

