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# Capacitance characterization of GaP/n-Si structures grown by PE-ALD

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**Abstract**. Thin layers of μc-GaP and a-GaP grown on n- type silicon wafers by plasma-enhanced atomic layer deposition at 380 °C are characterized by space charge capacitance techniques, C-V profiling and deep level transient spectroscopy (DLTS). Two defect levels with activation energies of 0.30 eV and 0.80 eV were detected by DLTS in the μc-GaP/n-Si structure. Measurements performed on Schottky barriers formed on n-Si after selective etching of the GaP layer did not reveal any defect level meaning that the observed defects in the μc-GaP/n-Si structure are related to μc-GaP layer.

## 1. Introduction

Nowadays, growth of III-V compounds on silicon wafers is a challenge for many scientists in the world. The development of such technology is essential for new silicon photonic applications: optoelectronic integrated circuits, silicon based multijunction solar cells (MJ SC) etc. GaP is one of the most interesting materials for the fabrication of photovoltaic devices. First of all, the GaP/Si heterojunction is a perspective for bottom subcells in MJ SC, because GaP has only 0.4% of lattice- mismatch with silicon and it can be grown on Si by modern epitaxial methods. Furthermore, dilute nitrides such as (In)GaP(NAs) can be grown on GaP layers for fabricating top subcells in view of high efficiency MJ SC. Nowadays, there are many efforts to grow GaP(NAs) layers on silicon wafers [1-3], but the quality of the obtained structures is not sufficient for photovoltaic applications. It is known that molecular beam epitaxy (MBE) and vapor phase epitaxy (VPE) require high temperatures (800-900 °C) during process growth. It leads to the deterioration of the Si wafer quality [4, 5] and of the GaP/Si interface due to different coefficients of thermal expansion and inter-diffusion of atoms at the III-V/Si interface. Recently, a promising technology of GaP growth was presented in [6]. It is based on plasma-enhanced-atomic-layer deposition (PE-ALD) with alternation of P and Ga sources at temperatures below 400 °C. This work presents initial research of GaP/n-Si structures grown on silicon wafers by the PE-ALD method. The main aim of the study is the characterization of the GaP/n- Si structure by the capacitance-voltage (C-V) method and deep-level spectroscopy (DLTS).

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## 2. Experiments and results

Two different types of structures were studied. Initially, thin GaP layers were grown by PE-ALD using an Oxford PlasmaLab System 100 at 380 °C with thickness of 50-75 nm on n-type (100) silicon substrates (2-7 Ω·cm). Phosphine ($PH_3$) and trimethylgallium (TMG) were used as sources of P and Ga, respectively. An additional flow of silane is considered as a source of Si to obtain donor-doped GaP. As a result, 50 nm of amorphous and 75 nm of microcrystalline GaP layers were grown (a-GaP/n-Si and μc-GaP/n-Si). Mesa-structures were fabricated for capacitance measurements. In a first step, 50 nm of n- type amorphous silicon was deposited on the bottom of the silicon wafer by PECVD. Then silver was evaporated onto a-Si:H to form the bottom contact. This bottom contact became ohmic after thermal annealing during 20 min at 170 °C in the air atmosphere. Gold contact dots with diameter of 0.5 and 1 mm were evaporated on the top of the structures to form Schottky barrier (SB) diodes to GaP. Finally, mesa structures were formed by dry etching of the GaP layer and 2 μm of silicon. The schematic view of the fabricated structure with GaP/n-Si heterojunction is shown in Figure 1a. Furthermore, a second type of structures was fabricated to study the influence of the growth process onto the silicon wafer properties. Firstly, the GaP layer was selectively removed by wet etching. Then the same silver ohmic contact and gold SB were formed on the bottom and top sides of the silicon wafer, respectively. The mesa structures were fabricated in the same way by dry etching of 2 μm of Si. The schematic view of such Au/n-Si SB structures is shown in Figure 1b.

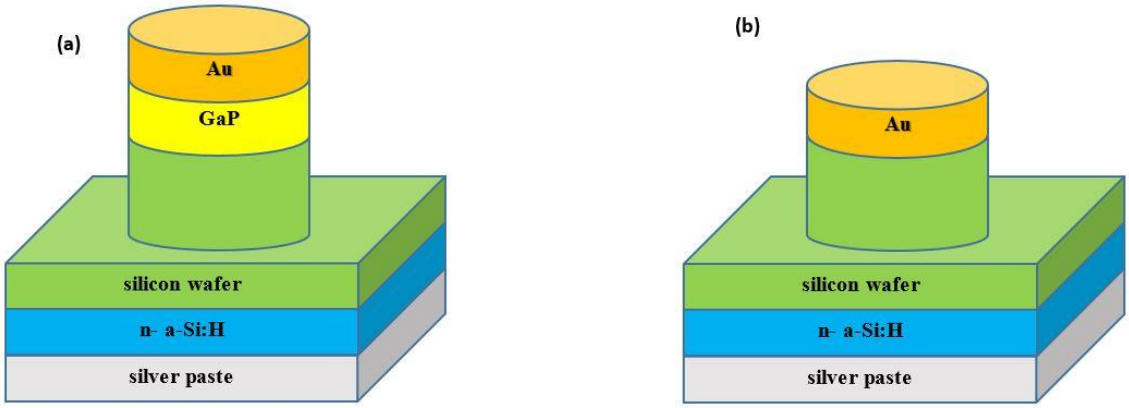


**Figure 1 (a, b).** Schematic view of GaP/n-Si (a) and Au/n-Si (b) structures.

Measurements of C-V and DLTS were performed using a liquid nitrogen cryostat in the temperature range of 80-400 K. Using C-V characteristics, profiles of effective concentration of free carriers ($N_{CV}$ - $W$) were estimated in the depletion layer approximation by equations:

$$N_{CV} = \frac{2}{q\varepsilon\varepsilon_0 S^2}\left(\frac{dC^{-2}}{dV}\right)^{-1} \quad W = \frac{\varepsilon\varepsilon_0 S}{C} \qquad (1)$$

where $W$ is the width of the space-charge region, $q$ is elementary charge, $\varepsilon_0$ is the permittivity of vacuum, $\varepsilon$ is the relative permittivity, and $S$ is contact area. An automated installation based on a Boonton- 7200B capacitance bridge was used for measurements by the classical DLTS method [7].

## 3. Results

Capacitance-voltage characteristics of the GaP/n-Si samples at 80 K and Au/n-Si at 300 K are shown in Figure 2a. The capacitance decreases with increasing amplitude of reverse bias voltage for both samples. Consequently, the extension of the space charge region (SCR) inside the structures is observed: this is the conventional behaviour of C-V curves. $N_{CV}$ - $V$ and $N_{CV}$ - $W$ profiles were plotted for the three samples in Figure 2b and Figure 2c, respectively.

The concentration profile for Au/n-Si is almost constant with a value of $1\times10^{15}$ cm$^{-3}$. It corresponds to the doping concentration of the silicon wafer (2-7 Ω.cm). The experimental profile for a-GaP/n-Si shows the constant value of $7\times10^{14}$ cm$^{-3}$, which also corresponds to the doping concentration of the silicon wafer. However, for the µc-GaP/n-Si structure a clear peak of concentration is observed at low bias voltage, which corresponds to the lowest depth of SCR. With the increase of reverse bias voltage (increase of SCR depth) the concentration becomes constant with the same value as in the Si wafer. Also, the capacitance is much higher for low bias voltage in µc-GaP/n-Si so the SCR width is lower than in a-GaP/n-Si and Au/n-Si structures.

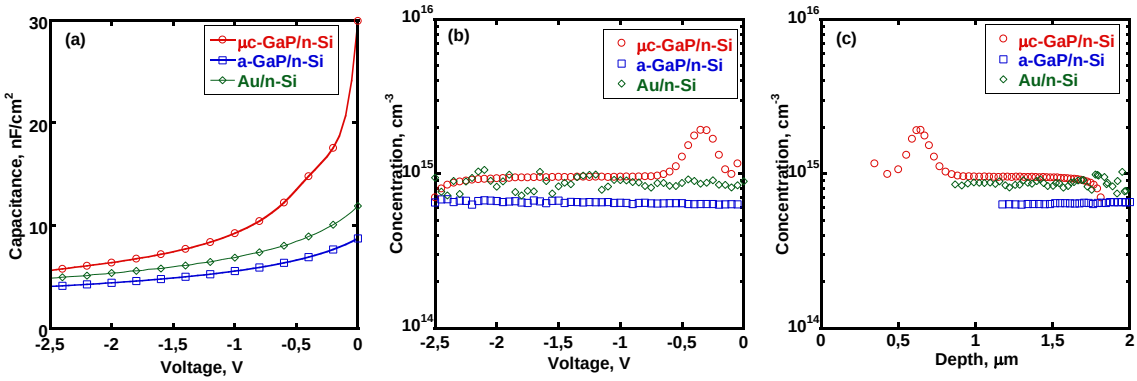


**Figure 2 (a, b, c)**. Analysis of the bias dependence of the measured capacitance of the three types of structures: *C-V* (a), $N_{CV}$-*V* (b) and $N_{CV}$-*W* (c).

Two differences are observed from the comparison of profiles for a-GaP/n-Si and µc-GaP/n-Si: smaller width of SCR for µc-GaP/n-Si and existence of a peak on its profile at low reverse bias voltage. One of the possible explanations is the different n-type doping level in GaP. We suggest µc-GaP is more doped compared to a-GaP so the concentration peak appears when SCR extends from GaP to Si through the n-GaP/n-Si interface [8]. Figure 3 shows the band diagram for GaP (n= $1\times10^{17}$ cm$^{-3}$)/Si (n= $1\times10^{15}$ cm$^{-3}$) heterojunction at zero bias voltage and the concentration profile of electrons at 80 K simulated using AFORS-HET 2.5 software [9]. The position of the peak in the concentration profile corresponds to the GaP/Si interface: for the experimental µc-GaP/n-Si sample similar phenomenon is observed (Figure 2c). However, values of SCR width are higher in the experiment than in the simulation. Disparity of values can come from imperfect bottom contact to silicon wafer. Consequently, estimation of the absolute value of interface position from the experiment can be incorrect and should be considered more critically. On the opposite, the described peak does not appear on the profile for a-GaP. It means that the SCR extends inside the silicon wafer even at zero bias voltage. Consequently, a-GaP should be fully depleted at any reverse bias voltage. It explains why the capacitance of µc-GaP/n-Si is much higher compared to that of a-GaP/n-Si. It is a very important issue because it means that the border of SCR for the a-GaP/n-Si sample is further from the heterojunction compared to the µc-GaP/n-Si one. Therefore in case of the a-GaP/n-Si sample the DLTS experiment is expected to rather detect the response of defects far from the a-GaP/n-Si interface in the bulk silicon.

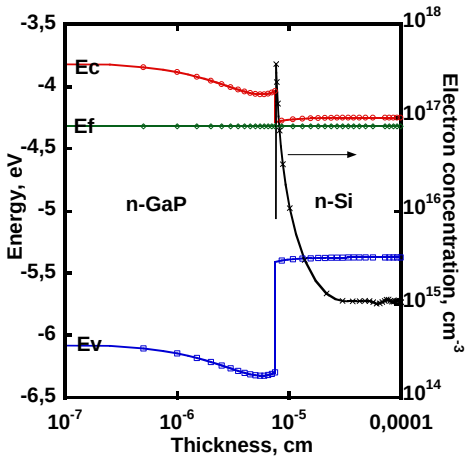


**Figure 3.** Band diagram of n-GaP/n-Si and profile of electron concentration at 80 K.

Results of DLTS measurements are shown in Figure 4. DLTS spectra of µc-GaP/n-Si (Figure 4a) have two series of peaks, which are characteristic for the response from two defect levels. Their properties are estimated from the Arrhenius plot (Figure 5) by:

$$e = AT^2 e^{-E_a/k_B T} \tag{2}$$

where $e$ is emission rate, $A$ is a pre-exponential factor, $E_a$ is the activation energy of the defect level, $k_B$ is Boltzmann's constant. Activation energies for low- and high-temperature levels are equal to 0.3 eV and 0.8 eV, respectively. Both peaks are broadened so non-exponential behavior of the capacitance relaxation due to extended defects can be suggested in this structure [10]. Unfortunately, low thicknesses of GaP layer and width of SCR estimated from *C-V* measurements do not allow us to define exactly the region in the µc-GaP/n-Si structure where the response takes place. The response can be from the GaP/Si interface, from the GaP layer or from the bulk Si. $S(T)$ spectra for a-GaP/n-Si do not allow one to extract any defect responses within our measurement accuracy (Figure 4b), because the signal is much lower compared to that of the µc-GaP/n- Si sample. Nevertheless, defects described above were not detected in a-GaP/n-Si. However, according to the above explanation the a-GaP layer is fully depleted and the SCR extends deeper in the silicon bulk as opposed to the µc-GaP/n-Si structure, so we can not detect defects in a-GaP. Also, we did not find any peaks on the $S(T)$ spectra of the Au/n-Si structures in the used temperature range (Figure 4c). It means that the silicon bulk was not deteriorated by the deposition of the GaP layer in our low-temperature deposition method. Consequently, the detected defects in the µc-GaP/n-Si structure are attributed to the µc-GaP layer. Since the detected peaks are broad, the defects can tentatively attributed to threading dislocations in µc-GaP appearing during the growth. Analysis of their nature and value of pre- exponential factors is a complicated issue and it will be explored in the future experiments in details.

Nevertheless, *C-V* and DLTS characteristics show high differences between samples with and without GaP layer. Therefore, these methods allow one to study the structures with thin GaP layers grown by PE-ALD on silicon wafers. The future research will be focused on the interpretation of the obtained results for GaP/Si structures grown in different conditions.

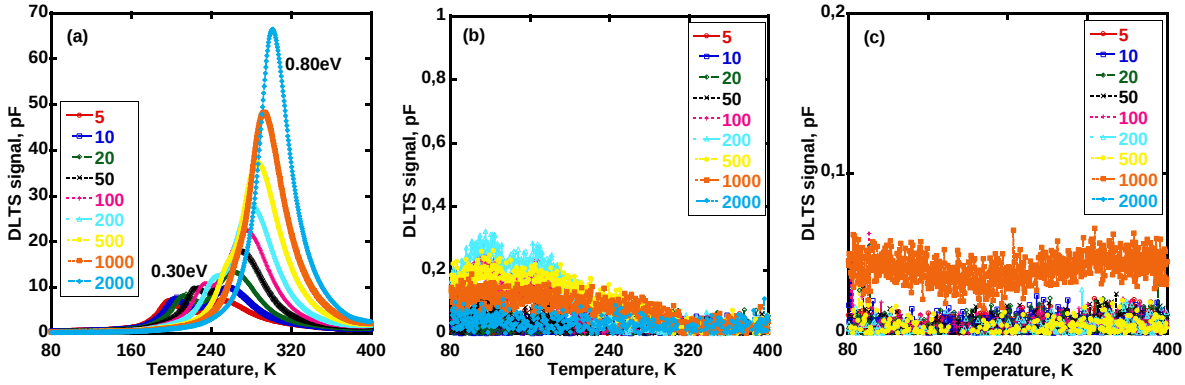


**Figure 4 (a, b, c).** DLTS spectra $S(T)$ of µc-GaP/n-Si (a), a-GaP/n-Si (b), and Au/n-Si (c) for different emission rates (in $s^{-1}$) obtained by changing the DLTS gate window.

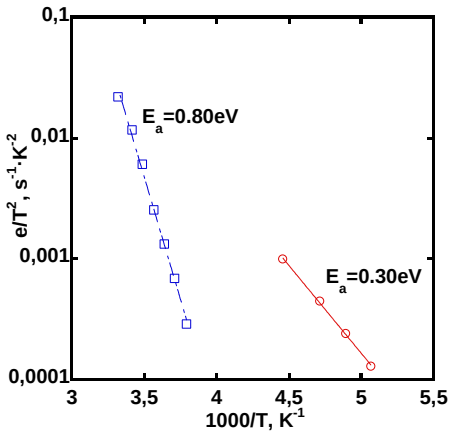


**Figure 5.** Arrhenius plots of $e/T^2$ for the two DLTS peaks detected in the µc-GaP/n-Si structure.

## 4. Conclusion

Thin layers of µc-GaP and a-GaP were grown on n-type silicon wafers by the new low temperature PE–ALD technique. Structures were characterized by capacitance-voltage and DLTS techniques. The a-GaP layer is fully depleted and no defects could be observed in the c-Si wafer. We have observed two peaks in the DLTS spectra of the µc-GaP/n-Si structure associated with defect levels having activation energies of 0.30 and 0.80 eV. The lack of response in Schottky barrier structures formed on silicon after etching of µc-GaP demonstrates that the detected defects originate from the µc-GaP layer and that no deterioration of c-Si is induced by the low temperature PE-ALD GaP process.

## Acknowledgements

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