An Accuracy-Area Tradeoff for Mixed-Signal Computation in Programmable Smart Image Sensors

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***Abstract*— Tightly embedded systems often require low power real time processing of acquired sensor data. This paper presents the design and transistor-level implementation of a mixed-signal processing element for highly area-constrained systems in applications where approximate computing is sufficient. The analog processing unit consists of a switched capacitor circuit whose imperfections such as finite gain or offset errors are evaluated here through theoretical analyses and Monte Carlo simulations for a CMOS 0.35µm technology. Transistor-level simulation results further demonstrate that this processing unit is suitable for image pre-processing tasks such as spatial convolution for edge detection.**

Keywords*— *Mixed analog-digital electronics, approximate computing, algorithm-architecture matching, smart image sensor, vision system on a chip (VSoC).

I. INTRODUCTION

Tightly integrated embedded systems need to process data streams from sensors in real-time while keeping power consumption low. Accuracy in the computation of a mathematical or logical operation is usually achieved at the expense of complexity and energy consumption. However, in many applications one can be satisfied with an approximation of the result [1], therefore the approximate computing paradigm is currently attracting a lot of interest in the design, test and embedded systems community [2]. Some image processing tasks were reported to fall under this category, such as DTC compression [3] or SVM classification [4].

Nowadays, approximate computing is being pursued mostly in terms of logic circuits or algorithms, and, with the exception of neural network that typically carry out high-level classification tasks [5], less published works study the possibility of approximate computation in the analog domain. Nonetheless, there are low-level image processing tasks where deterministic yet approximate computations could be carried out in the analog domain, saving power and chip area.

This paper describes in detail the design considerations for the implementation of mixed-signal circuits performing approximate computation for spatial and temporal filtering, in the context of a novel architecture of smart image sensors. These circuits implement approximate computations in the analog domain, with deterministic digital control. The basic concept and design equations can be used for any other analog signal processing unit where silicon area is constrained and approximate computing is acceptable. Our target application is focal-plane feature extraction for smart image sensors. These sensors provide pre-processing algorithms based on linear combinations of pixel outputs (analog values) with integer multiplicative coefficients. These coefficients must be on-the-fly reconfigurable to ensure versatility.

Many possible implementations of feature extraction for smart image sensors have been reported, such as in-pixel or matrix-wide implementations, using analog or digital approaches [6-10]. This paper uses the mixed-signal architecture introduced in [11] that aims at obtaining, at system-level, a good trade-off between versatility and surface (measured in terms of fill-factor). The flexible, smart image sensor relies on the use of macropixels which are blocks of active pixel sensors locally hard-wired to a processing element (PE), with a ratio of 1 PE for a block of 3x3 pixels as presented on Fig. 1. It was demonstrated that the required accuracy on the result of the linear combination (or convolution) is low [11]. The targeted frame rate is a classic 25 frames per seconds, which means only 25 image acquisitions and convolutions per second.

The main contribution of this paper is a thorough analysis of the proposed implementation of the PE as a switched-capacitor (SC) circuit. The SC circuit imperfections are evaluated through theoretical considerations and Monte Carlo simulations. Although switched-capacitor circuits have long been studied [12, 13], it is the first time, to the best of our knowledge, that such a study is performed in the perspective of approximate computing for extremely area-constrained systems.

Following this introduction, Section II describes the analog PE that performs reconfigurable linear combinations. Several design considerations, w.r.t. the influence of the SC circuit imperfections and the signal ranges expected in our CMOS imager are given. Theoretical expressions for the influence of a low gain, small area amplifier, as well as for the offset compensation scheme are given and discussed. Section III presents simulation results of the schematic (sized transistor-level circuit). Full-scale simulations using synthetic images pre-processed with this PE confirm the feasibility of our design approach. Section IV gives our conclusions, and outlines the remaining obstacles that must be addressed in order to fabricate a full prototype of a smart image sensor with this new architecture.

II. ANALOG PROCESSING

The PE addressed here performs linear combination of analog signal values with on-the-fly programmable integer coefficients. The originality of this implementation is the use of an analog circuit working in discrete time (a switched-capacitor

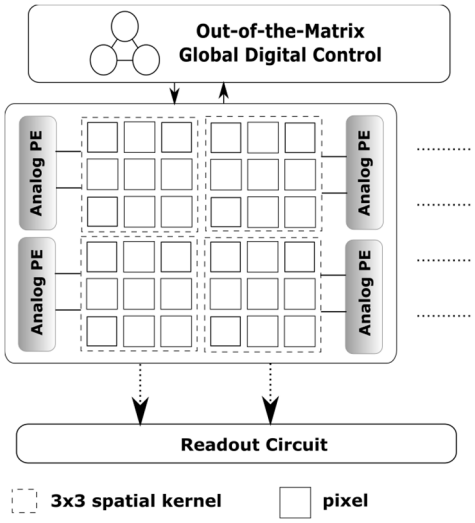

Fig. 1: Targeted system overview: a smart image sensor with processing elements (PE) distributed over the matrix of pixels. Each PE computes linear combinations of its 9 dedicated pixels, thus performing downsampled convolution [11].

circuit) to compute this operation sequentially. The required accuracy for our application was established through functional simulations [11]. In the following subsections, we discuss the design of the chosen SC circuit and evaluate its imperfections.

A. Principle of operation

In our imager, the signal coming from the photodiode is integrated on a floating diffusion node and buffered by a source follower (SF), a common read-out for active pixel sensors (APS) [14]. Further processing in current-domain would require a highly linear, low-noise conversion stage. On the other hand, linear voltage to charge conversion is easily done in CMOS using capacitors, so we chose to carry out computing in the charge domain. The challenge becomes then to design a switched-capacitor (SC) circuit taking minimum area and

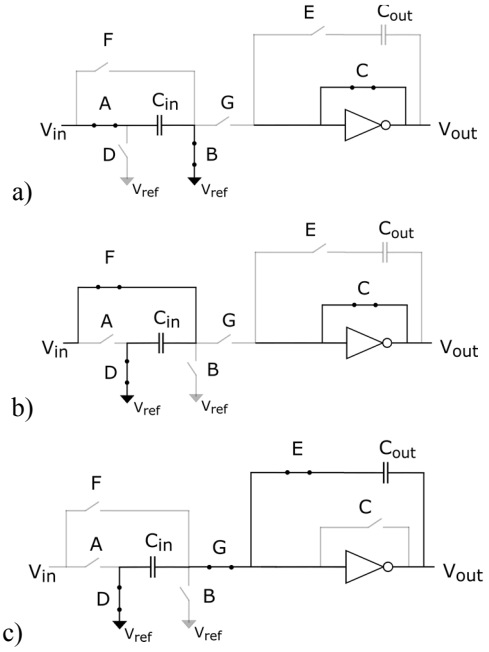

Fig. 2: Schematics of an analog accumulator: forward (a) and backward (b) charging phases and charge transfer to the output capacitance (c).

power. Our APS ensures that all input signals (as voltages) are available simultaneously, hence the inherent sample/hold (S/H) available allows us to use sequential computations instead of parallel ones, so as to minimize the area of the PE by re-using the same circuit, at the cost of loss of velocity for the PE computation. So, one programmable PE processes the different inputs one after another, accumulating the intermediate results until the operation is completed. The speed reduction has no impact, as will be shown, since all macropixels work in parallel on the full frame.

The SC circuit is based on the one presented in Fig. 2. The first input voltage value (sample) is charged on the input capacitor C_{in}, and is later transferred on the output capacitor C_{out} (see (a) and (c) schematics of Fig. 2). The same steps are applied for all input values to be summed up by the PE. The multiplication by a programmable integer is done by accumulating several times the same input. A simple modification of the basic SC circuit allows for multiplication by programmable negative integers: the sample must only be charged backward on the sampling capacitor, as shown in Fig. 2 (b). The equation for the ideal value of V_{outN}, the output of the SC accumulator after N accumulations, is given by:

$$V_{outN} = \frac{C_{in}}{C_{out}} \left(\sum_{K=1}^{N} s_K \left(V_{in(K)} - V_{ref} \right) \right) + V_{ref} \quad (1)$$

where s_K is the sign of the K^{th} accumulation. This equation corresponds to the linear combination of the inputs with $V_{in(K)}$ being the input voltage for the K^{th} accumulation, and V_{ref} is a fixed reference level that represents a null value. One can observe that the ratio of C_{out}/C_{in} is essential for an appropriate charge accumulation. Considering the input swing, the output range of the amplifier *Range* and the desired maximum number of accumulations N_{accu}, Eq (2) gives a lower bound for C_{out}/C_{in}:

$$\frac{2 \times N_{Accu} \times \max(|V_{in} - V_{ref}|)}{Range} \leq \frac{C_{out}}{C_{in}} \quad (2)$$

The values of N_{accu} and V_{in} are set by the application, while *Range* depends on the amplifier. C_{in} must be commensurate w.r.t. the input source. To limit the occupied area, minimizing C_{out} is interesting. Therefore the value of V_{ref} should be chosen as the middle of the input voltage range. In our application, 9 accumulations are required, the pixel output range is [0.5V; 1.5V]. V_{ref} is set at 1.1V instead of 1V for ease of implementation (the supply being 3.3V), since the shift of 100mV does not change things much in (2). The designed amplifier then must have an output range of [0.5; 2V]. C_{in} is set equal to the floating diffusion capacitor of our pixel and so C_{out} must be greater than $7.2 \times C_{in}$. We chose 9 to add a little margin, chiefly to avoid the limits of the amplifier range. One may observe that the voltages are attenuated by going from C_{in} to C_{out}, and not amplified as commonly seen in SC contexts.

In order to save area and power, we chose an inverter-based SC amplifier circuit [15, 16]. This kind of amplifier suffers from low gain and high variability in the bias point. Monte-Carlo simulations with a standard CMOS 0.35µm 3.3V technology showed that the bias point of a small size inverter would vary too much. Therefore an offset compensation scheme is used to avoid saturation due to the deviation from the virtual reference

voltage V_{ref} [15]. To perform subtractions with respect to the virtual reference, switch H is also added. The complete SC circuit is shown in Fig.3. An example of timing diagram for the operation of this SC circuit is given in Fig. 4.

This PE uses many switches, hence their size must be carefully considered. Moreover, one must use NMOS, PMOS or, if needed, CMOS switches. In our case, given all voltage swings (for the mentioned input range and supply values), NMOS switches are enough. The sizes of the transistors depend on the timing constraints. In our case they are very relaxed: the target for this system is 25 convolutions/s with 9 accumulations between two frames at the most. Hence each accumulation can take 1ms with added margin. So, all NMOS switches are set at minimal size. The remaining imperfections which could limit the accuracy of this circuit are finite gain, offset compensation capacitor, mismatch and charge injection.

B. Finite Gain

In a SC circuit, the finite gain of the amplifier is a source of error. Equation (1) corresponds to an ideal infinite gain amplifier. The corresponding equation for a finite gain one is presented in (3):

$$V_{outN} \approx V_{ref} + \frac{C_{in}}{C_{out}} \sum_{k=1}^{N} \frac{s_k \left(V_{in(k)} - V_{ref} + \frac{V_{offset}}{A} \right) \left(1 + \frac{1}{A} \right)^{N-k}}{\left(1 + \frac{1}{A} + \frac{C_{in}}{A C_{out}} \right)^{N-k+1}} \quad (3)$$

where $A>0$ is the gain and V_{offset} is the offset of the inverter.

Finite gain is often a source of concern in classical SC circuits, however, in our application it was functionally demonstrated that the required accuracy for our main operation (spatial convolution for pedestrian detection) is low [11]. Therefore, there is no strong requirement on the gain: electrical simulations shown in section IV were run with a maximum gain as low as 150 for the inverter.

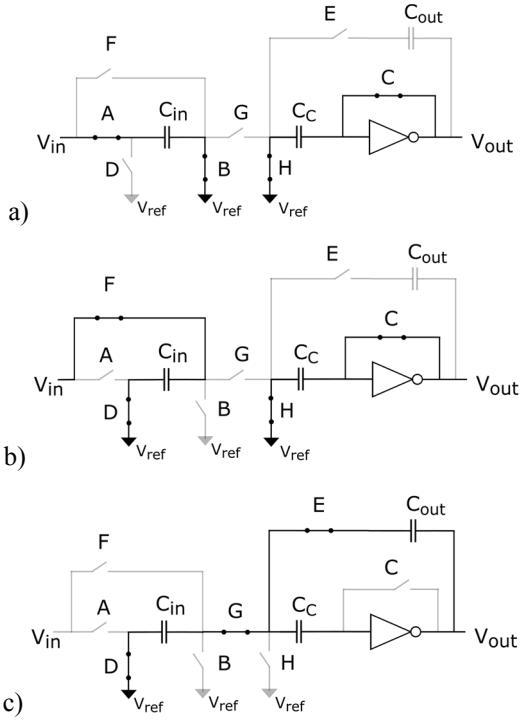

Fig. 3: Schematic of the analog accumulator with offset compensation and forward (a) as well as backward (b) charging phase and charge transfer to the output capacitance (c).

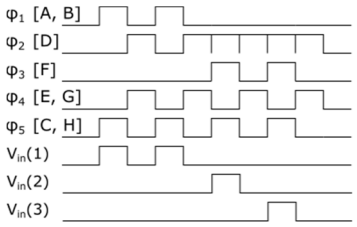

Fig. 4: Timing diagram of the control of the analog accumulator for [2 -1 -1] coefficients. φ_1 controls switches A and B, φ_2 controls D, φ_3 controls F, φ_4 controls E and G, and φ_5 controls C and H.

C. Offset Compensation Capacitor

The capacitor C_C [15] is used to compensate for the offset of the inverter. We would like to reduce its size as much as possible, to save area. To size this capacitor, we consider its influence on the output value for one charge transfer, and try to minimize this influence. We carried out a detailed analysis including all the capacitances around the inverter:

$$V_{out(/Cc)} = \frac{C_C}{C_C + C_{in} + C_{out}} \frac{C_{out} + C_{in}}{C_M} \frac{1}{1 + \frac{1}{A\,B_i} + \frac{B_0}{B_i}} V_C \quad (4a)$$

$$\text{with} \quad B_i = \frac{C_M}{C_P + C_M + \frac{C_C (C_{in} + C_{out})}{C_C + C_{in} + C_{out}}} \quad (4b)$$

$$B_0 = \frac{C_C}{C_C + C_P + C_M} \cdot \frac{C_{out}}{C_{out} + C_{in} + \frac{C_C (C_P + C_M)}{C_C + C_P + C_M}} \quad (4c)$$

where C_M is the Miller capacitance, C_P the parasitic capacitance at the input of the inverter and V_C is the voltage stored in C_C during the charging phase (difference between the actual bias point of the inverter and V_{ref}). The influence of C_C, shown through (4), decreases with the increasing value of C_C. Unfortunately, a higher value for a capacitance means a larger size. Therefore, an area/performance tradeoff must be done. The theoretical analysis in (4) has an inflexion point in the curve representing $V_{out(/Cc)}$ as a function of C_C as is illustrated on Fig. 5. The accumulator was simulated for a Sobel-like operation (4 positive and 4 negative accumulations), for various pairs of inputs. Those pairs were chosen as representative of all possible types of contrast between the first inputs and the second, since Sobel operation is used to detect edges on images. So Fig. 5 shows the mean error on the output for all these pairs. The shape is similar to the theoretical analysis of (4), and so we chose C_C = 90fF as the best area/accuracy tradeoff for our application.

D. Mismatch

Regarding capacitors mismatch, what influences the output of the accumulator is the ratio C_{out}/C_{in} as shown in (2). So Fig. 6 presents the influence of this ratio on the relative error on the

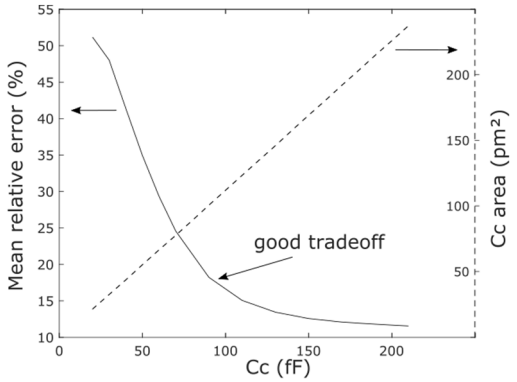

Fig. 5: Mean error on the output of the accumulator doing 4 positive accumulations and 4 negative for 81 representative sets of 2 incoming values, and area of a capacitor in a standard 0.35µm technology: both quantities are to be minimized.

output. For a given maximal error, the figure displays the maximum and the minimum acceptable ratio. For example, a ratio between 7.5 and 11 instead of a perfect 9 would not give an output error larger than 20%. Classic mismatch in standard CMOS technology (C_{out}/C_{in} between 8.9 and 9.1) therefore results on a low relative error compared to our needs (25% [11]).

E. Charge injection

Charge injection is usually a concern for SC circuits, and many circuit techniques (bottom plate sampling, half-sized dummy switch, etc.) are applied to counter it. In our approximate computation paradigm, using minimum sized transistors as switches, charge injection has such a minor impact that it was judged not worth the effort to apply any such techniques. This was confirmed by transistor-level simulations, shown later in Section III.

This design resulted in an accumulator of 1100pm² in AMS 0.35µm technology.

III. Application for a Smart Image Sensor

The designed accumulator is to be implemented in a macropixel, i.e. a group of 3x3 pixels. The complete system was designed and simulated at transistor level. As an example, simulations results for a Sobel mask used to detect edges are presented here. The Sobel mask for horizontal edges is

$$\begin{pmatrix} -1 & -2 & -1 \\ 0 & 0 & 0 \\ 1 & 2 & 1 \end{pmatrix}.$$

In terms of a macropixel, this mask means that the value of the first pixel is charged backward in the accumulator, then the value of the second top pixel twice backward, etc. until the value of the bottom right pixel is charged forward in the accumulator and accumulated. The final output value indicates whether there is an edge or not. We also ran Monte Carlo simulations to validate our design. Fig 7 presents the distribution of samples for Sobel convolution on different contrasts of edges in 1 macropixel. It demonstrates that low differences of contrasts can be told apart. The computation of Sobel masks on a complete image was also simulated at transistor level. Results are shown on Fig. 8. The horizontal and vertical edges are clearly visible. So this shows that the analog processing element performs as expected.

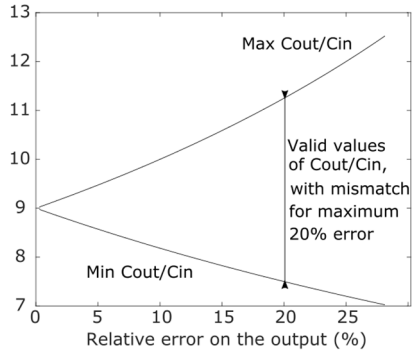

Fig. 6: Maximum and minimun acceptable C_{out}/C_{in} ratio for a given relative error on the output of the accumulator.

IV. Conclusion

We designed and explained the choices for a system performing analog approximate linear combination with tight area constraints. We discussed its imperfections such as low gain, large mismatch, and offset compensation, providing theoretical analysis along with transistor-level simulations. Given our application, a smart image sensor: performing programmable downsampled spatial convolution inside the focal plane, approximate computing using inverter-based SC circuits of very small size was shown by transistor-level simulations to yield a fully functional system. Future work is focused on the layout of the matrix of pixels and processing elements in CMOS 0.35µm standard technology, minimizing parasitic effects.

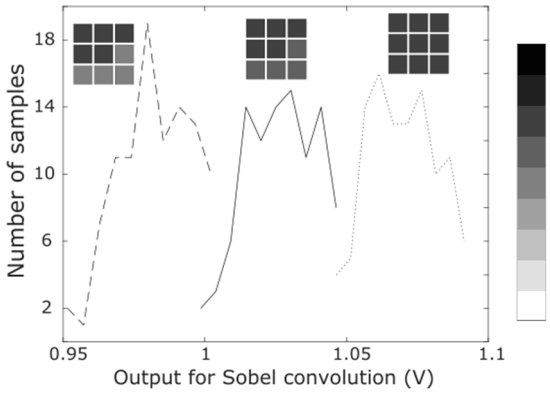

Fig. 7: Monte Carlo simulations of the system performing Sobel convolution on different types of contrasts, for 1 macropixel, respectively shown above the curves. The full grey scale is displayed on the right for comparison. Note that a plain macropixel answers near the reference of the SC circuit (1.1V).

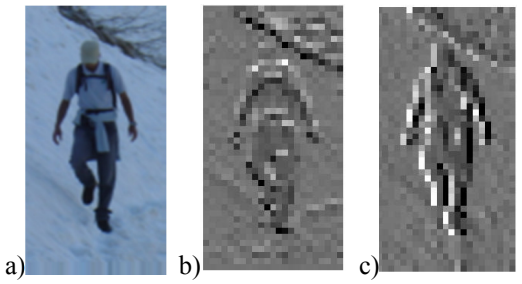

Fig. 8: Results of transistor-level simulations of our system on a whole image: a) original image (132x66 pixels); b) result of horizontal Sobel kernel (44x22 pixels); c) result of vertical Sobel kernel (44x22 pixels).

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