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ABSTRACT

Active inductors have become standard building blocks for many applications by its reconfigurability and reduced silicon area. However, the inductance variation over temperature is a main circuits' limitation in harsh environments. This paper presents a novel temperature analysis of a general architecture of active inductors, obtaining an optimal conductance value to minimize inductance variation over temperature. Based on the g_m/I_D and sensitivity analysis, temperature variation result highlights that, even if its counter intuitive to bias transistors in weak inversion, a low inductance variation of 139 ppm/°C is obtained from -45 to 175 °C.

CCS CONCEPTS

• **Hardware → Analog and mixed-signal circuit synthesis**.

KEYWORDS

temperature-aware, gm/ID methodology, active inductors, harsh environment

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1 INTRODUCTION

Internet of Things has brought the need for novel studies in order to address communication devices requirements, driven specifically by the Smart Vehicle industry [5]. In smart vehicles applications, the circuit specification is strictly regulated by security and safety standards. Reliability and robustness in the device operation must be ensured for harsh environments, including the required operating temperature range from -40 to 175 °C.

Receivers and transmitters nowadays are manly dedicated to the digital signal processing. In this context, the analog front-end is only reserved to the signal conditioning before the analog-to-digital conversion or to the amplification before transmission. In such devices, the use of inductors is indispensable for impedance matching [11] or bandwidth extension [4]. The need for a large silicon area to fabricate spiral inductors and transformers has also sparked a great interest in and an intensive research on the synthesis of inductors and transformers using active devices [15].

Active inductors (AI) have noticeable advantages as: low surface, reconfigurability, and digital CMOS compatibility. However, AI's major drawbacks are poor noise performance and power consumption. J. Ou and P.M. Ferreira have analyzed the power consumption and noise of those devices [10]. Design considerations are revealed in order to optimize AIs. However, the temperature dependency is indicated in [1] as a major challenge for AIs design. V. Kulmar *et al.* have presented new results of temperature variation effects in different AIs topologies [8]. Temperature-analyses of the variation of central frequency of a LC oscillator is revealed, and a best-case scenario is shown for a resonant frequency variation of 4.6 GHz from -20 °C to 100 °C.

Still, no design methodology is available to minimize performance variation over temperature. This paper presents an analysis of the overall thermal stability of a generic AI to propose a g_m/I_D-based design methodology. The proposal is exemplified by an AI design using XFAB 0.18 μm technology Post-layout results are presented to validate the proposal from -40 to 175 °C.

2 ACTIVE INDUCTOR

Active inductor implementations usually come from gyrators theory, and can be implemented by connecting two transconductors back-to-back as shown in Fig. 1.

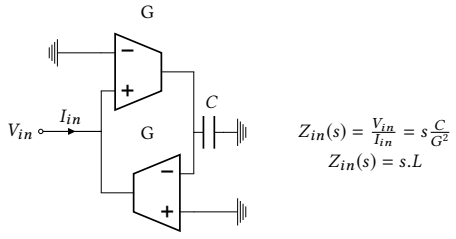

Figure 1: A Gyrator-C model representation

In order to evaluate the temperature variation effects, the transconductance is assumed to be the only temperature dependent value since C it is determined by physical dimensions and properties of the device, leading to

$$L(T) = \frac{C}{G_1(T)\,G_2(T)}. \quad (1)$$

A sensitivity function ($S_x^{f(x)}$) is defined as the percentage variation of $f(x)$ as x varies 1%, mathematically expressed as

$$S_x^{f(x)} = \frac{\frac{\Delta f(x)}{f(x)}}{\frac{\Delta x}{x}} \approx \frac{x}{f(x)}.\frac{df(x)}{dx}. \tag{2}$$

Calculating the inductance value $L(T)$ sensitivity to temperature, one may find

$$\begin{aligned} S_T^{L(T)} &= \frac{T}{L(T)} \cdot \frac{dL(T)}{dT} \\ &= -T\left(\frac{1}{G_1}\frac{dG_1(T)}{dT} - \frac{1}{G_2}\frac{dG_2(T)}{dT}\right) \end{aligned} \tag{3}$$

To minimize the temperature effects on the inductance value and consequently $S_T^{L(T)}$, an optimal $G(T)$ behavior should be found, thus

$$\begin{aligned} C\left[G(T)_{1,2}\right] &=< S_T^{L(T)}; S_T^{L(T)} >= \int_0^\infty \left(S_T^{L(T)}\right)^2 dT \\ &= \int_0^\infty \frac{T^2\left(G_2(T)G_1'(T) + G_1(T)G_2'(T)\right)^2}{G_1(T)^2 G_2(T)^2} dT. \end{aligned} \tag{4}$$

This minimization problem can be solved by a calculus of variations method and the solution is given by solving the Euler-Lagrange system equations:

$$\begin{aligned} \nabla C\left[G_{1,2}(T)\right] &= \frac{\partial L}{\partial G_{1,2}}\left(T, G_{1,2}, H_{1,2}\right) \\ &\quad - \frac{d}{dx}\left(\frac{\partial L}{\partial H_{1,2}}\left(T, G_{1,2}, H_{1,2}\right)\right) = 0 \\ L\left[T, G_{1,2}, H_{1,2}\right] &= \frac{T^2\left(G_2(T)H_1(T) + G_1(T)H_2(T)\right)^2}{G_1(T)^2 G_2(T)^2} \\ H_{1,2} &= \left(\frac{dG_{1,2}(T)}{dT}\right), \end{aligned} \tag{5}$$

applying the boundary condition that $G_0 = G(T_0)$ and solving (5) the optimal found is

$$G_{1,2}(T) = G_0.e^{\pm\alpha(T-T_0)}. \tag{6}$$

This solution can be proved by using the theorem described in [7].

3 TEMPERATURE EFFECTS ON CMOS TRANSISTORS

Actual AI implementations typically uses MOSFETS gyrators, those transistor models are usually derived from two limit situations in [6]. The first one, weak inversion (WI), is obtained when the gate to source voltage (V_{GS}) is lower than the threshold voltage (V_{th}). Otherwise when $V_{GS} >> V_{th}$, it is said that the transistor works in strong inversion (SI) regime. Transistor IxV characteristics are described in [2] and in [6] as

$$\begin{aligned} I_D\Big|_{WI} &= I_0 \cdot \frac{W}{L} e^{\frac{V_{GS}-V_{th}}{n\phi_t}} \cdot \left(1 - e^{\frac{V_{DS}}{\phi_t}}\right), \\ I_D\Big|_{SI} &= \frac{\mu \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{th})^2. \end{aligned} \tag{7}$$

The C_{ox} is the gate oxide capacitance density; $\frac{W}{L}$ is the transistor aspect ratio; μ is the carriers mobility; The ϕ_t is the thermal voltage defined as $\frac{k.T}{q}$, where k is the Boltzmann constant, q the electron charge and T the absolute temperature in Kelvin. It is important to point out that, in [2], the I_0 temperature dependency is not explicit, however it can be shown that it is proportional to $C_{ox} \cdot \mu \cdot \phi_t^2$ [9]. The body and Drain-induced barrier lowering (DIBL) effects where omitted on (7) for reader clarity.

To fully analyze the transistor performance in temperature, one need to model their parameters behavior defined as

$$\begin{aligned} V_{th}(T) &= V_{th0} \cdot \left[1 + \alpha_{th}(T - T_0)\right], \\ \mu(T) &= \mu_0 \left(\frac{T}{T_0}\right)^{-\alpha_\mu}, \end{aligned} \tag{8}$$

where based on the Boltzmann Transport Equation solution, α_μ is bias dependent. That can be explained by the fact that when electric field is low (i.e. WI), the transport phenomena is dominated by the diffusion effect having a positive temperature dependency due to thermal excitation [9]. Considering the increase in the channel electric field and subsequently the V_{GS}, the drift effect is predominant given a negative temperature dependency to the current density due to the energy losses by phonon emission. On both regions, one can define the small signal drain to source conductance (g_{ds}) and gate voltage to drain current transconductance (g_m) by following [6] model.

3.1 Temperature-aware sensitivity analysis

Model in [6] allows the definition of analytical expression for the different g_m/I_D temperature sensibilities on both WI and SI. The λ is the DIBL factor, which is described in [13] as temperature invariant. Those expressions can be useful when analyzing the sensitivity in a circuit where the transistors bias is known.

$$\begin{aligned} S_T^{J_{DS}}\Big|_{WI} &= 2 - \alpha_\mu \frac{V_{GS}}{\phi_t}, \\ S_T^{J_{DS}}\Big|_{SI} &= -2\frac{\alpha_{th}.T.V_{th0} + \alpha_\mu\left(V_{GS} - V_{th}(T)\right)}{V_{GS} - V_{th}(T)}, \\ S_T^{\frac{g_m}{g_{ds}}}\Big|_{WI} &= -\frac{1}{\phi_t}\frac{V_{DS}\,\mathrm{csch}\left(V_{DS}/(2.\phi_t)\right)}{4\cdot\lambda - 2.n\left(1 + \tanh\left(V_{DS}/(2\phi_t)\right)\right)}, \\ S_T^{\frac{g_m}{g_{ds}}}\Big|_{SI} &= S_T^{J_{DS}}\Big|_{SI}, \\ S_T^{\frac{g_m}{I_D}}\Big|_{WI} &= -1, \\ S_T^{\frac{g_m}{I_D}}\Big|_{SI} &= \frac{2\alpha_{th}}{(V_{GS} - V_{th}(T))^2}. \end{aligned} \tag{9}$$

4 AI DESIGN EXAMPLE

In order to validate the hypothesis made in Sections 2 and 3, a transistor-level AI is designed. Figure 2(a) illustrates the chosen AI topology. Figure 2(b) is the AI model used in this work. In Fig. 2(a), the M_p transistor works as a transconductance in SI, and the M_n transistor works as a simple voltage-controlled resistor. So the conductance required in (1) are g_{mp} and g_{dsn}. If M_n is biased in WI it g_{ds} presents a high exponential temperature characteristic, as desired in(6). Since V_{DS} is too small, one can write

$$g_{ds}\Big|_{WI} = \frac{\phi_t^3}{2}.Cox.\mu(T)\frac{W}{L}.n.e^{\frac{V_{GS}-V_{th}}{n\phi_t}}. \tag{10}$$

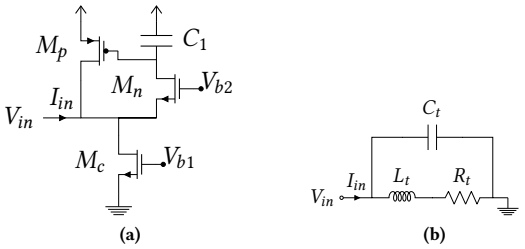

Figure 2: (a) AI implementation proposed in [10] and (b) the transistor level model from [15]

In addition, ϕ_t is in the order of tenths of millivolts, and thus ϕ_t^3 can be considered negligible. The equivalent model values are calculated as:

$$\begin{cases} L_t &= \frac{C_1}{g_{dsn}(g_{dsp}+g_{mp})}, \\ R_t &= \frac{1}{g_{dsp}+g_{mp}}, \\ C_t &= C_{gsn} + C_{gdc} + C_1 + \frac{C_1 . g_{dsp}}{g_{dsn}}. \end{cases} \quad (11)$$

The M_p drain to source conductance appears as a parasitic effect due the DIBL and can be minimized by using large length transistors. In order to analyze the different parameters contribution to the overall temperature sensitivity using the g_m/I_D methodology, one can find L_t as

$$L_t = \frac{1}{W_t . J_{DSn} . J_{DSp}} . \frac{C_1 . g_{mn}/g_{dsn}}{\left(g_{dsp}/I_{Dp} + g_m/I_{Dp}\right) . g_m/I_{Dn}}, \quad (12)$$

where $W_t = W_p . W_n$. Since wide channel transistors are used, one may assume $g_{dsp}/I_{Dp} << g_m/I_{Dp}$. Using this approximation, one may calculate the overall inductance sensitivity to the temperature as

$$S_T^{L_t} \approx S_T^{\frac{g_m}{g_{dsn}}} - (S_T^{\frac{g_{mn}}{I_{Dn}}} + S_T^{J_{dsp}} + S_T^{J_{dsn}} + S_T^{\frac{g_{mp}}{I_{Dp}}}). \quad (13)$$

As a consequence of no DC path on M_n I_{Dn}, one can suppose that its drain to source voltage is very low, making this approximation in the equations deduced in Sec. 3 and considering WI the following approximation is valid:

$$S_T^{\frac{g_m}{g_{dsn}}} = S_T^{\frac{g_{mn}}{I_{Dn}}} = -1. \quad (14)$$

Therefore, it is possible to nil $S_T^{L_t}$ by making

$$S_T^{J_{DSn}} + S_T^{J_{DSp}} + S_T^{g_{mp}/I_{Dp}} = 0. \quad (15)$$

4.1 Temperature-aware transistor analysis

The XH018 process technology from the XFAB Silicon Foundries is chose in this work. XH018 technology is ideal for system-on-chip (SoC) applications in the automotive market such as high-voltage control devices, in engine compartments or housings circuitry with temperature range up to 175 °C, as well as embedded low-voltage applications in the communications, consumer and industrial market [14].

In order to evaluate the different sensibilities on the XH018, parameters were estimated (electrical simulation) by injecting a desired drain to source current over a normalized MOSFET with a width of 1 μm using an ideal Wilson's current mirror. The simulated sensibilities are shown in Fig. 3(a), 3(b) and 3(c).

With the different sensibilities calculated it is possible to numerically determinate the optimal J_{DS}^* by finding the values that nil (15). Analytical results are depicted in dashed blue line in Fig. 4. It presents a strong exponential characteristic in agreement to simulation data in continuous red line, which validates the proposal in Sec. 2. Thus, a fitting was carried out in J_{DS} expression to obtain

$$g_{mp}^* = \frac{2.J_{DS}^*.W}{(Vgs - V_{th})} = G_0 . e^{C_1(\frac{1}{T_0} - \frac{1}{T})}. \quad (16)$$

Since V_{GS} is fixed by the circuit, V_{th} presents a linear dependency on temperature as

$$J_{DS}^* = G_0 . e^{\alpha(T-T_0)}(V_{GS} - V_{th0}(1 + \alpha_{th}(T - T_0))). \quad (17)$$

To achieve this result a beta multiplier reference [3] using a negative temperature coefficient was designed using Spectre Virtuoso global optimization tools. Temperature characteristics match the second order Taylor series of (17). The M_c and M_p transistor width was chosen in order to have to desired J_{DS}^* of 400 $\mu A/\mu m$ at 27 °C, their lengths where chosen to bias the transistor in SI with $I_{DS} \leq 500\ \mu A$. The final values obtained are: $W_p = W_2 = 1.6\ \mu$m, $W_n = 880$ nm, $W_1 = 2\ \mu$m, $L = 680$ nm, $k = 0.25$,$R = 1.47\ k\Omega$. W_1 are the PMOS transistor widths of the beta multiplier, W_2 the NMOS beta multiplier width and k the ration between the beta multiplier's NMOS width.

4.2 Post-Layout Simulation Results

The AI layout was implemented using Cadence Virtuoso with the XTH018 design kit having an area of 15.6 x 10.4 μm^2, circuit layout was omitted due to the lack of space. Post-layout 80-points Monte Carlo S-parameters (from V_{in} to V_{b2} ports) simulations are carried out for 221-points temperature variation from -40 to 175 °C. The input impedance is obtained from the V_{in} node and the inductance value is extracted.

Figure 5(a) compares the optimized active inductor design, in blue, using the sensitivity analysis with a reference active inductor design, in orange, with a simple current mirror bias. Only mean results of Monte Carlo simulation are presented; they are normalized for $L_t = 2.65\ \mu$H. Optimized inductor presents a variation below 3 %, while reference design varies for 100 % for a temperature variation from -40 to 175 °C.

Figure 5(b) presents the optimized active inductor mean value, continous line, and three standard deviation, in error bars. The results have a maximum variation of 139 ppm/°C for the L_t. Besides, a 1035 ppm/°C for R_t is found fluctuating around 400 Ω (figure not presented). A controlled and a small L_t variation over temperature is first presented here, which enables the use of AIs in harsh environments applications as smart vehicles.

5 CONCLUSION

AIs have an interesting trade-off when inductor reconfiguration is required. However, its use in hash environments is limited due the usual high sensitivity to temperature effects. This paper presented a new temperature-aware design methodology to deal with this issue. Based on the g_m/I_D and sensitivity analysis, temperature variation is minimized when a counterintuitive transistor bias (WI)

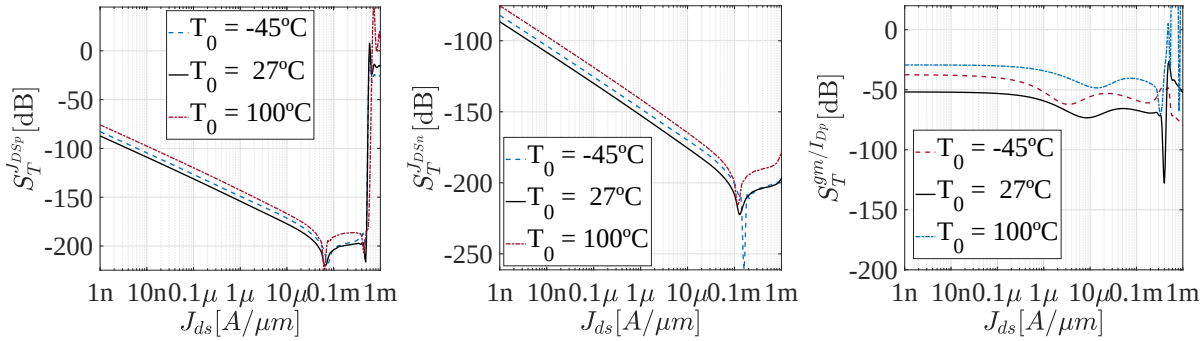

Figure 3: Ideal Wilson current mirror is used for parameters extraction: (a) $S_T^{J_{DSp}}$ (b) $S_T^{J_{DSn}}$ (c) $S_T^{g_{mp}/I_{Dp}}$

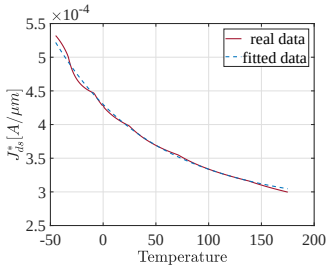

Figure 4: Sensitivity roots, and fitted data based on model presented in (17).

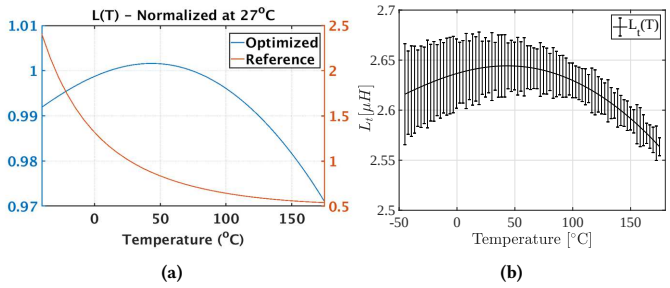

Figure 5: Post-layout Monte Carlo simulations from -40^oC to 175^oC : (a) comparison between the optimized design in blue and reference design in orange; (b) variability analysis of the optimized design having the mean values in continuous line and 3 σ in error bars.

is used. An inductance variation as low as 139 ppm/°C is reported from -40 to 175 °C. The proposed methodology can be used to fabricate reliable low-power temperature-aware AIs suitable in harsh environments such as internet of things and autonomous cars applications.

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