Building blocks development for defect-free growth of GaAs on silicon for tandem solar cells

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BUILDING BLOCKS DEVELOPMENT FOR DEFECT-FREE GROWTH OF GaAs ON SILICON FOR TANDEM SOLAR CELLS

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ABSTRACT: The monolithic integration on silicon of GaAs, and more generally of III-V semiconductors, is a very attractive and promising route for the production of high efficiencies multijunctions devices in the manner of those developed for space applications on germanium, but at a much lower cost suitable for terrestrial PV applications. The purpose of this paper is to present the building blocks we have developed for defect-free growth of GaAs on silicon for tandem solar cell applications. This will be addressed from the technological point of view as well as from design, modelling and characterization perspectives. Preliminary work has allowed the identification of critical technological bottlenecks, following which solution routes have been developed as will be presented and discussed. The resulting design for a GaAs/Si tandem solar cell will then be described..
Keywords: Epitaxy, III-V Semiconductors, Silicon, Multijunction Solar Cell

1 INTRODUCTION

The integration of III-V materials on Si substrates is a long standing goal in optoelectonics. For example Yang et al. [1] demonstrated a three terminal design at 19% efficiency. Later, the field concentrated on graded buffer techniques until a recent result by S. Essig et al. [2] who, going back to techniques similar to Yang [1], have demonstrated a 29.8 % AM1.5G efficiency with a mechanically stacked GaInP/Si tandem cell. Compared to the technology leading to this last outstanding efficiency record, the benefit of our approach is the monolithic integration of the III-V compound directly on the silicon substrate [3, 4].

The lattice parameter mismatch leading to threading dislocations is however the major problem that many approaches have tried to circumvent. But until now no one has succeeded in achieving defect-free and cost-effective direct integration of the simplest GaAs binary compound on silicon. One of these approaches, selective area epitaxy (SAE) of GaAs on patterned Si, has shown significant improvements, yielding mostly defect-free epitaxial layers. In previous work, we have demonstrated the perfect integration on silicon of micrometric size GaAs crystals without any structural defects nor stress, using Chemical Beam Epitaxy (CBE) with Epitaxial Lateral overgrowth on Tunnel Oxide from nanoseeds (ELTOn) [5], the principle of which is illustrated in Figure 1. The second breakthrough that we demonstrated previously is the very good electrical connection not only between the GaAs microcrystals and the Si substrate, but also across the GaAs/thin SiO_2/Si sandwich (tunneling assisted transport) surrounding the nanoholes [5].

An interesting consequence of this is that unlike many optoelectronic devices where continuous layers are desirable, the micrometric GaAs crystals form a textured surface which can be exploited to improve light management by reducing front surface reflection and contributing to light trapping. The GaAs array of non coalescent micro-crystals, free of structural defects, providing a quasi complete covering of the Si substrate, is therefore a promising route to III-V on Si mulltijunction solar cells. In this paper, we present and discuss three main critical technological bottlenecks and their solution routes identified by previous work, allowing progress towards a GaAs on Si tandem demonstrator based on our ELTOn process. These three technological bottlenecks are : i/ the SiO_2/Si surface patterning in order to integrate the GaAs crystals in a regular way, ii/ the control and optimization of the GaAs doping, iii/ the quasi complete covering of the SiO_2/Si substrate with non coalescent GaAs crystals.

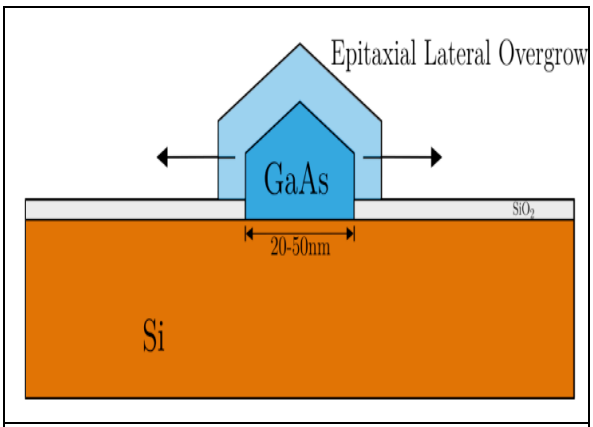

Figure 1: Epitaxial Lateral overgrowth on Tunnel Oxide from nanoseeds (ELTOn): the growth first only begins inside the nanoholes performed in the ultra-thin SiO_2 layer covering the crystalline silicon wafer and then can also extend laterally on top of the SiO_2 layer, once the GaAs growing surface comes out of the hole.

2 RESULTS AND DISCUSSION

2.1 Nanoscale opening inside the ultra-thin silica layer

Prior to GaAs epitaxy an important step is the opening of the nanoscale holes through the ultra-thin silica layer (around 1 nm thick). To demonstrate the ability of the ELTOn growth for the perfect integration of micrometric size GaAs crystals, we first used a random patterning of the silica layer directly performed in situ in the growth reactor. The oxidized silicon substrate was

exposed to a silane partial pressure of 0.66 Pa at a temperature less than 650 °C during 4 min for Si (001) and 1 min 30 s for Si (111). This results in pure Si nano-areas formed via the reduction of SiO_2 into volatile SiO. This method has the advantage of easily providing nanoscale seeds around 50 nm in width, randomly spaced at the surface of the oxidized Si substrate. With this in situ patterning of the silica layer, we have already demonstrated for the first time a monolithically integrated GaAs/Si heterojunction diode with excellent rectification properties exhibiting a dark forward current as high as 10 $kA.cm^{-2}$ [5]. This also shows that current-assisted tunnelling is possible through the entire ultrathin silica layer underneath the whole GaAs crystal, which is an important point for further device implementation.

However, in order to produce a PV device demonstrator of significant area around 1 cm^2, an important aim is now to extend this epitaxial method to surface patterning in order to integrate the crystals in a regular way to have a quasi-complete covering of the Si substrate, without coalescence of the GaAs microcrystals to maintain their very good electronic properties by avoiding detrimental grain boundaries. We achieved good initial results (Fig. 2 and 3) with a conventional technique based on E-beam lithography. However, as can be seen in Fig. 2, not all GaAs crystals are monocrystalline (e.g. the defective crystallite in the first column on the left). The reason has been identified and we now present the route to improving this process or to develop an alternative more up-scalable technique.

In order to minimise the cost of the localisation process for nanoscale seeds we propose to apply and develop other lithography method such as Nanoimprint (NIL) and Nanosphere Lithography (NSL) which have the advantages to be cost effective and up-scalable techniques for PV. The nanoimprint method is based on Soft UV nanoimprint lithography (S UV-NIL) [6]. This technique uses the printing of a mold also called “stamp” in a resist. In our case the stamp will be flexible, generally in Poly(dimethylsiloxane) PDMS, and the fundamental step is to design this stamp from a silicon master mold obtained by E-beam lithography. PDMS mixed with his curing agent is casted on master mold and annealed. Figure 4.1, presents SEM image of an imprint in UV curable resist (AMONIL from AMO GMBH) with PDMS flexible stamp obtained from a Si master mold. Comparing this achievement with the ELTOn process requirements necessary to grow non coalescent GaAs crystals with a typical 1 micrometer size ensuring however a quasi complete coverage of the SiO_2/Si surface, we note that the diameter of the nanoholes has to be decreased down to 50 - 100 nm, and their centers spacing has to be increased twice. These typical dimensions are compatible with S UV-NIL.

In parallel, in order to minimise further the cost of the localisation process, we propose also to study the use of nanosphere lithography (NSL). The NSL technique is based on the self-assembly [7] of commercially available low cost polystyrene beads (Fig. 4.2). By using simple process routes, single or double monolayers (Fig. 4.3) of spin-coating beads can be deposited onto substrates. Using different bead diameters, the separation distance between the openings can be tuned with the fabrication of size-tunable nanoparticles in the 20-1000 nm range. Small openings in-between the beads (down to 20 nm) can be used to deposit various materials, or as an etching mask.

It should be noted that nanosphere lithography yields only hexagonal patterns, which is perfect for the integration of closely-packed hexagonal GaAs µ-crystals. Thus, the implementation of this NSL technique as an etching mask also appears very attractive and it twill be interesting to compare its results with the NIL one in order to produce hexagonal patterns of nanoscale seeds through a very thin SiO_2 layer.

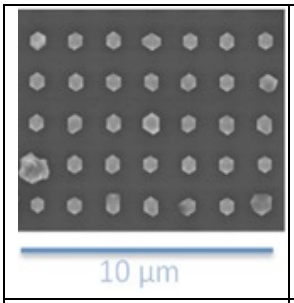

Fig. 2: Plan-view of a scanning electron microscopy (SEM) image of regularly patterned microscale GaAs crystallites on (111) Si. Underneath silica layer patterned with e-beam lithography.

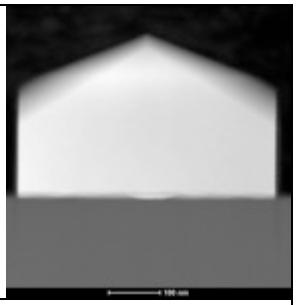

Fig. 3: Dark-field cross-sectional TEM images of the localised GaAs/(111) Si µ-crystal showing the perfect integration without any antiphase domains nor dislocations nor twins.

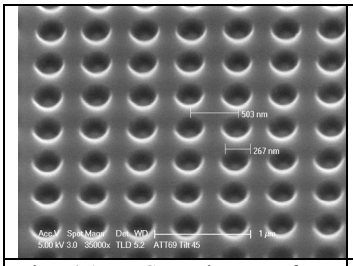

Fig. 4.1 : SEM image of an imprint in UV curable resist with PDMS flexible stamp obtained from a Si master mold, obtained at C2N (horizontal distance between two adjacent holes centers = 503 nm)

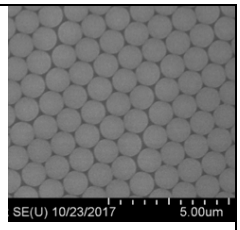

Fig. 4.2: Regularly ordered nanospheres based on the self-assembly of polystyrene beads on Si (001) obtained at C2N

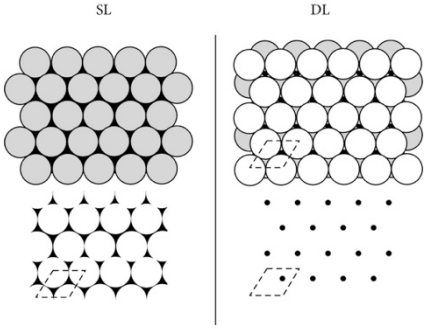

Fig. 4.3 : Schematic diagrams of single-layer (SL) and double-layer (DL) nanosphere masks and the corresponding periodic particle array surfaces (dotted line = unit cell) [8]

2.2 Control of the GaAs doping

The residual doping control in a single GaAs micro-crystal is a pre-requisite first step to developing future

design and technology of multijunction solar cells based on this approach. Local scale electrical I(V) measurements of the GaAs/Si heterojunction performed with CP-AFM have demonstrated a high rectification ratio [5]. However a high p-type non intentional doping level was indicated, which is related to high carbon incorporation induced by the trimethylgallium, the Ga precursor. The precise doping level determination in a single µ-crystal by local I(V) or C(V) measurements is difficult because in the first case the estimation is too indirect and in the latter one, the capacitance values are too small to be easily measured. To obtain a better estimation of the doping level, we have developed a contactless method based on the measurement of the variation of the bandgap versus temperature [9]. The bandgap value is extracted from the micro-photoluminescence spectra of a single GaAs crystal and the lattice temperature is evaluated by Raman scattering. The bandgap narrowing due to high density of free carriers is taken into account and the doping density can then be estimated from the fit of the bandgap evolution with temperature. With an improvement of this method detailed in [10] we have extracted a p-type doping density comprised between $2.0x10^{18}$ cm^{-3} and $2.8x10^{18}$ cm^{-3} in a nominally undoped GaAs crystal grown under our standard CBE growth conditions detailed elsewhere [3, 5].

Such a rather high doping content has been attributed to carbon incorporation during the Epitaxal Lateral overgrowth on Tunnel Oxide from nanoseeds (ELTOn) process using TriMethyl-Gallium (TMGa) and TertiaryButyl-Arsine (TBAs) as gas precursors [9]. This high carbon doping has been observed in the literature, and one of the proposed solutions to control the carbon incorporation is to adjust the concentration by the simultaneous use of TEGa (TriEthyl-Gallium) and TMGa together with TBAs. Using TEGa and TMGa in variable proportions is expected to allow a good control of the level of doping over a range from 10^{14} cm^{-3} to 10^{20} cm^{-3} [11]. One can also note that carbon is a very popular element for GaAs p-type doping thanks to its high solubility limit and its low diffusion coefficient, making it ideal for abrupt junctions.

For the n-type doping of GaAs, we have recently found that the use of SiH_4 as precursor gas for Si also permits to dope GaAs. However when TMGa is the only gas precursor for Ga, Si seems acting like carbon and probably favors a p-type doping of GaAs (C and Si are both group-IV materials). To determine if a n-type doping could be more easily achieved, it would then be relevant to investigate the use of TEGa (instead of TMGa, or a mixture of both precursors) and SiH_4 during the growth. Nevertheless, for the n-type doping of GaAs, Tellurium-doping with the use of DETe (Diethyl Telluride) as precursor gas could reveal an interesting alternative route. Tellurium has several remarkable properties that makes it an attractive n-type dopant for GaAs. It allows high doping levels to be achieved as a result of a low activation energy compared to other typical n-type dopants such as silicon. It shows a weaker memory effect as compared to other group-VI dopants such as sulfur or selenium as well as having a low diffusion coefficient in GaAs that favors the growth of abrupt interfaces, which is a significant factor in the development of tunnel junctions.

2.3 Impact of a partial coverage of the SiO_2/Si substrate with non coalescent GaAs crystals

S. Essig et al. [2] have demonstrated the last outstanding 29.8 % AM1.5G efficiency record with a mechanically stacked GaInP/Si tandem cell. Using the simpler GaAs binary compound, we have shown by quantitative modelling that the same high efficiency is achievable with a GaAs/Si tandem cell [12]. The assessment of our realistic model software [13] (called SOL) has been fully proven by our very accurate modelling of the published experimental data of record multijunctions solar cells [12]. For a full coverage of the SiO_2/Si substrate with GaAs crystals, Figure 5 shows the results of our SOL modelling of the targeted GaAs/Si tandem cell demonstrator under AM1.5G spectrum [12].

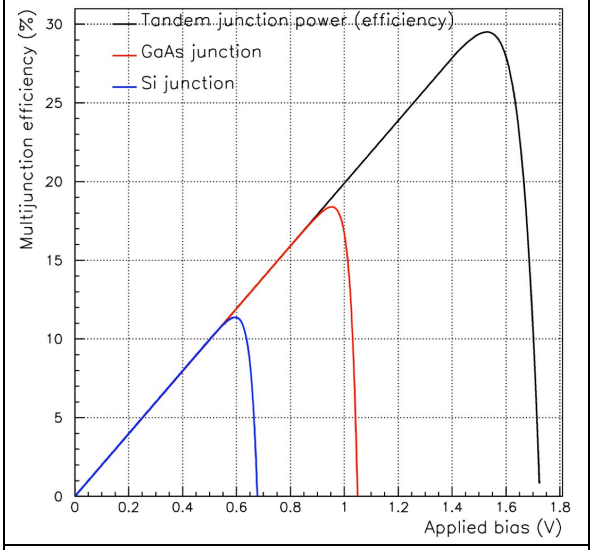

Fig. 5 : SOL modelling of the GaAs/Si tandem junction device (complete GaAs area coverage) showing the power curves converted to efficiency by dividing by the incident AM1.5G spectrum. The peak efficiency is 29.2 % at Vmp = 1.54 V and J_{SC} = 19.5 mA/cm^2, V_{OC} = 1.72V, FF = 87.3 %

This structure reaches 29.2 % without concentration. While lower than the ideal limiting efficiency, it must be emphasized that this realistic modelling achieves efficiencies greater than current records for single junction Si cells. In this device, the GaAs cell is thinned to match currents between the GaAs cell and the Si cell. Improving our present SOL modelling with optical 2D (3D) numerical modelling will help addressing this current matching issue with both layer thickness and the implicit surface texturing resulting from non-coalescent GaAs crystals. The experimental efficiencies are expected to be lower than exhibited in Figure 5 due to the lack of coalescence between GaAs microcrystals. Figure 6 shows efficiency trends as a function of technological bottleneck (iii) the area coverage mentioned in the introduction. For complete GaAs area coverage, an optimum GaAs thickness is found by the SOL model such as to maximise tandem efficiency by ensuring current continuity which is 0.4 µm in total [12]. For lower area coverage, the GaAs thickness must be increased in order to continue to ensure current continuity. Fig. 6a shows this optimal GaAs layer thickness as a function of area coverage which is necessary in order to obtain current matching and optimal efficiency. We can note that these optimal GaAs

thicknesses are fully compatible with reasonable CBE durations growth.

Nevertheless, efficiency will drop as more light is transferred directly to the Si subcell, and an increasing proportion of the light which should ideally be absorbed in the GaAs is absorbed in the Si, thereby increasing the thermalisation loss. Figure 6b shows that efficiency increases quasi linearly above an 80% area coverage of GaAs microcrystals leading to efficiencies comprised between 25% and 28% for a compact area coverage range between 86% and 96% that is expected achievable with the NIL or NSL approaches described in sections 2.1.

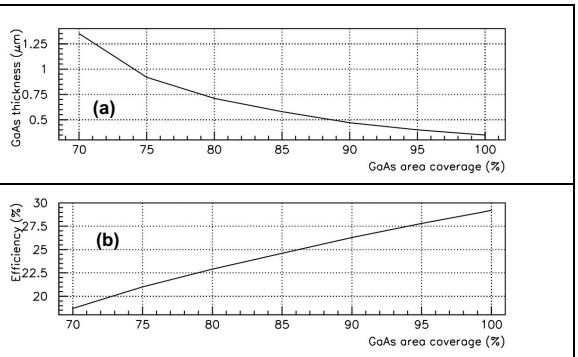

Fig. 6 : SOL modelling of the GaAs/Si tandem junction device showing (a) the optimized GaAs thickness and (b) the efficiency dependence, versus the GaAs coverage of the SiO_2/Si surface.

3 SUMMARY

We have presented an innovative strategy based on Chemical Beam Epitaxy (CBE) with Epitaxial Lateral overgrowth On Tunnel oxide (ELTOn) to integrate monolithically on silicon defect-free micrometric size GaAs crystals. Integrating these crystals in a regular array to have a quasi-complete covering of the Si substrate, without coalescence of the GaAs microcrystals, is therefore a very promising route towards the production of a GaAs/Si tandem cell at an affordable cost for terrestrial PV applications. The results already achieved have enabled the identification of the bottlenecks and to discuss the possible routes for III-V on silicon multijunctions solar cells as the tandem structure presented in this paper can be the building block for further extension to triple junctions.

4 ACKNOWLEDGMENTS

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