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Study of GaP/Si heterojunction solar cells

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Abstract

The GaP/Si heterojunctions fabricated by molecular beam epitaxy (MBE) and plasma enhanced atomic layer deposition (PE-ALD) were studied. The degradation of charge carrier lifetime in Si was observed during the growth of single-crystalline GaP layer on Si substrates by MBE at 500-600 °C. The study performed by PL and DLTS has demonstrated the presence of the defective layer in Si, which is located within ~30 nm near to the GaP/Si interface. This defective layer leads to significant reduction of solar cell performance for anisotype n-GaP/p-Si heterojunction due to strong recombination in the space charge region. The GaP/Si heterostructure with Si n-p homojunction exhibits better performance compared to the anisotype n-GaP/p-Si heterojunction because the defective layer is located in the n-Si emitter formed by intentional P diffusion. On the contrary, the deposition of amorphous GaP layer by PE-ALD at T < 380 °C does not lead to the degradation of Si wafer charge carrier lifetime.

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Keywords: Silicon, GaP, heterojuction, defect characterization, MBE

1. Introduction

Silicon based solar cells are by far dominating the PV market due to the availability and relatively low price of Si substrates. One of the most efficient ways to increase the Si solar cell performance is to use heterojunction designs. Thus heterojunctions combining hydrogenated amorphous silicon (a-Si:H) and crystalline silicon (c-Si)

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have reached 24.7% conversion efficiency for n-type Si wafers with conventional architecture, and 25.6% when combined with interdigitated back contacts [1]. This value is relatively close to the theoretical limit of Si single junction solar cells, which is mainly caused by the thermalization losses [2]. The most efficient way to reduce the thermalization losses is to use the multijunction approach. The multijunction solar cells based on III-V compounds have demonstrated the most successful development achieving the absolute world efficiency over last tens years. Therefore further significant increase of the Si based solar cell efficiency could be achieved by combining III-V compounds and silicon. The problems of the III-V material growth on Si substrate as well as fabrication of effective III-V/Si heterojunction sub-cell should be solved for successful integration of III-V with Si. It means that the same III-V material should be used as a nucleation layer as well as a wide gap window (or even emitter) for III-V/Si heterojunction with low recombination rate at the interface.

Gallium phosphide (GaP) could fit both requirements. GaP has a band gap of 2.26 eV and has the smallest lattice mismatch with Si among III-V binary compounds (less 0.4 %) providing conditions for low defect density at the interface with the Si substrate. Therefore, GaP/Si heterojunctions are of great interest for III-V/Si multijunctions as in case of the lattice-matched concept where diluted nitrides (GaNAsP) are used for the top junctions [3] as well as in case of the metamorphic concept where GaAsP top cells are grown via a graded GaAsP buffer layer on the top of the GaP nucleation layer [4]. However, the commonly used techniques for the growth of GaP layers such as molecular beam epitaxy (MBE) and metal organic vapor-phase epitaxy (MOVPE) require high temperatures of 800-900°C at least at the initial stage for silicon oxide removing and surface reconstruction [5-9]. High temperatures affect the Si wafers quality and the properties of III-V/Si interface leading to low photovoltaic performance of GaP/Si heterojunctions obtained by epitaxy compared to the high efficiency a-Si:H/c-Si solar cells [3, 10]. The problem can be related to elastic stresses in the growing layer, which lead to the appearance of dislocations. Moreover, the use of high temperatures leads to inter-diffusion of group-III and -V atoms into Si and opposite, which act as dopants affecting the electrical properties of heterojunctions, and it can also promote the fast diffusion of species that can degrade the carrier lifetime in c-Si [11]. In this paper we study the electronic properties of GaP/Si heterojunctions growth using MBE.

2. Experiment

Epitaxial single-crystal GaP layers were grown by MBE (using Veeco Gen III) on silicon substrates with (100) orientation (4° cut-off towards (110)). After deoxidation and surface reconstruction at 800-900 °C a two step growth was used. First step is the nucleation with migration enhanced epitaxy (MEE) at 400 °C and in a second step MBE growth at 500-600 °C was performed [10]. Si and Be were used for GaP doping of n- and p-type, respectively. GaP/Si heterojunctions were fabricated on n- and p-type Si substrates. The isotype n-GaP/n-p Si heterojunction with n-p homojunction was formed by phosphorous diffusion in p-Si before n-GaP growth. The Si surface was exposed to P flux during 10 minutes at 500 °C.

To verify the temperature influence on the electronic properties of the GaP/Si heterojunction an amorphous GaP was deposited on Si by plasma enhanced atomic layer deposition (PE-ALD) at 350-380 °C. PE-ALD deposition was performed using the Oxford Plasmalab 100 PECVD (13.56 MHz) setup supplied with phosphine (PH_3) and trimethylgallium (TMG) lines for sources of phosphorus and gallium, respectively. Hydrogen was used as a gas carrier for TMG.

The layer parameters of the heterojunctions are presented in table 1. To check the electrical properties of the GaP/Si heterostructures indium dot contacts were deposited on top of the GaP layer. Contacts on the rear side of the Si substrates were formed by deposition of doped a-Si:H followed by evaporation of Ag.

Table 1. Samples parameters.

Sample	Technology / temperature (°C)	GaP doping level (cm^{-3})/thickness (nm)	Substrate type / doping levele (cm^{-3})
p-GaP/n-Si	MBE / 600	p (10^{19}) / 200	n / 10^{15}
n-GaP/p-Si	MBE / 560	n (10^{18}) / 200	p / 10^{16}
n-GaP/n-p Si	MBE / 600	n (10^{18}) / 800	p / 10^{16}
n-GaP/p-Si	ALD / < 380	n (unknown)/ 50	p / 10^{16}

3. Results

3.1. Heterojunction design

The transport properties of different heterojunction designs were analyzed in terms of the band diagrams. The calculated band diagram for p-GaP/n-Si and n-GaP/p-Si heterojunctions are presented in Fig. 1. According to literature results [12, 13] the valence band offset (ΔE_V) at the GaP/Si is in the range of 0.8-1 eV and thus forms a significant potential barrier for the holes, which could cause a serious transport limitation [14]. The calculated external quantum efficiency (EQE) with ΔE_V = 0.8 eV (Fig. 2a) predicts that in the case of the p-GaP/n-Si heterostructure the hole transport is completely blocked by the potential barrier. The EQE measurements for the fabricated p-GaP/n-Si structure confirm the limitation of the hole transport though the GaP/Si interface (Fig. 2b). Only holes generated in p-GaP contribute to the spectral response (Fig.2b). In contrary, in the case of the n-GaP/p-Si heterojunction no transport limitation was observed. Therefore only the p-type Si substrates may be used for solar cells. There are two types of heterojunctions that could be fabricated. The first one is an isotype n-GaP/n-Si/p-Si heterojunction with an n-p Si homojunction formed in Si by phosphorous diffusion. Conventionally P diffusion occurs during the GaP growth at high temperatures (above 750 °C) usually used for MOVPE. The MBE of GaP was performed at lower temperatures and relatively sharp P profile could be achieved. This creates a possibility to form an anisotype n-GaP/p-Si heterojunction, where GaP is used as the wide band gap emitter. Here both types of heterojunction were fabricated by MBE.

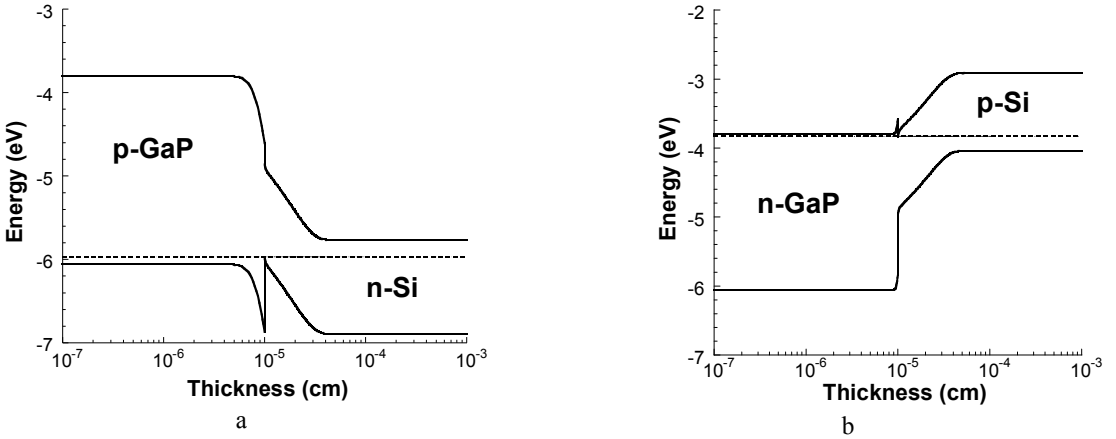


Fig. 1. Calculated band diagram for p-GaP/n-Si (a) and n-GaP/p-Si (b) heterojunctions.

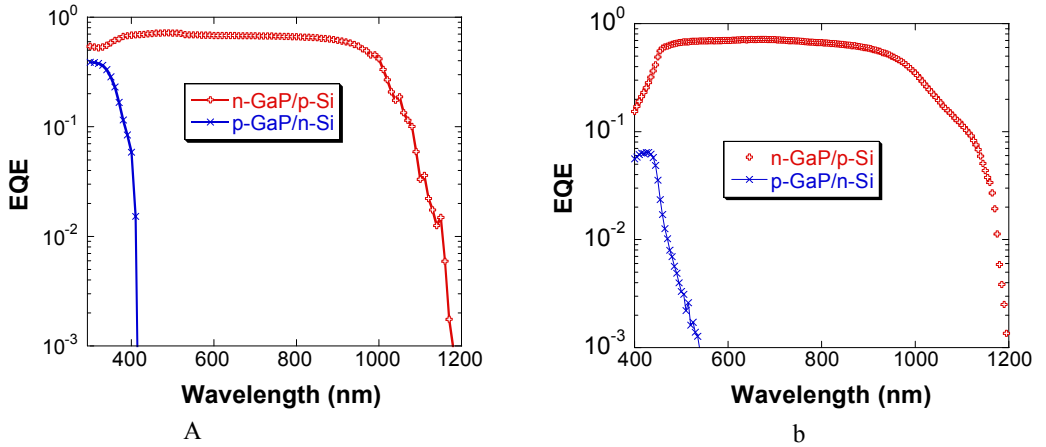
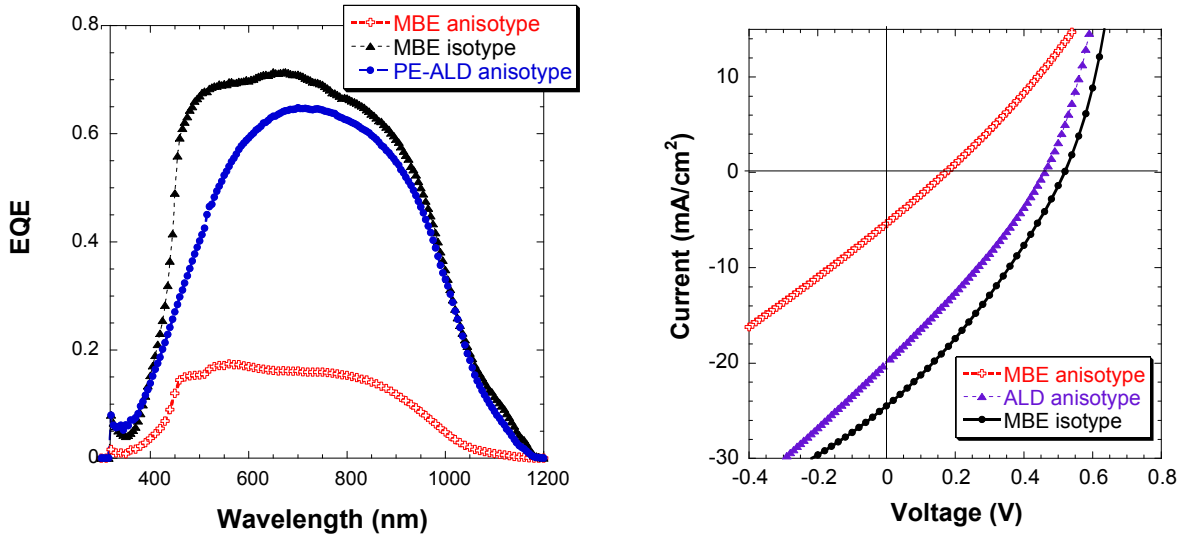


Fig. 2. Calculated (a) and measured (b) EQE for p-GaP/n-Si and n-GaP/p-Si heterojunctions.

3.2. Photoelectrical properties

The measured EQE spectra and I-V curves under AM1.5G illumination are presented in Fig.3 for both types of heterojunctions fabricated by MBE. The anisotype n-GaP/p-Si heterojunction grown by MBE has the lowest quantum efficiency and V_{OC} (0.2 V). The isotype n-GaP/n-Si/p-Si heterojunction has the highest performance with V_{OC} = 0.52 V. In comparison the anisotype n-GaP/p-Si heterojunction fabricated by PE-ALD has a V_{OC} value of 0.46 V and lower quantum efficiency in the short wavelength region due to the absorption in the amorphous GaP layer. Extremely low fill factor (FF) for all the samples is caused by non-optimized contacts. Indeed, no contact grid was used at front surface and no optimization of contact resistivity was performed for either side. Nevertheless, the strong difference for the two designs of GaP/Si heterojunction cells grown by MBE is surprising.



a b

Fig. 3. Measured EQE (a) and I-V curves under illumination (b) for anisotype n-GaP/p-Si heterojunctions fabricated by MBE and PE-ALD, and for isotype n-GaP/n-p Si heterojunction fabricated by MBE.

3.3. Computer simulation

In order to clarify the observed difference between anisotype and isotype heterojunctions numerical modeling was performed using AFORS-HET software [15]. The calculated band diagrams of the studied structures are presented in Fig.4. The main difference is that the space charge region is located in close proximity to the GaP/Si interface in case of the anisotype heterojunction while for the isotype structure they are separated by the (n) c-Si region (emitter). First, the influence of interface states on the solar cell performance was studied by introducing significant interface defect density (D_{it}) at the interfaces of both structures. The interface was described by introducing a very thin (d = 1 nm) defective Si layer between the Si and GaP. The defect distribution, g_{it}, in this defective layer was taken as constant through the bandgap, assuming donor/acceptor-like defects in the lower/upper half of the bandgap. The electron and hole capture cross-sections were set at 10^{-14} cm^2. The interface defect density, $D_{it} = g_{it} \times d$, was set to $D_{it} = 10^{12}$ cm^{-2}eV^{-1}. The calculated I-V curves under AM1.5 illumination, which are presented in Fig. 5a, do not exhibit any distinguishable difference between the anisotype and isotype heterojunctions. Therefore the interface states have the same influence for both types of heterojunctions. In a second simulation step, a thicker (100 nm) extremely defective Si layer with charge carriers lifetime (τ) of 5 ps was introduced between the Si substrate and the GaP layer. The I-V curves in this case are quite different (Fig. 5b). The value of V_{OC} for the anisotype heterojunction is strongly reduced compared to that of the isotype heterojunction. For the anisotype heterojunction the defects are located in the space charge region which leads to high recombination losses. In case of

the isotype heterojunction design the defects are in the highly doped n-Si emitter and therefore they have lower influence on the solar cell performance. Thus the simulations could explain the strong experimentally observed difference between the two types of heterojunctions by the presence of volume defects in Si near to the GaP/Si interface.

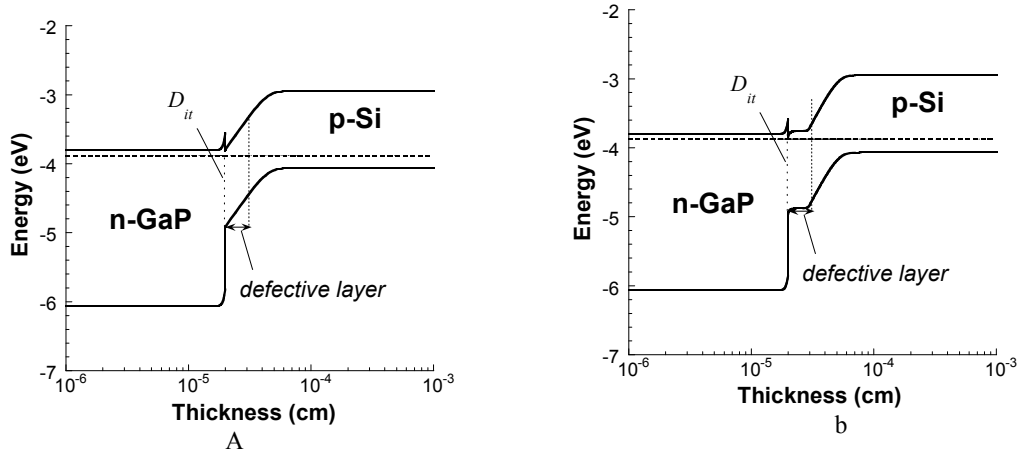


Fig.4. Calculated band diagrams for anisotype n-GaP/p-Si (a) and isotype n-GaP/n-p Si (b) heterojunctions. The position of 100 nm defective layer in Si near the interface is indicated.

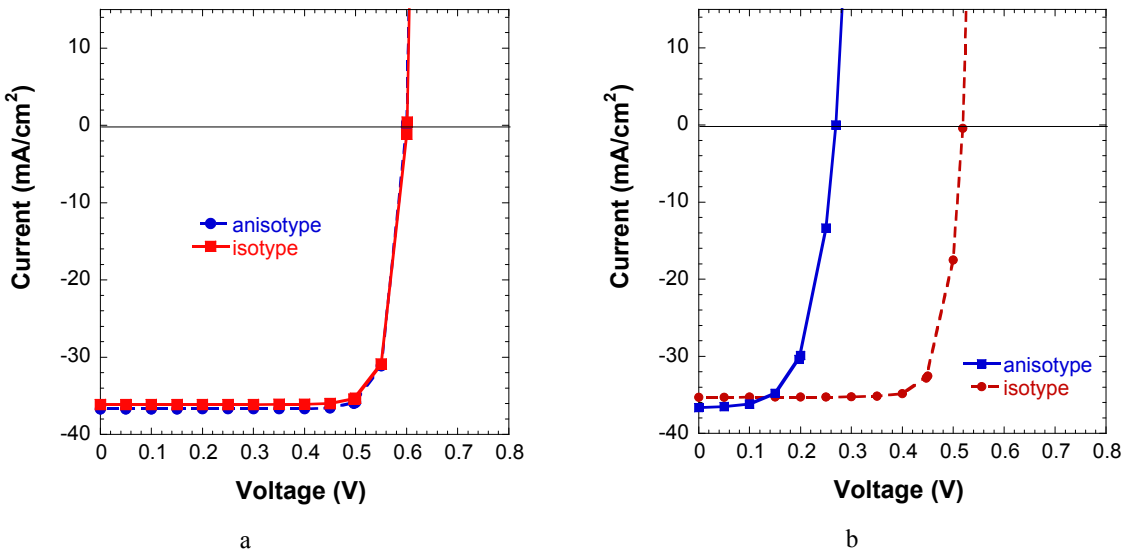


Fig.5. Calculated I-V curves under AM1.5G illumination for anisotype n-GaP/p-Si and isotype n-GaP/n-p-Si heterojunctions with D_{it} =10^{12} cm^{-2}eV^{-1} at the GaP/Si interface (a) and with 100 nm defective layer in Si near the interface (b).

3.4. Photoluminescence measurements

Photoluminescence (PL) is known to be a powerful tool for the characterization of interface properties in Si based heterojunctions [16, 17]. The radiative recombination of excess carriers in the volume depends on the effective charge carriers' lifetime, which is affected by volume and surface recombination. The PL signal from Si (at λ=1150 nm) decreases with increasing recombination rate at the GaP/Si interface. The PL measurements were

performed at room temperature with excitation at a wavelength of 778 nm (minimum absorption in GaP) using an Accent RPM Sigma PL system.

The PL measurements performed for the GaP/Si heterostructures fabricated by MBE and PE-ALD (at 600 and 350 °C, respectively) are presented in Fig. 6. The PL signal for the MBE GaP/Si structure drastically decreased compared to that of the Si substrate passivated by a-Si:H. The PL signal for the GaP/Si structure fabricated by PE-ALD at lower temperature is significantly higher compared to that of the MBE GaP/Si. We then removed the GaP layer by wet etching (using acid based etchant) from MBE and PE-ALD grown samples and passivated the silicon surface by a-Si:H . The intensity of the PL signal for the MBE sample remained at the same level while for the PE-ALD sample the PL intensity increased, approaching the initial Si wafer value. This proves that the carrier lifetime in silicon was degraded during the high temperature epitaxial growth. We should emphasize that initially all the Si substrates were similar (with the same charge carrier lifetime). However high temperatures used in MBE processes could lead to higher defect density in Si substrates. On the contrary the low temperature PE-ALD process did not affect the properties of the Si wafers. In order to verify if the degradation during MBE growth occurs in the Si wafer volume or just near the interface the Si substrate was further etched after GaP removing. The wet acid based etching was used to avoid any damage (in case of dry etching) or contamination (in case of alkali based etchant). The first 200 nm of Si were etched and then the Si surface was passivated again. The PL signal became closer to the substrate level (Fig. 6a) indicating that most of the created defects are located near the GaP/Si interface. The series of accurate etching with a step of 10 nm allowed us to conclude that most defects are located within the first 30 nm of Si for both isotype and anisotype GaP/Si heterojunctions.

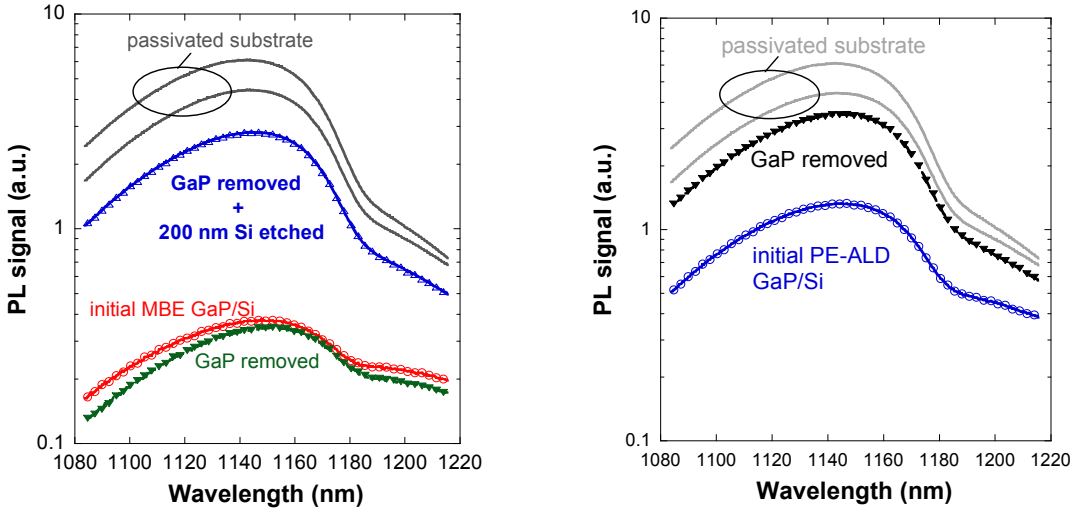


Fig.6. PL spectra for GaP/Si heterojunctions fabricated by MBE (a) and by PE-ALD (b) at the initial state; after GaP removing and passivation; after GaP removing 200 nm Si etching and passivation. The PL spectra of the passivated Si wafers are also presented.

3.5. DLTS measurements

Deep level transient spectroscopy (DLTS) is a powerful tool for defect characterization in semiconductors [18]. We just note that the DLTS signal is sensitive to the defects located in the space charge region. Increasing the reverse voltage filling pulse amplitude could extend the space charge region and therefore the information about defect profiling may be obtained. A homemade DLTS setup based on the Boonton 7200 capacitance bridge and Janis VPF-100 liquid nitrogen cryostat was used for GaP/Si defects characterization.

The measured DLTS spectra for isotype n-GaP/n-p Si heterojunctions at two reverse voltage pulses are shown in Fig. 7a. We should stress that the space charge region for this structure is somewhat far from the interface. The observed peaks with weak dependence on reverse voltage are associated with the defects in the bulk of Si wafers

(with concentration of about 10^{13} cm^{-3}). The precise identification of the defects is difficult because three or four peaks with different positions could fit the spectra. The DLTS spectra are likely to correspond to a mix of responses coming from transition metals like Ni, Cu or Fe, which presence in the Si wafer is expected.

The DLTS spectra of anisotype n-GaP/p-Si heterojunction where the space charge region is close to the interface (Fig. 7a) have strong dependence on reverse voltage. The spectrum at lower reverse voltage (-2 V) exhibits a response of defects (at 350 K) located near the interface with significantly higher concentration compared to bulk defects. Increase of reverse voltage (-3 V) leads to the extension of the space charge region and to a dramatic reduction of the defects response at 350 K, which confirms their location close to the GaP/Si interface.

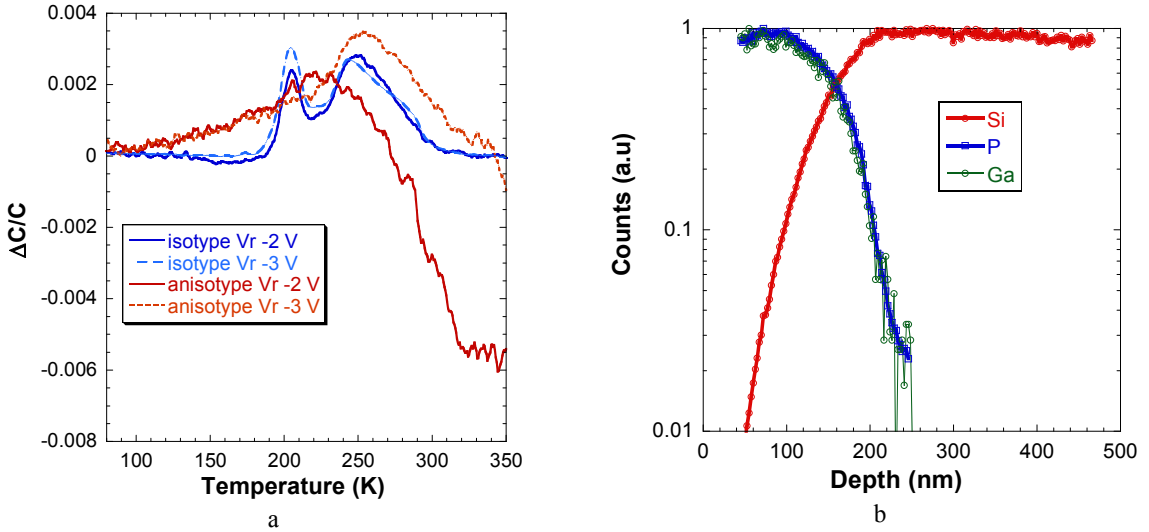


Fig.7. DLTS spectra for anisotype n-GaP/p-Si and isotype n-GaP/n-p Si heterojunctions fabricated by MBE (a); SIMS profile for anisotype GaP/Si heterojnction grown by MBE (b).

4. Discussions

A strong degradation of charge carrier lifetime in the Si substrate was observed after MBE GaP growth at temperatures higher than 500°C. The results of two independent measurements have demonstrated that defects, which obviously affect the lifetime, are located near the interface. On the other hand the deposition of GaP by PE-ALD at lower temperatures (< 380 °C) does not affect the Si wafer properties. The temperature dependence and localization of defects near the interface rather indicate the diffusion related origin of the defects. The SIMS profile (Fig. 7b) indicates that Ga and P have diffused to the depth of few tens of nanometers during the MBE GaP growth. This diffusion depth is in agreement with the estimation of defect region length by PL (30 nm). Thus the diffusion related nature of the defects formation in Si during GaP MBE growth seems to be the most probable.

5. Conclusions

The growth of monocrystalline GaP on Si substrates by MBE at 500-600 °C leads to the degradation of charge carrier lifetime in the Si wafer due to the creation of defects. The study performed by PL and DLTS has demonstrated that most defects are located in Si within ~30 nm near the GaP/Si interface. This defective layer in Si affects the solar cell performance of anisotype n-GaP/p-Si heterojunction due to strong recombination in the space charge region. The isotype n-GaP/n-p Si heterojunction exhibits better performance compared to the anisotype one because the defective layer is located in the n-Si emitter formed by intentional P diffusion. When amorphous GaP is deposited by PE-ALD at T < 380 °C no degradation of the charge carrier lifetime in Si is observed.

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References

[1] Masiko K, Shigematsu M, Hashiguchi T, Fujishima D, Kai M, Yoshimura N, Yamaguchi T, Ichihashi Y, Yaman-ishi T, Takahama T, Taguchi M, Maruyama E, Okamoto S. IEEE J. of Photovoltaics 2014; 4, 1433.
[2] Shockley W, Queisser HJ. Detailed balance limit of efficiency of p-n junction solar cells. Journal of Applied Physics 1961; 32, pp. 510-519.
[3] Geisz JF, Olson JM, Friedman DJ et al. 31th IEEE PVSC; 2005, p. 695.
[4] García-Tabarés E, García I, Rey-Stolle I, Algora C, Martín D. Integration of III-V materials on silicon substrates for multi-junction solar cell applications. Proceedings of the 8th Spanish Conference on Electron Devices; 2011, pp. 1-4.
[5] Sadeghi M, Wang S. J Cryst Growth; 2001, 227–228, 279.
[6] Wright SL, Kroemer H, Inada M. J Appl Phys; 1984, 55, 2916.
[7] André JP, Hallais J, Schiller C. J Cryst Growth; 1975, 31, 147.
[8] Samuelson L, Omling P, Grimmeiss HG. J Cryst Growth; 1984, 68, 340.
[9] Olson JM, Al-Jassim MM, Kibbler A, Jones KM. J Cryst Growth; 1986, 77, 515.
[10] Sobolev MS, Lazarenko AA, Nikitina EV, Pirogov EV, Gudovskikh AS, Egorov AY. Semiconductors; 2015, 49, 559.
[11] Varache R, Darnon M, Descazeaux M, Martin M, Baron T, Muñoz D. Energy Procedia; 2015, 77, 493.
[12] Hannes W et.al. J Appl Phys; 2014, 115, 044508.
[13] Isao S et. al. Applied Physics Express; 2008, vol. 1, nr. 9.
[14] Gudovskikh AS, Kleider JP, Kalyuzhnyy NA et al. Band structure at heterojunction interfaces of GaInP solar cells. Sol Energy Mat and Solar Cells; 2010, 94, p. 1953–1958.
[15] Varache R, Leendertz C, Gueunier-Farret ME, Haschke J, Muñoz D, Korte L. Investigation of selective junctions using a newly developed tunnel current model for solar cell applications. Sol Energy Mat and Solar Cells; 2015, 141, 14–23.
[16] Tardon S, Rösch M, Brüggemann MR, Unold T, Bauer GH, J Non-Cryst Solids; 2004, 338-340, 444.
[17] Bauer GH, Tardon S, Rösch M, Unold T. Phys Status Solidi (c); 2004, 1, 1308.
[18] Lang DV, J Appl Phys; 1974, 45, 3023.