



A General gm/Id Temperature-Aware Design Methodology Using 180 nm CMOS up to 250 °C

João R. Raposo de O. Martins, Francisco de Oliveira Alves, Pietro Maris Ferreira

► To cite this version:

João R. Raposo de O. Martins, Francisco de Oliveira Alves, Pietro Maris Ferreira. A General gm/Id Temperature-Aware Design Methodology Using 180 nm CMOS up to 250 °C. Journal of Integrated Circuits and Systems, 2022, 17 (1), pp.1 - 9. <10.29292/jics.v17i1.552>. <hal-03689553>

HAL Id: hal-03689553

<https://centralesupelec.hal.science/hal-03689553v1>

Submitted on 7 Jun 2022

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



HAL Authorization

A General g_m/I_D Temperature-Aware Design Methodology Using 180 nm CMOS up to 250 °C

João R. R. O. Martins^{†*}, Francisco Alves[†], Pietro M. Ferreira[†]

[†] Université Paris-Saclay, CentraleSupélec, CNRS, Lab. de Génie Électrique et Électronique de Paris, 91192, Gif-sur-Yvette, France.

[†] Sorbonne Université, CNRS, Lab. de Génie Électrique et Électronique de Paris, 75252, Paris, France.

* X-FAB France, 91100, Corbeil-Essonnes, France

email: Joao-roberto.raposo-de-oliveira-martins@xfab.com, francisco.alves@u-psud.fr, maris@ieee.org

Abstract— The advent of the Internet-of-Things brings new challenges in circuit design. The presence of circuits and sensors in harsh environments brought the need for methodologies that account for them. Since the beginning of the transistors, the temperature is known for having a significant impact on performance, and even though very low temperature sensitivity circuits have been proposed, no general methodology for designing them exists. This paper proposes an extension of the methodology presented in [15], generalizing the g_m/I_D technique for designing temperature-aware circuits that can be used either on measurement data, analytically, or based on simulation models. This model is validated using measurements up to 250 °C of X-FAB XT018 transistors and later with a Voltage-Controlled Oscillator circuit design example.

Index Terms— Temperature-aware, gm/Id, SOI, harsh environments, smart vehicles, Voltage Controlled Oscillator

I. INTRODUCTION

Smart sensing and positioning have gained increasing attention in the last few years. Smart Vehicles sensing must efficiently locate, sense, and communicate with other nearby devices, considering the working environment [1]. For obvious reasons, circuit design and specification are regulated by many strict security and safety standards. The temperature range is arguably the most demanding environmental challenge for electronics in the automotive industry [2], and aircraft [3].

Literature has proposed some solutions for low temperature coefficient oscillators. Ottaviani et al. evaluate temperature variations on inductors and capacitors components for high-frequency and high-temperature GaN-based oscillators [4]. However, wide band-gap materials having a higher production cost hinders the integration of digital circuits on-chip, an essential feature of smart sensing. Schwartz and Ponchak propose a 1 GHz SiC Clapp oscillator working at 200 °C [5]. However, no frequency temperature stabilization is proposed. Shanmugalingam et al. propose a digital supply voltage modulation scheme to compensate for the temperature effects on a 5-stage ring oscillator [6]. Shin et al. propose a diffusion doping-based method for controlling the frequency temperature coefficient for a MEMS resonator achieving smaller than dozens ppm/°C [7]. The result is validated at different resonant modes, and crystalline orientations maximum frequency variation on a reduced maximum surface is of 0.29 mm².

In [8], a passive LC-VCO with a low temperature coefficient is achieved using an additional PLL loop filter and auxiliary varactors. However, the analyzed temperature range is limited to 80 °C. Besides, passive inductors and the high values of resistors and capacitors are a limiting factor for certain technology nodes and considerably increase the silicon surface. In [9], a PLL with a digital-controlled oscillator is proposed with an external calibration circuit implement on an FPGA to compensate the temperature drift. Published works often rely on wide-bandgap transistors or feedback control systems to stabilize the VCO, increasing power consumption and silicon area.

The temperature has always been a concern for analog design. Special outside bias conditions called zero temperature coefficient (ZTC), transistor parameters vary greatly with temperature. In literature, the first ZTC bias point, the I_{DZTC} , has been explored by Park *et. al* [10]. In his work, Park proposed a temperature-stable output frequency for a ring oscillator. Later, using the UICM model [11], Toledo et al. have proposed g_{mZTC} [12]. Using g_{mZTC} , an OTA and an OTA resistance presenting respectively low temperature sensitivity for the transconductance, and equivalent impedance were designed.

In [13] first general considerations for biasing transistors using the g_m/I_D methodology [14] for high-temperature circuits. The paper proposes four different designs achieving an estimated temperature coefficient from 2917 ppm/°C, to 4674.16 ppm/°C, for the gain and from 2686.32 ppm/°C to 3719.43 ppm/°C for the transition frequency. Those parameters were obtained from measurement data from 27 °C to 300 °C. However, no ZTC point was exploited, nor were analytical expressions for the different g_m/I_D temperature behaviors discussed.

This paper extends the proposals of [15, 16] in a general temperature-aware framework using the g_m/I_D methodology. This work introduces two new parameters G_g and G_d that are so-called "temperature normalized g_m/I_D parameters" validated from -40 °C to 175 °C using simulations and measurement data of from XT018 a 0.18 μm node from X-FAB. It is important to highlight that even though higher temperatures are explored in research, producing an industrial node for temperatures higher than 175 °C are limited by the back end of line (BEOL). The methodology was used to design an OTA with temperature-stable differential gain [15] and a Voltage Controlled Oscillator [16]. However, no straightforward indications are given for generic circuits.

This paper extends the proposition of [15] presenting new measurement data for transistors at 225 °C and 250 °C, showing a possible general recipe for making a temperature-aware circuit and introducing a new tool for temperature analysis on integrated circuits. The presented recipe is then applied for the VCO circuit presented at [16] obtaining the same results with a more general framework the one proposed on [15].

This brief is organized as follows. Section II briefly presents the normalized temperature g_m/I_D coefficients and their different properties. Section III uses the previously developed temperature models and generalizes their usage in an analog circuit. Section IV applies the technique in the VCO presented in [16] and Section V concludes and summarizes this brief.

II. THE TEMPERATURE NORMALIZED g_m/I_D ZTC POINTS

The temperature normalized g_m/I_D parameters were introduced in [15] as an adaptation to the g_m/I_D methodology. This modification allows the designer to take into account temperature effects in an early design stage [15]. The proposed parameters G_g and G_d are illustrated on Fig. 1 extracted from measurement data from 27 °C to 250 °C for 2 different transistor lengths ($L = 180$ nm, $W = 10$ μm). The G_g characteristics were obtained from the $I_D \times V_{GB}$ characteristics at the different temperature, g_m was obtained by a 6-order BSpline interpolation. The G_d was obtained by fitting the UICM model with drain induced barrier lowering (DIBL) and channel length modulation (CLM). The G_d extraction process will be better detailed in the next section.

The G_g and G_d definitions and their respective ZTC biasing conditions are given by

$$G_g = \phi_T \cdot \frac{g_m}{I_D}, \quad (1)$$

$$V_p|_{G_{gZTC}} = \frac{\alpha_{th} \cdot T}{\eta}, \quad (2)$$

$$G_d = \frac{g_{ds}}{I_D} \phi_T, \quad (3)$$

$$\left(V_p|_{G_{gZTC}} - V_p|_{G_{dZTC}} \right) = - \frac{8\eta\phi_T^2}{\alpha \cdot (V_0 + V_{DS})\sigma} \approx 0, \quad (4)$$

where ϕ_T is the thermal voltage; α_{th} the linear temperature coefficient for the transistor threshold voltage (V_{th}); η the subthreshold non-ideality factor; V_p the pinchoff voltage; σ the DIBL coefficient; and α and V_0 CLM parameters as explained in [17].

A. Zero Temperature Coefficients (ZTC) Points

Most temperature-aware circuit designs use either mutual cancellation of different parameters [18], or ZTC biases [12] to achieve a low temperature coefficient of a given parameter. Both strategies come with different advantages and drawbacks.

The first relies on regional approximations of MOSFET current characteristics, usually from the weak inversion.

Even though it presents very good results, regions in which no regional approximations exist, such as the moderate inversion, the application of this technique is very limited.

Before introducing the temperature normalized g_m/I_D ZTC points, the existing ZTC points had two main drawbacks. First is the ZTC bias condition dependency on the mobility temperature coefficient, which needs greater investigation with the introduction of ballistic transport in smaller nodes [19]. Second, the dependency of the ZTC condition on multiple transistor voltages or currents cannot be guaranteed to be temperature stable.

The relative variation $(|p(T) - p(27^\circ\text{C})|/p(27^\circ\text{C}))$ of the g_{mZTC} ; I_{DSZTC} ; and G_{gZTC} in respect to temperature and V_D while keeping V_S constant is here shown on Fig. 2. The results were calculated using the UICM for a large transistor with doping concentration of $5 \times 10^{17} \text{ cm}^{-3}$ and an oxide thickness of 4 nm implemented in MOSLab.jl [20]. The parameters ZTC were found using Newton's method on the temperature derivative obtained using automatic differentiation in Julia. It can be seen that in comparison to g_{mZTC} and I_{DSZTC} , which may vary up to 40 % the G_{gZTC} , have a variation of less than 4 %. This ZTC variation was obtained in a large transistor model, not considering small geometry effects, such as DIBL, CLM, velocity saturation considering those phenomena may impact even more the ZTC variation on the different bias conditions.

B. Capacitive ZTC's

The existence of ZTC points is not limited to transistors small signal parameters. In [16] new ZTC points for the transistor total gate capacitance and gate to source capacitance (C_{gg} , C_{gs}) were also proposed. Figure 3 illustrates the total gate capacitance temperature sensitivity extracted from measurement data from 27 °C to 175 °C. It is noticeable that the temperature behavior at depletion and inversion follows closely the G_g temperature sensitivity illustrated on Fig. 3(b). This result can be interpreted by rearranging the G_g expression given by the UICM model as:

$$G_g = \frac{1}{\eta \cdot \left(\frac{q_{is} + q_{id}}{2} + 1 \right)} = \frac{1}{\eta (\bar{q}_i + 1)} \quad (5)$$

where \bar{q}_i is the average channel inversion charge; q_{is} the inversion charge on the source; q_{id} the inversion charge on the drain; and η the sub-threshold non-ideality factor. Since η has negligible temperature variation [15], the G_g ZTC points occur on the same bias as the ZTC of the average channel inversion charge being also the main parameter that defines different transistor capacitance.

A second ZTC point can also be found on the total gate capacitance at the accumulation region. This ZTC point can be explored at RF circuits in which non-quasi-static effects may change the C_{gg} characteristics dramatically at the end of depletion and inversion levels. The ZTC bias condition for the accumulation region can be found by

$$V_{GB} = \alpha_{fb} T + V_{fb} - (2 \ln(\gamma) + 1) \phi_t \quad (6)$$

$$\alpha_{fb} = \frac{1}{T} \left(\frac{E_G(T=0)}{2 \cdot q} - \phi_F \right), \quad (7)$$

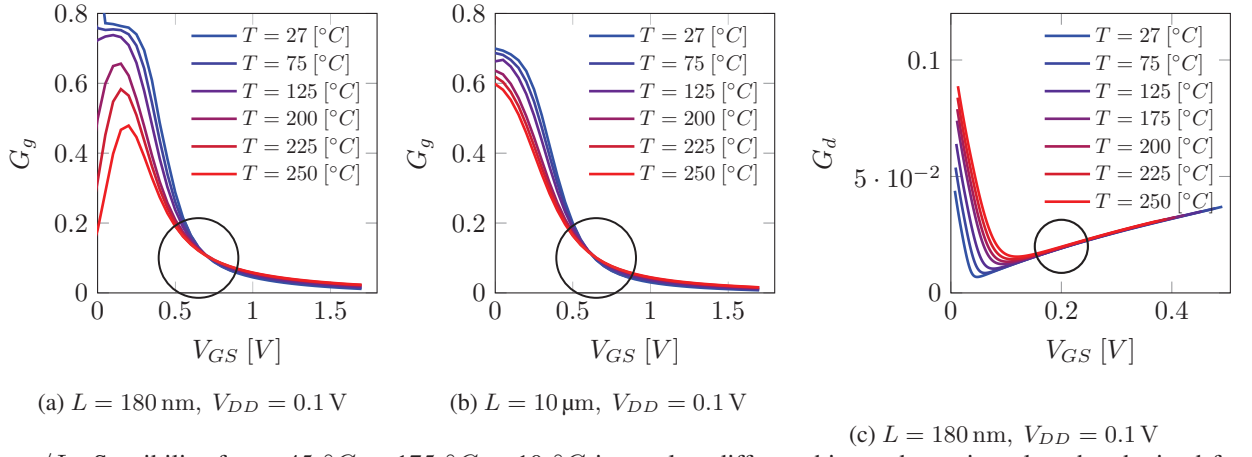


Fig. 1: g_m/I_D Sensibility from -45°C to 175°C at 10°C interval at different bias and transistor lengths obtained from Virtuoso Spectre simulations for a NMOS transistor with $W = 10\ \mu\text{m}$.

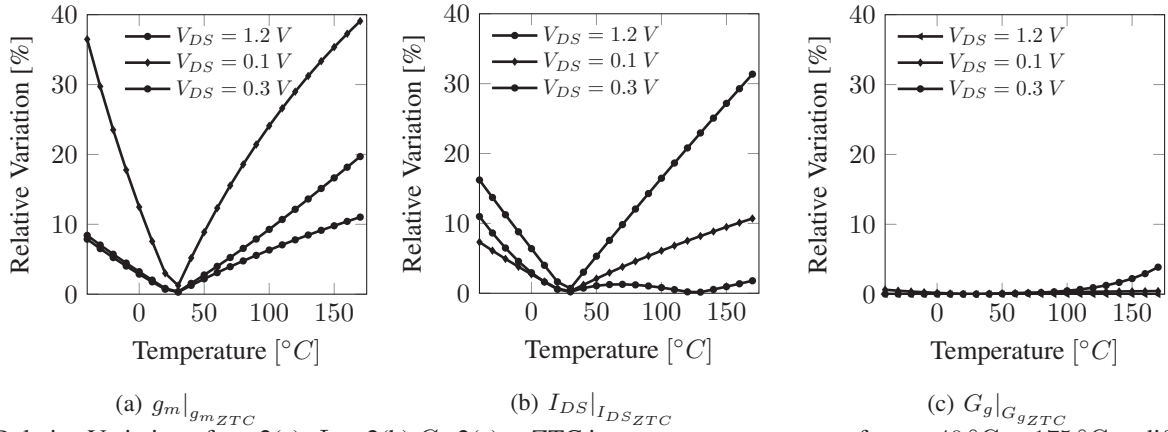


Fig. 2: Relative Variation of g_m 2(a), I_{DS} 2(b), G_g 2(c) at ZTC in respect to temperature from -40°C to 175°C at different to V_D biases

for Silicon, the extrapolated bandgap at 0 K ($E_G(T=0)/q$) is 1.12 eV; for usual doping levels, the bulk Fermi level ϕ_F is not very apart from the middle gap ($E_G(T=0)/2 \cdot q$) making the flat-band voltage (V_{FB}) temperature derivative very low and therefore the accumulation ZTC point very close to V_{FB} and mostly dependent of the substrate doping.

The same ZTC point found on G_g and C_{gg} was also found on C_{gs} , reinforcing the hypotheses of the close relationship between the G_g ZTC and the average channel inversion charge ZTC on transistors. The ZTC bias condition is found by

$$V_p|_{C_{gs}ZTC} = \frac{\alpha_{th} \cdot T}{\eta}. \quad (8)$$

III. A GENERAL TEMPERATURE-AWARE FRAMEWORK

Even though the ZTC points are good starting points for the temperature desensitization of a specification P depending on g_m , I_{DS} and more recently g_m/I_D , g_{ds}/I_D , C_{gg} and C_{gs} . The biasing of the transistors related to P at ZTC is often not possible. This can occur either by limitations of the topology or by transistors having to be biased at two conflicting ZTC point.

This limitation can be solved by combining the two previous approaches for temperature desensitization, ZTC bias

points and mutual cancellation of temperature coefficients. According to the Buckingham Pi-Theorem [21], a parameter of interests P , that depends on variables $x_i \in x$ can be written as:

$$P(x) = \prod_{i=1}^N y_i^{a_i} \cdot g(\pi), a \in \mathbb{Q}^N, \pi \in \mathbb{G}^M \quad (9)$$

where y is a vector of the circuit parameters with dimensions; a a vector of rational numbers; and π a vector of unit-less quantities; N and M are such $N + M$ is the total number of parameters of x .

Intuitively, (9) shows that the equation arriving at parameter P with a specific unit must have the same unit as P . This unit equality can only be achieved with the combination of rational powers of the parameters since, for example, $\exp(1\text{ [V]})$ has no defined unit. Therefore, the equation of P must have the form described by (9) where the product must have the same unit of P , and g must be dimensionless.

Notice that the temperature normalized g_m/I_D parameters (G_g, G_d) are indeed dimensionless quantities. Therefore by rewriting the parameter of interests with π being a vector containing the temperature normalized g_m/I_D parameters of the different transistors. The temperature sensitivity of P can

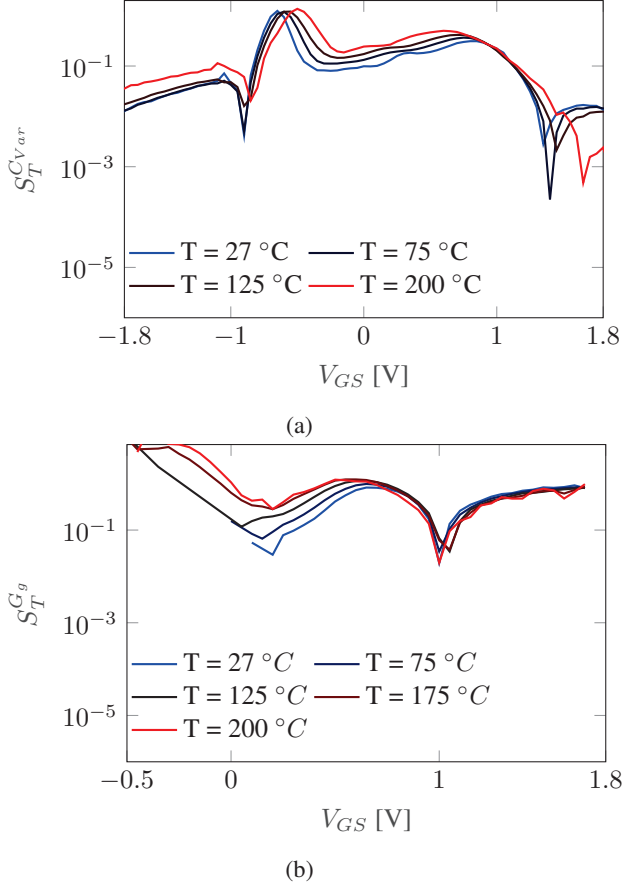


Fig. 3: Extracted sensitivity extracted from measurement data for C_{var} (a) and G_g (b).

be obtained by

$$S_T^P = \sum_{i=1}^N a_i \cdot S_T^{y_i} + S_T^{g(G_{g_i}, G_{d_i})} \quad (10)$$

and therefore the ZTC condition can be obtained by

$$\sum_{i=1}^N a_i \cdot S_T^{y_i} = -S_T^{g(G_{g_i}, G_{d_i})} \quad (11)$$

The condition on (11) can be obtained by fixing the parameters y at a point of low temperature sensitivity such as with the ZTC conditions of G_g , G_d and the temperature sensitivity approximations of these quantities. Thus, the parameter ZTC can be achieved. The choice of y_i parameters can be done by using lookup tables of the different parameters temperature sensitivities. Otherwise, if the temperature-dependent parameters of y are currents and intrinsic MOSFET capacitances, then the proposed ZTC points and temperature sensitivity approximations can be used.

Conversely, the temperature desensitization may be depicted in a more analytical analysis on, let:

- $P(g_m/I_{D_1}, \dots, g_m/I_{D_N}, g_{ds}/I_{D_1}, \dots, g_{ds}/I_{D_N}, C_1, \dots, C_N, I_{DS_1}, \dots, I_{DS_N})$ be the parameter of interest
- Where g_m/I_{D_i} , g_{ds}/I_{D_i} , I_{DS_i} are respectively the g_m/I_D , g_m/g_{DS}
- I_{DS} of the i th transistor and C_j a capacitance, possibly from a transistor.

- If P can be expressed as a first-order polynomial ratio, or represented by a Padé approximation at the vicinity of G_{gZTC} , i.e., P is analytical, as:

$$P = \frac{N(L)}{D(L)}, N \in \mathbb{P}^1, D \in \mathbb{P}^1 \quad (12)$$

where L is a vector containing all the parameters of P . By multiplying $N(L)$ and $D(L)$ by ϕ_T , considering no cross products in N and D , P can be expressed by:

$$P = \frac{n(G_g, G_d) + \phi_T \cdot p(I_{DS}, C)}{d(G_g, G_d) + \phi_T \cdot q(I_{DS}, C)} \quad (13)$$

- Then, the temperature sensitivity of P can be calculated by:

$$\begin{aligned} S_T^P &= S_T^{n+\phi_T p} - S_T^{d+\phi_T q} \\ &= \frac{\phi_T \cdot p S_T^n + n \cdot (1 + S_T^p)}{n + \phi_T \cdot p} - \frac{\phi_T \cdot q S_T^d + d \cdot (1 + S_T^q)}{d + \phi_T \cdot q} \end{aligned} \quad (14)$$

- If p and q are such the $I_{DS} = I_{DSZTC}$ and $C = C_{ZTC}$ are biased at ZTC, P achieves ZTC when:

$$\frac{\phi_T \cdot p S_T^n + n}{n + \phi_T \cdot p} = \frac{\phi_T \cdot q S_T^d + d}{d + \phi_T \cdot q} \quad (15)$$

where q and p are constants. By using the proposed approximations for the temperature sensitivity and values for the parameters at ZTC vicinity, a value of G_g and σ (DIBL coefficient) can be obtained for each transistor. With the help of a lookup table or the parameters (σ_0, σ_1, m) relating σ and L , the sizing of different transistors can be analytically obtained for the desired P ZTC point.

IV. VCO TEMPERATURE ANALYSIS EXAMPLE

To give an example of the proposed general temperature-aware design methodology one may design a active inductance Voltage Controlled Oscillator (VCO). First by evaluating the temperature behavior as in [16] and then the proposed general technique comparing the obtained results. Lu et al. presented a very wide tuning range LC-based (VCO) with an active inductance and low noise performance [22]. Figure 4 illustrates the VCO under analysis, composed by an active inductor (L_{active}), a MOS capacitor (C_{var}), and a negative impedance (G_{comp}).

The active inductance L_{active} , controlled by V_{ctrl1} , allows a very wide tuning range. However, it can present a large temperature variation [23]. The tunable MOS varicap C_{var} is controlled by V_{ctrl2} . The G_{comp} works as a negative resistance to nil the real part of the LC impedance and enforce oscillations. The LC tank resonance frequency gives the oscillation frequency:

$$F_{osc} = \frac{1}{2 \cdot \pi \sqrt{L_{eq} \cdot C_{var}}} \quad (16)$$

To evaluate the oscillation frequency temperature sensitivity, one may use the sensitivity operator, defined as $S_x^{f(x)} = \partial f(x) / \partial x \cdot x / f(x)$, from [15]

$$S_T^{F_{osc}} = S_T^{L_{eq}} + S_T^{C_{var}} \quad (17)$$

approximations for G_g and $S_T^{G_g}$ values at the ZTC proximity, given in [15] (28) can be approximated by

$$S_T^{L_{eq}}(G_{d_5}) \approx - \left(\left(\frac{T \cdot \alpha_{th}}{V_{p_5} \cdot \eta} - 1 \right) \frac{V_{p_5}}{4 \cdot \phi_T} \left(\sigma - \frac{\sigma^2}{(1-\sigma)} \right) \right) + 2\beta_\mu - 2, \quad (29)$$

$$S_T^{L_{eq}}(G_{d_5}) \approx \frac{\sigma(1-2\sigma)}{4\phi_T(1-\sigma)} V_p - \frac{q\alpha\sigma(1-2\sigma)}{4\eta k_B(1-\sigma)} + 2\beta_\mu - 2 \quad (30)$$

Equation (30) shows a linear relation between $S_T^{L_{eq}}(G_{d_5})$ and V_p that in this technology present a small linear coefficient. Therefore, for some range of V_{ctrl1} the equivalent inductance temperature sensibility can be considered as almost constant.

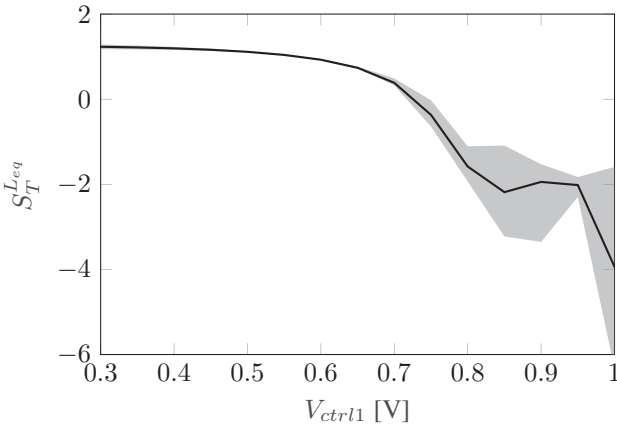


Fig. 5: Active Inductance equivalent inductance range (gray) and mean (solid) at different control voltages and temperature from -40°C to 175°C .

Fig. 5 illustrates the equivalent inductance sensitivity range from temperatures ranging from -40°C to 175°C . This figure shows a ZTC point of the average temperature sensitivity at $V_{ctrl1} \approx 0.7$ V. However by biasing M_5 in ZTC, the VCO loses its frequency control characteristics. Fig 5 also shows an almost constant temperature sensitivity around 1.3 in the region from V_{ctrl1} between 0.3 and 0.6 V. This constant temperature sensitivity can be compensated by the C_{var} temperature sensitivity using (18) to achieve a frequency ZTC point and still allow for VCO control as presented on [15].

B. Active Inductance Temperature Analysis - General Framework

The same analysis did on the last section can be done using the general framework proposed in this paper. Notice that (23) can be rewritten as:

$$L_{eq} = \frac{\phi_t^2 C_{tot}}{I_{DS}^2} \frac{1}{G_{d_5}(2G_{g_1} + rG_{g_3} - G_{d_5})} \quad (31)$$

where the term $C_{tot} = C_{gs1} + C_{gs3}$, and its temperature sensitivity can be calculated as:

$$S_T^{C_{tot}} = \frac{C_{gs1} S_T^{C_{gs1}} + C_{gs3} S_T^{C_{gs3}}}{C_{gs1} + C_{gs3}}. \quad (32)$$

Notice that on (31), the term $\phi_t^2 C_{tot}/I_{DS}^2$ has units of [H] and the second term is dimensionless and a function of only the temperature normalized g_m/I_D parameters. By biasing transistors M_1 and M_3 in G_{gZTC} , (32) becomes zero, since C_{gs} and G_g shares the same ZTC bias condition. Therefore, the vectors a and y described in (10) are given by

$$y = \begin{bmatrix} \phi_t \\ I_{DS} \\ C_{gs1} \\ C_{gs3} \end{bmatrix}, \quad a = \begin{bmatrix} 2 \\ -2 \\ 0 \\ 0 \end{bmatrix} \quad (33)$$

making the temperature sensitivity of L_{eq} around the ZTC of G_{d_5} equal to

$$S_T^{L_{eq}} = 2 - 2 \cdot S_T^{I_{DS}} \quad (34)$$

notice that the obtained result is similar to the one obtained in (25), however, in a much more direct way than the previous published one. Besides, the sensitivity can also be calculated using the measurement data or using lookup tables.

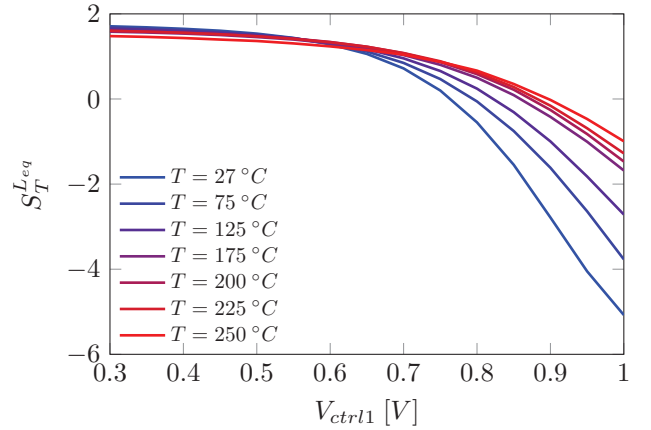


Fig. 6: Active Inductance equivalent inductance sensitivity obtained from measurement data with the temperature ranging from 27°C to 250°C .

Figure 6 shows the estimated temperature sensitivity for the active inductance when obtained from measurement data with the temperature ranging from 27°C to 250°C ($S_T^{G_{g_5}} \approx 0$). The drain current temperature derivative was obtained using a cubic BSpline interpolation for I_{DS} current at a given bias and the different temperatures.

The overall result matches with those obtained from Virtuoso Spectre simulations having an almost constant sensitivity region from $0.3\text{ V} < V_{ctrl1} \leq 0.6\text{ V}$ and a decreasing region for higher temperatures. It is important to clarify that since the sensitivity does not change with the multiplication of I_{DS} by a constant, by disregarding small geometry effects, the results are expected to be the same for any transistor sizing. For this matter the transistor used for the temperature sensitivity extraction was a 10

$0.18\text{ }\mu\text{m}/\mu\text{m}$. Besides, transistor arrays (series and parallel combinations) could be used to achieve any equivalent transistor aspect ratios with the same characteristics of a single transistor extracted.

V. VCO PLS RESULTS

To achieve F_{osc} ZTC while maintaining tuning range, the active inductance was biased with G_g ZTC for transistors M_1 and M_3 , and the MOS varicap was biased with a V_{ctrl2} of 1.3 V, making the V_{BG} equal 0.4 V when the source voltage is $V_{DD}/2$ and temperature sensitivity is -1.3. The maximum real part of the equivalent impedance seen from the parallel of C_{var} and L_{active} is shown on the Fig. 7. Post-layout simulation results achieve a maximum value of 600 Ω .

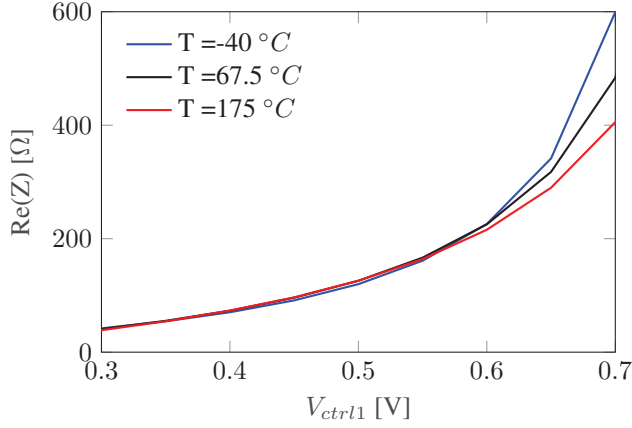


Fig. 7: PSL Real Part from active inductance impedance for V_{ctrl1} at the tuning range and different temperatures.

The G_{comp} network was designed to have a negative resistance bigger than 600 Ω ($g_m/I_{D7} = 5.95$ at $27^\circ C$) and the M_{10} , M_9 ($W \times L = 200\mu m \times 300nm$) sizes were adjusted for L-Band range. Figure 8 presents the oscillation frequency and the temperature variation of the circuit.

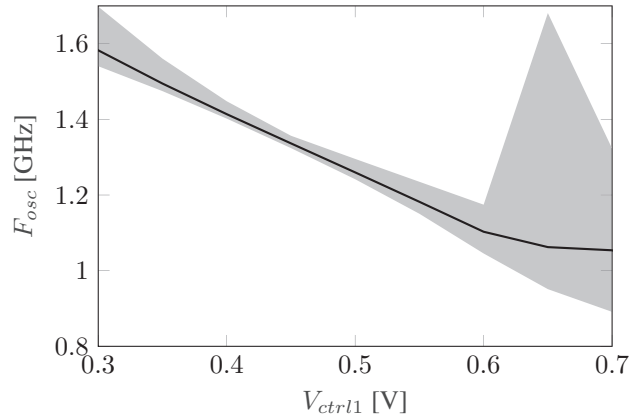


Fig. 8: PSL Oscillation frequency range (gray) and mean (solid) at different control voltages and temperature from $-40^\circ C$ to $175^\circ C$.

The frequencies presented in Fig. 8 are designed for a 10% head-up in order to account for the latter parasitic capacitors on the layout. The final circuit layout is presented in Fig. 9 having an area of $163.5 \times 190 \mu m^2$. For impedance matching two common-source output buffers with 50 Ω drain P+ non-salicated poly resistors presenting its 40 ppm/ $^\circ C$ resistance temperature coefficient, see details in Fig. 9. Power supply planes were made to decrease line resistance and increase bypass capacitance. All trace widths were drawn to minimize electromigration effects.

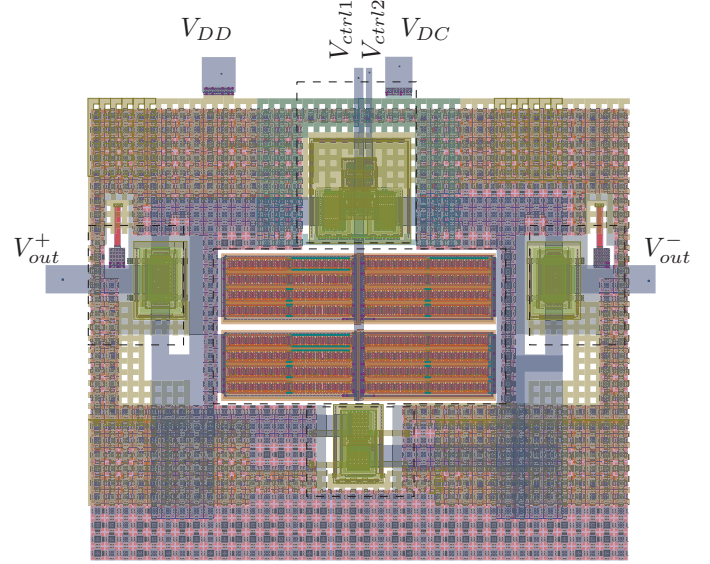


Fig. 9: Temperature-Aware VCO Layout, presenting an area of $163.5 \times 190 \mu m^2$, is rendered using icLayoutRender tool [24].

In order to compare the temperature-aware design with the proposition in [22], Fig. 10 shows the temperature coefficient of the circuit from [22] called "Traditional" ($g_m/I_{D1} = 9.9$, $g_m/I_{D3} = 9.8$, $g_m/I_{D7} = 7.8$ at $27^\circ C$) and the results presented in this paper.

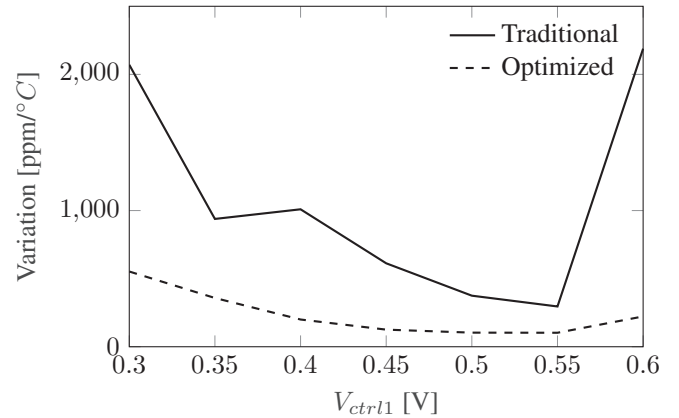


Fig. 10: Frequency Temperature coefficient comparison between [22] and this work.

The presented work shows an overall zero temperature coefficient, with a temperature coefficient reduction between 2.62 to 9.84 times better than the more traditional design and a mean temperature coefficient of 237.8 ppm/ $^\circ C$. It is important to point out that the traditional circuit does meet the oscillation condition for some V_{ctrl2} values at low-temperature and low V_{ctrl1} or high-temperature and high V_{ctrl1} .

To evaluate the process and mismatch variations and their consequences on the circuit temperature behavior, a 41-point Monte Carlo simulation was made for 9 V_{ctrl1} points and 11 temperature points, in a total of 4059 simulations. Since this work's goal is to account for reliability, all results will be presented on the worst-case Monte Carlo points. The mean and

3σ variation over temperature and the maximum frequency temperature variation is shown in Fig. 11.

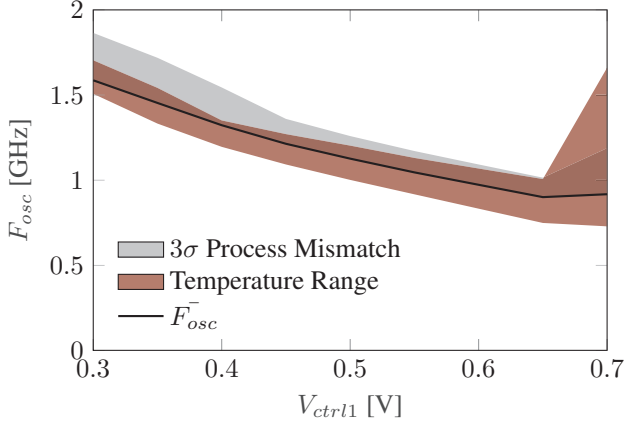


Fig. 11: Monte Carlo Results for the oscillation frequency of the proposed VCO.

The Monte Carlo results show a temperature variation smaller than the mean 3σ variation compatible with electric simulations. Such results highlight that the temperature awareness is kept even with process and mismatch variations. The final VCO present a worst-case phase noise of -60 dBc/Hz at 100 kHz frequency offset, a worst-case power consumption varying from 70 mW to 54 mW and a negative temperature coefficient. Since the oscillator is targeted to be used in a transmitter, where it will operate in only one frequency per transmission, the figure of merit is given by:

$$\text{FOM} = \left| L(\Delta f) + 20 \log \left(\frac{\Delta f}{f_0} \right) + 10 \log \left(\frac{P}{1 \text{ mW}} \right) \right|, \quad (35)$$

where $L(\Delta f)$ is the phase noise with a frequency offset of Δf ; f_0 is the oscillation frequency; and P the power consumption. The circuit presents a mean FOM over temperature and control voltage of 131 dB. The typical FOM values are compatible with the state of art.

VI. CONCLUSION

A low-temperature coefficient VCO suitable for L-band simulated a temperature from -40°C to 175°C and a strong indication that the circuit works up to 250°C . The proposed circuit presents a mean temperature coefficient of 237.8 ppm/ $^\circ\text{C}$ from -40°C to 175°C and V_{ctrl1} from 0.3 V to 0.6 V range. A circuit design was presented using a g_m/I_D methodology and can be adapted to other frequency ranges by sizing the circuit's varicap.

The obtained result was achieved analytically in a methodological way that can be used for any circuit. Being the first proposition of a general temperature-aware design methodology based on g_m/I_D . This is an extension of [16] technique for a larger temperature range of a temperature-independent oscillation frequency for an extended temperature range suitable for harsh environments applications to the best of our knowledge.

VII. ACKNOWLEDGMENT

The authors would like to thank Rachid Hamani for the provided measurement data that without it, the presented results would not be possible in this work.

REFERENCES

- [1] J. D. Cressler and H. A. Mantooth, *Extreme Environment Electronics*, 1st ed. CRC Press, Apr. 2017. ISBN 9781315216911
- [2] R. Johnson, et al., "The Changing Automotive Environment: High-Temperature Electronics," *IEEE Trans. Electron. Packag. Manufact.*, vol. 27, no. 3, pp. 164–176, Jul. 2004. [Online]. Available: <https://doi.org/10.1109/TEPM.2004.843109>
- [3] C. Buttay, et al., "State of the art of high temperature power electronics," *Materials Science and Engineering: B*, vol. 176, no. 4, pp. 283–288, Mar. 2011. [Online]. Available: <https://doi.org/10.1016/j.mseb.2010.10.003>
- [4] A. Ottaviani, et al., "Evaluation of High-Temperature High-Frequency GaN-Based LC-Oscillator Components," *IEEE Trans. Electron Devices*, vol. 67, no. 11, pp. 4587–4591, Nov. 2020. [Online]. Available: <https://doi.org/10.1109/TED.2020.3016918>
- [5] Z. Schwartz and G. Ponchak, "1-GHz, 200/spl deg/C, SiC MES-FET Clapp oscillator," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 11, pp. 730–732, Nov. 2005. [Online]. Available: <https://doi.org/10.1109/LMWC.2005.858995>
- [6] K. Shanmugalingam, et al., "Temperature Sensing and Data Transmission Mechanism for High Temperature Applications," in *2019 1st Int. Conf. Electrical, Control and Instrumentation Engineering (ICE-CIE)*, Nov. 2019, pp. 1–7. [Online]. Available: <https://doi.org/10.1109/ICECIE47765.2019.8974747>
- [7] D. D. Shin, et al., "Lateral diffusion doping of silicon for temperature compensation of MEMS resonators," in *2018 IEEE Int. Symp. on Inertial Sensors and Systems (INERTIAL)*. Moltrasio: IEEE, Mar. 2018, pp. 1–4. [Online]. Available: <https://doi.org/10.1109/ISSS.2018.8358144>
- [8] Q. Liu and C. Chai, "A 1.8-GHz temperature drift compensated LC-VCO for RFID transceiver," *Analog Integr. Circ. Sig. Process*, vol. 105, no. 1, pp. 7–12, Oct. 2020. [Online]. Available: <https://doi.org/10.1007/s10470-020-01694-x>
- [9] K. Okuno, et al., "A 2.23 ps RMS jitter 3 μs fast settling ADPLL using temperature compensation PLL controller," in *2014 21st IEEE Int. Conf. on Electronics, Circuits and Systems (ICECS)*, Dec. 2014, pp. 68–71. [Online]. Available: <https://doi.org/10.1109/ICECS.2014.7049923>
- [10] C. Park, et al., "Reversal of temperature dependence of integrated circuits operating at very low voltages," in *Proc. Int. Electron Devices Meeting*, Dec. 1995, pp. 71–74. [Online]. Available: <https://doi.org/10.1109/IEDM.1995.497185>
- [11] C. Galup and M. Schneider, "The compact all-region MOSFET model: Theory and applications," in *IEEE New Circuits Syst. Conf.*, IEEE, Jun. 2018, pp. 166–169. [Online]. Available: <https://doi.org/10.1109/NEWCAS.2018.8585657>
- [12] P. Toledo, et al., "CMOS transconductor analysis for low temperature sensitivity based on ZTC MOSFET condition," in *Int. Symp. on Integrated Circuits and Systems Design (SBCCI)*, Apr. 2015, pp. 1–7. [Online]. Available: <http://dx.doi.org/10.1145/2800986.2801000>
- [13] J.-P. Eggermont, et al., "Design of SOI CMOS operational amplifiers for applications up to 300/spl deg/c," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 2, pp. 179–186, Feb. 1996. [Online]. Available: <https://doi.org/10.1109/4.487994>

- [14] F. Silveira, D. Flandre, and P. Jespers, "A g_m/I_D based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," vol. 31, no. 9, pp. 1314–1319, Sep. 1996. [Online]. Available: <https://doi.org/10.1109/4.535416>
- [15] J. R. O. R. Martins, et al., "A Temperature-Aware Framework on g_m/I_D -Based Methodology using 180 nm SOI from -40°C to 200°C ," *IEEE Open J. Circuits Syst.*, pp. 1–1, Mar. 2021. [Online]. Available: <https://doi.org/10.1109/OJCAS.2021.3067377>
- [16] J. R. O. R. Martins, F. Alves, and P. M. Ferreira, "A 237 ppm/ $^\circ\text{C}$ L-band active inductance based voltage controlled oscillator in SOI 0.18 μm ," in *Int. Symp. on Integrated Circuits and Systems Design (SBCCI)*, Oct. 2021, pp. 1–6. [Online]. Available: <https://doi.org/10.1109/SBCCI53441.2021.9529990>
- [17] G. Hibliot, "DIBL-Compensated Extraction of the Channel Length Modulation Coefficient in MOSFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 4015–4018, Sep. 2018. [Online]. Available: <https://doi.org/10.1109/TED.2018.2853699>
- [18] T. H. P. de Castro, R. L. Moreno, and D. M. Colombo, "A 0.85 V CMOS voltage and current reference using SCCTs," in *IEEE New Circuits Syst. Conf.*, IEEE, Jun. 2021, pp. 1–4. [Online]. Available: <https://doi.org/10.1109/NEWCAS50681.2021.9462762>
- [19] M. Lundstrom, *Fundamentals of Carrier Transport*, 2nd ed. Cambridge University Press, Mar 2010. [Online]. Available: <https://doi.org/10.1017/CBO9780511618611>
- [20] J. Martins, F. Alves, and P. M. Ferreira, "MOSLab: From Semiconductor to Transistor-Level Modeling in Julia," in *Open Software* Oct. 2021. [Online]. Available: <https://doi.org/10.5281/zenodo.5589821>
- [21] E. Buckingham, "On Physically Similar Systems; Illustrations of the Use of Dimensional Equations," *Physical Review*, vol. 4, no. 4, pp. 345–376, Oct. 1914. [Online]. Available: <https://link.aps.org/doi/10.1103/PhysRev.4.345>
- [22] L. Lu, H. Hsieh, and Y. Liao, "A Wide Tuning-Range CMOS VCO With a Differential Tunable Active Inductor," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 9, pp. 3462–3468, Sep. 2006. [Online]. Available: <https://doi.org/10.1109/TMTT.2006.880646>
- [23] J. Martins, E. Avignon-Meseldzija, and P. M. Ferreira, "Temperature-Aware g_m/I_D -based Methodology for Active Inductor Design," in *Workshop Circuits Syst. Design*, Aug. 2019, pp. 1–4. [Online]. Available: <https://hal-centralesupelec.archives-ouvertes.fr/hal-02268794>
- [24] J. Martins, F. Alves, and P. M. Ferreira, "IC-Layout Render : Image rendering tool for integrated circuit layout in Python," in *Open Software* Nov. 2021. [Online]. Available: <https://doi.org/10.5281/zenodo.5618268>