A Contactless Patterned Plasma Processing for Interdigitated Back Contact Silicon Heterojunction Solar Cells Fabrication

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Abstract— We present results from the application of a novel, contactless patterning technique to form the doped fingers required for interdigitated back contact silicon heterojunction (IBC-SHJ) solar cells. The technique involves patterning the RF powered electrode in a custom-designed RF-PECVD chamber. The patterned powered electrode – which has 1 mm wide opening-slits in it - is brought in close proximity to the substrate surface, to localize the plasma and the process it performs. In this work, the localized plasma process being employed is an NF_3/Ar etching, and is used to form doped fingers that are sub-mm wide and 60 mm long. The interdigitated structure (alternating electron and hole collection zones) is created by first uniformly depositing an intrinsic/n-type a-Si:H passivation stack, followed by an n-type/p- type µc-Si:H recombination junction on the rear side. A passivation layer is also deposited on the front side. The regions for the hole collection zones are then etched down to the intrinsic a-Si:H layer, and finally, a uniform p-type a-Si:H layer is deposited everywhere. The etched finger areas are first investigated by profilometry and spectroscopic ellipsometry, showing that the process can be controlled to leave as little as a few nanometers of passivating intrinsic a-Si:H. This fine control is achieved by pulsing the plasma, to slow the etching rate to a few Å/s. To evaluate the detailed opto-electronic properties of the structure, the samples are mapped out using two contactless techniques: Photoluminescence and Surface Photovoltage measurements (done with a macroscopic scanning Kelvin probe performed under dark and illuminated conditions). These measurements enable one to see both zones of degraded passivation, and the effectiveness of the doped regions in generating an open circuit voltage under illumination.

Keywords—IBC-SHJ, PECVD, crystalline silicon, surface photovoltage, patterned plasma etching

I. Introduction

The interdigitated back contact (IBC) design provides impressively high efficiencies for silicon heterojunction (SHJ) solar cells due to the lack of metallic contact shading on the front surface. This enhancement in efficiency comes at a cost of more complex fabrication, due to the necessity of performing certain type of patterning of the interdigitated doped areas on the rear. The potential payoff is evident, as some of the record breaking efficiencies for crystalline silicon solar cells have been achieved using this architecture [1, 2].

In this work, we present a new strategy to perform this patterning step, however one that is contactless and requires no masking steps. By using a custom-designed radiofrequency (RF) capacitively coupled plasma (CCP) etching process system, we can perform the necessary patterning steps to fabricate the interdigitated doped areas with the precision and scale necessary for IBC-SHJ solar cells.

II. Experimental Details

A. Plasma Process

The experiments presented herein were carried out in a single chamber PECVD reactor, which comprises a cylindrical plasma confinement vessel (grounded) surrounding two parallel positioned electrodes: an RF powered electrode and a grounded electrode (where the substrate was placed). As described in [3], the contactless plasma patterning step involves the use of a grooved powered electrode, as shown in Fig. 1 (a). This powered electrode has five evenly spaced 1 mm wide opening-slits in the showerhead, each with a length of 60 mm.

Under typical operating conditions (inter-electrode distances of a few cm and gas pressures of a few Torr) such slits would provide a hollow cathode enhancement to the plasma [4, 5], making the plasma denser but maintaining a uniform distribution. However, by approaching the powered electrode to within a very short distance of the substrate surface, plasma ignition is inhibited in all zones outside of the slits, as depicted in Fig. 1 (b). The sample photograph after a typical patterned plasma etching is presented in Fig. 1 (c). In this work, the plasma process being employed is an NF_3/Ar etching, but previous work has shown it to be effective for deposition as well [3].

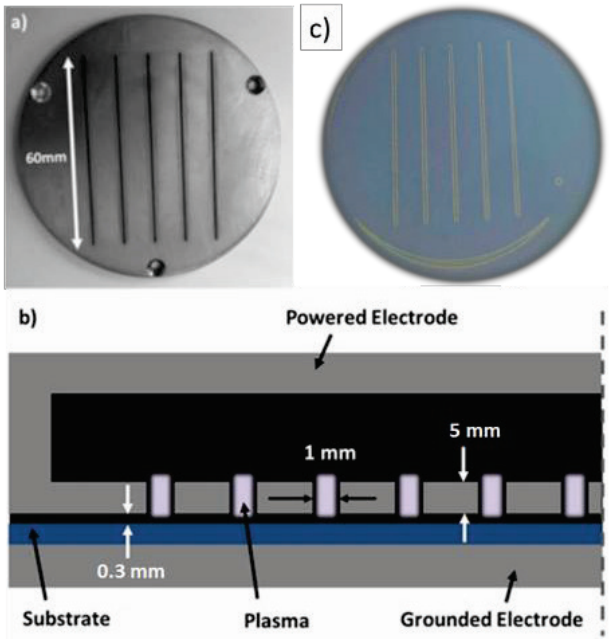

Fig. 1. (a) Photograph of grooved powered electrode, removed from showerhead assembly, (b) schematic showing localization of plasma within slits, limiting the extent of plasma processing area, and (c) photograph of a typical patterned etched sample (silicon thin film stack deposited on 4-inch crystalline silicon wafer, and the arc-like pattern at bottom is resulting from parasitic plasma).

B. *Device Structure*

As shown in Fig. 2 (a), we demonstrate the use of this localized plasma etching to create the IBC structure. The crystalline silicon (c-Si) wafer used is a 280 µm thick double-side polished n-type <100> float-zone wafer, with a resistivity of 1-5 Ω·cm. After oxide removal via 30 seconds HF dip, uniform layers are deposited on the entire substrate surface: on the rear, a 15 nm intrinsic hydrogenated amorphous silicon ((i)a-Si:H) passivation layer. On the front, the same passivation layer is followed by a 13nm n-type ((n)a-Si:H) back surface field layer, and a 55 nm n-type/p-type hydrogenated microcrystalline silicon ((n)µc-Si:H/(p)µc-Si:H) recombination junction (the use of which in multitechnology multijunctions [6] and micromorph thin film silicon [7] designs is well documented).

After the uniform film stacks are deposited, the localized plasma etching process is employed to etch down to the (i)a-Si:H passivation layer. To allow one to stop on this layer, the localized process must be slowed down (as the hollow cathode effect tends to result in very fast processing rates). Slowing down the process is achieved by pulsing the plasma at a low frequency (from 100 Hz to 1 kHz) and at a low duty cycle (0.5 % to 1 %), permitting one to prevent over-etching (removing passivation) or under-etching (etching stopped before reaching the passivation layer), as illustrated by Fig. 2 (b). Finally, a uniform deposition of 30 nm p-type a-Si:H ((p)a-Si:H) emitter is done. The final structure is similar to that described in [9], wherein the areas with (i)a-Si:H covered first by (n)a-Si:H and then a recombination junction act as the electron collection zones, and the areas with (i)a-Si:H covered first (and only) by the (p)a-Si:H function as the hole collection zones.

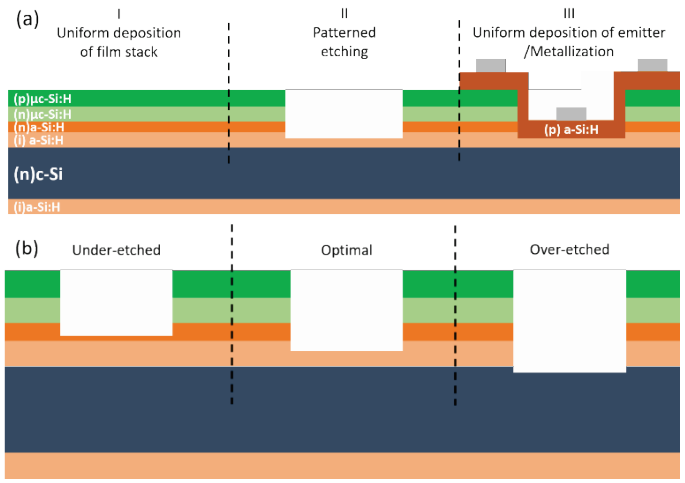

Fig. 2. Fabrication steps for device structure: (a) (I) uniform deposition of front passivation layer, rear passivation layer, back surface field layer, and recombination junction, (II) localized plasma etching down to passivation layer, and (III) uniform deposition of (p)a-Si:H emitter. (b) In step II, three different etching scenarios are displayed: under-etched, optimal and over-etched.

C. *Characterization Techniques*

The resulting patterned structures have been first investigated by profilometry (Bruker Dektak XT) and spectroscopic ellipsometry (Horiba Jobin-Yvon UVISEL). The corresponding opto-electronic properties were further mapped out using contactless techniques: photoluminescence (PL) (WITec, and BT Imaging LIS-R2) and surface photovoltage (SPV) (KPtechnology ASKP200250) measurements. The SPV mapping is acquired by performing Kelvin Probe Atomic Force Microscopy both in the dark and under illumination, and by subtracting the dark map (which is a map of the work function) from the latter one [8]. It should be noted that due to experimental constraints, illumination has been done from the patterns side (so, the wrong side for proper IBC-SHJ solar cells operation).

III. Results and Discussion

A. *Patterned plasma etching*

A typical depth profile covering all the five etching trenches obtained by profilometry is shown in Fig. 3, and one can note that the width of the trenches (FWHM of around 800 µm) is narrower than the slits in the powered electrode. Even narrower trenches can be expected by further reducing the slit width. As well, one should remark the different scales on the axes (depth in angstroms, and lateral dimensions in µm); this process results in very low aspect ratio structures. Moreover, in Fig. 4, a 3D mapping of one etching trench shows an excellent uniformity along 10mm of its length.

To further quantify the etching process, spectroscopic ellipsometry measurements have been performed on a sample having a single layer of (i)a-Si:H deposited on top of the c-Si wafer. Fig. 5 presents the ellipsometry spectra of the imaginary part of dielectric function obtained from the measurements taken within the etching trench before and after one-minute of plasma etching (with an RF power of 60 W pulsed at 1 kHz and with a duty cycle of 1 %).

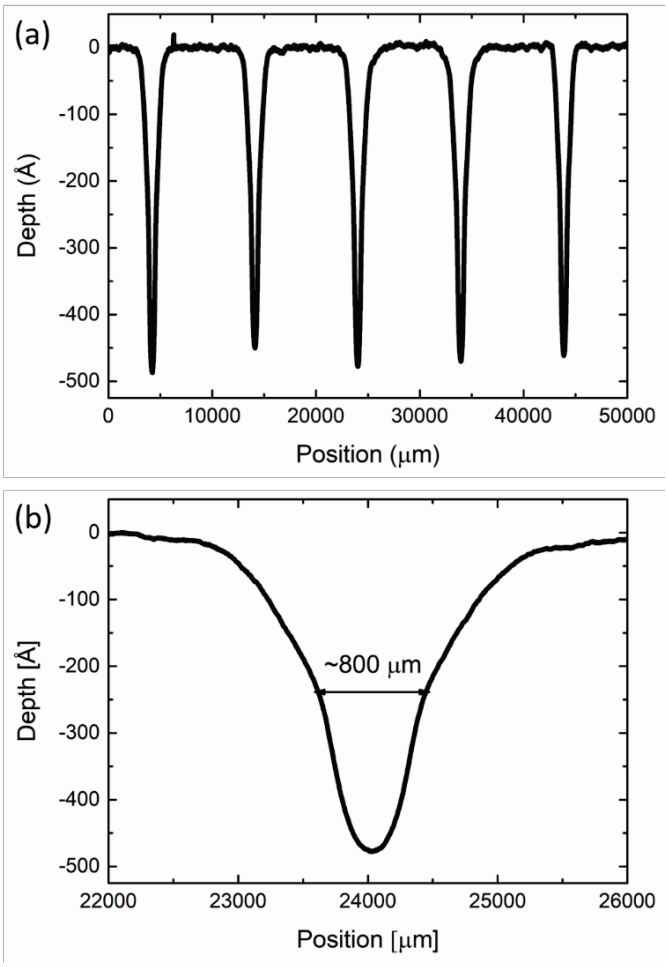

Fig. 3. Typical profilometry scans performed on a patterned etched sample: (a) covering five etching trenches, and (b) zoom in one trench. Note different scales for depth and lateral dimensions.

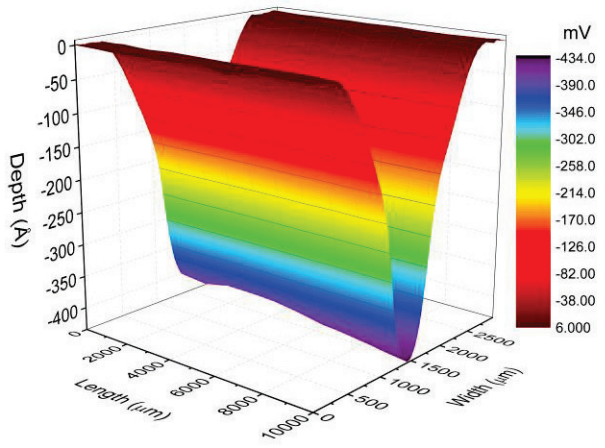

Fig. 4. 3D profilometry mapping of one etch trench along 10 mm of its length. Note different scales for depth and position.

To fit the experimental data, the two-layer model with a bulk layer and a surface roughness has been used, where the amorphous material is described by a single Tauc-Lorentz dispersion formula. The surface roughness was defined by a mixture of 50 % of the bulk material and 50 % of voids using the Bruggeman effective medium approximation [10]. The parameters allowed to vary in the fitting process are the thickness of each layer and all the parameters of Tauc-Lorentz dispersion formula. A further description of the ellipsometric modeling for a-Si:H film can be found in [11].

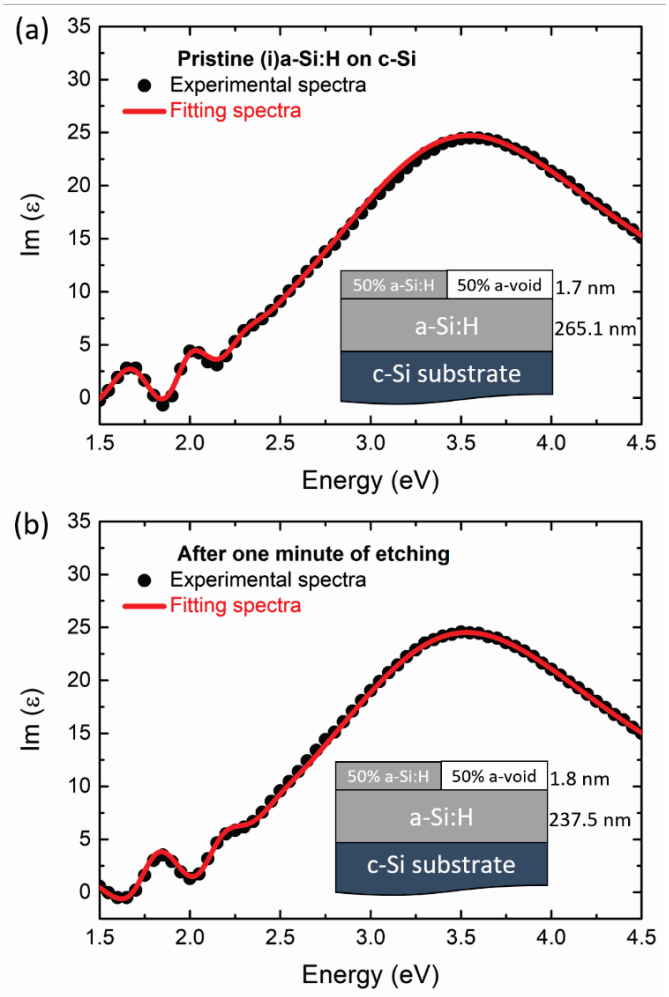

Fig. 5. Ellipsometry spectra of the imaginary part of dielectric function (black dots) obtained from the measurements taken within the etching trench (a) before and (b) after one-minute of plasma etching. The fitting spectra are also depicted (red lines) along with the models for fit (insets).

As one can see, the one-minute etching process leads to a reduction of the total thickness by 27.5 nm, giving the etching rate of around 4.6 Å/s (even lower etching rate can be achieved by further reducing the plasma pulsing duty cycle). Moreover, the similarity of spectra in both states indicates that very little roughness is induced by the etching process. This is further confirmed by the fitting results, as illustrated by the insets.

B. Patterned plasma etching of film stack for IBC structure

Similarly, the film stack prepared for the IBC structure was etched by the localized plasma. As an example, the ellipsometry spectra obtained before and after etching is shown in Fig. 6. For the pristine stack, the shoulder-like peaks at 3.4 eV and 4.2 eV provide a signature of the microcrystalline silicon phase in the top layer. Thanks to the fine control of etching rate, an optimal

etching – leaving behind the passivating (i)a-Si:H layer with reasonable thickness – can be achieved. As indicated by the fitting results, a thickness of around 12 nm remaining (i)a-Si:H layer inside the etching trench was obtained after the patterned plasma etching (with an RF power of 90 W pulsed at 100 Hz and with a duty cycle of 0.5 %).

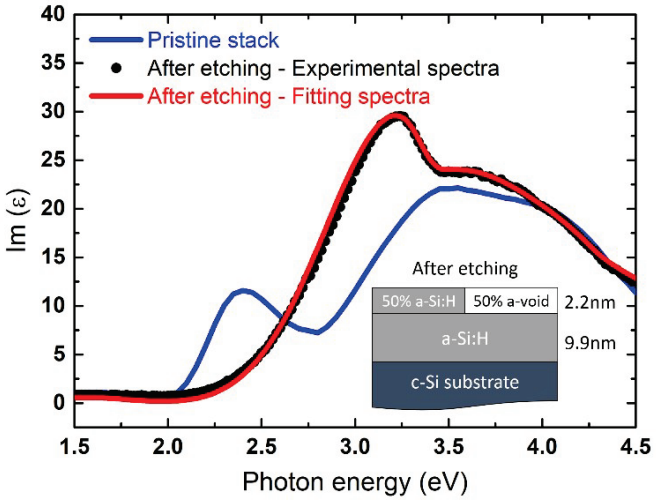

Fig. 6. Ellipsometry spectra for film stack taken within the etching trench before (blue line) and after (black dots) plasma etching in the optimal case. The fitting spectra after etching is also depicted (red line) along with the model for fit (inset).

C. *Opto-electronic properties*

It has been shown that the patterned plasma etching can be effective for the partial etching of the film stack. To finish the IBC structure, uniform (p)a-Si:H layers have been deposited on top of a series of patterned etched stacks with different etching scenarios: under-etched, optimal, and over-etched, as depicted in Fig. 2 (b). The opto-electronic properties of the device structures have been analyzed.

By using the quasi-steady-state photoconductance decay calibrated PL, the effective lifetime measurements have been done for these stacks before and after the final uniform (p)a-Si:H emitter deposition. The high resolution lifetime mappings, reported for minority carrier densities of 10^{15} cm^{-3}, are shown in Fig. 7. The first, second, and third row corresponds to the case of under-etched, optimal, and over-etched, respectively. As indicated by the patterns corresponding to the localized plasma positions, the patterned plasma etching leads to a certain degree of passivation degradation. Such degradation can be partially recovered after the following uniform (p)a-Si:H deposition. However, as one can note from Fig. 7 (c) and (f), the over-etched case is an exception. This suggests that the plasma-surface interaction can induce irreversible damage if the etching is performed all the way down to the crystalline silicon surface, and it is evident that a certain thickness of passivation layer is necessary to serve as a protection barrier against the intense plasma treatment.

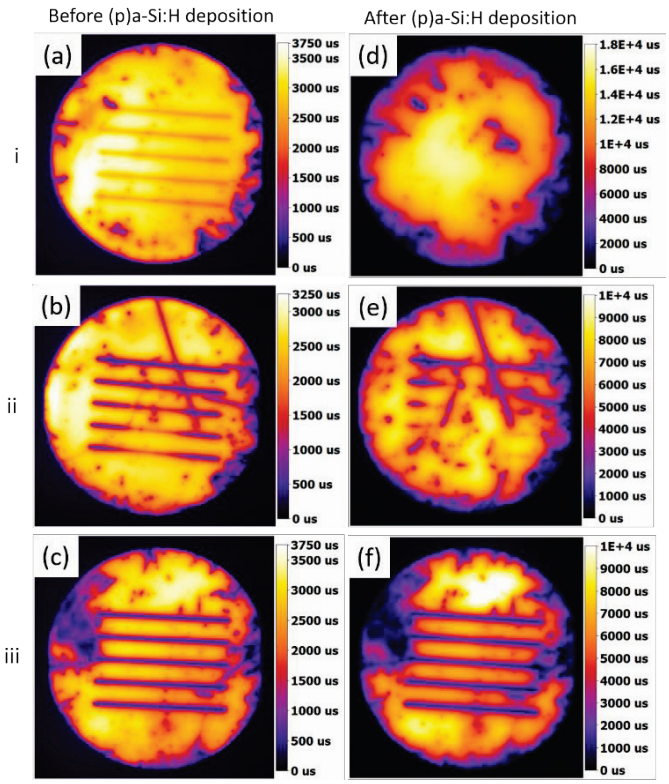

Fig. 7. Quasi-steady-state photoconductance decay calibrated PL lifetime mappings (a), (b), (c) before (left column) and (d), (e), (f) after (right column) (p)a-Si:H deposition for film stacks having three different scenarios in the patterned etching step: under-etched, optimal, and over-etched, corresponding to row (i), (ii), and (iii), respectively.

To further quantify the etching quality, another series of samples having different thicknesses (from 2 nm to 14 nm) of remaining protective (i)a-Si:H passivation layer after the patterned plasma etching were prepared. Fig. 8 presents the PL spectra acquired inside and outside of the etching trenches for these samples. As a comparison, the spectra for an over-etched sample is also included. It should be mentioned (and as it has been indicated in the figures) that the measurement integration time is different for different samples and different acquisition locations. As one can see, PL signal intensity decreases with remaining (i)a-Si:H thickness, and removal of the passivation does indeed reduce the PL signal to a very low level. This is in line with the results presented in Fig. 7. One can conclude from these results that having a passivation layer of around 10 nm left after the patterned plasma etching is a reasonable balance between the formation of patterns for IBC-SHJ structure and a good passivation quality.

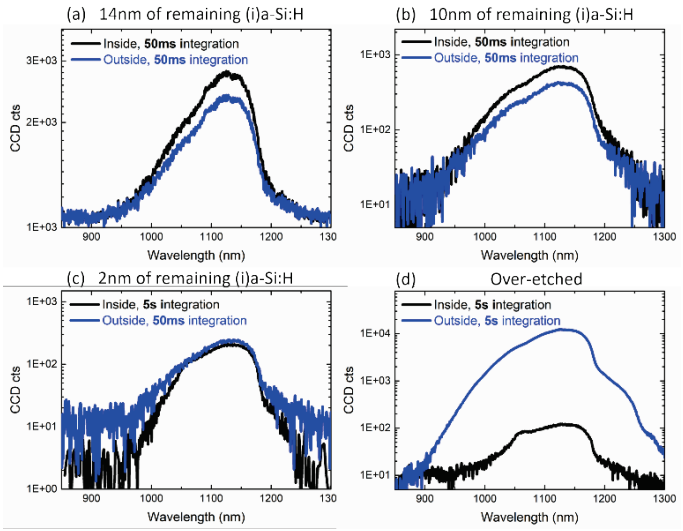

Fig. 8. PL spectra obtained inside (black) and outside (blue) of the etching trench for samples with different thicknesses of remaining (i)a-Si:H passivation layer after the patterned plasma etching. Note different integration time for different samples and acquisition locations.

To complement the PL measurements, SPV mapping measurements have also been performed, using full spectrum tungsten-halogen fiber illumination from the top, patterned side. These mappings have been performed on two of the typical patterned stacks discussed above: one with a 10 nm passivation layer left, and another over-etched sample. One can see that, in Fig. 9 (a), within the etching trenches, the measured voltage is lower (around -150 mV), whereas on the plateaus, the values closer to 50 mV are measured. This indicates that the photovoltaic effect and an open circuit voltage (V_{OC}) are present, and the latter is quantified to be ~200 mV. Whereas, for the case of removing all the passivation layer during etching as shown in Fig. 9 (b), the value is reduced down to ~150 mV.

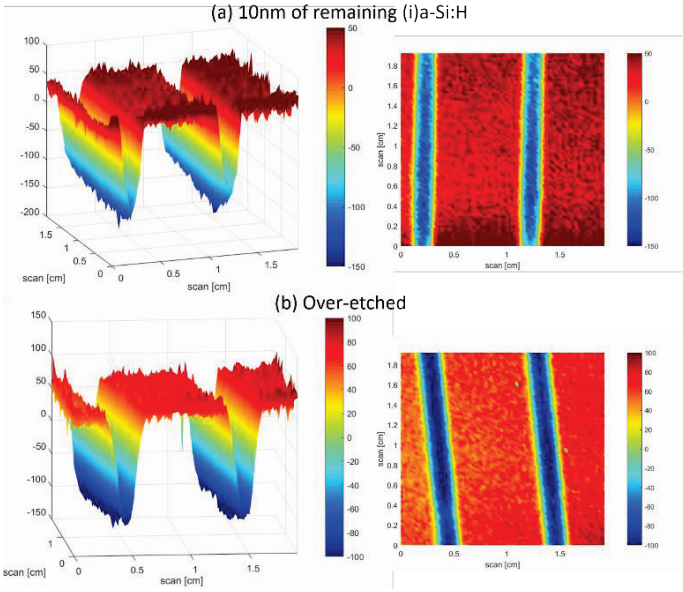

Fig. 9. 3D mapping (left) and 2D top view (right) of surface photovoltage for samples shown in Fig. 8 (b) and Fig. 8 (d) (covering two etching trenches, with illumination from the patterned side). Note the unit of mV for z-axis.

Previous work using SPV to characterize IBC-SHJ solar cells has also noted that although the value of the difference in photovoltage will increase with the V_{OC} of the solar cell, it is not necessarily equal to V_{OC} due to surface states and stray capacitances.

D. Conclusions

In this work, we have presented a novel technique to fabricate the interdigitated patterns on silicon thin film stacks for IBC-SHJ solar cells, and have shown results concerning the structural and opto-electronic properties. The use of ellipsometry, PL, and SPV in particular permits one to evaluate the process quality and is helpful to indicate if the initial uniform film stack has been over-etched (removing passivation) or under-etched (leaving behind the opposite doped layer).

These characterization techniques are currently being used to improve the process and guide the fabrication of solar cells. After metallization, preliminary results about the device IV characteristics were obtained, but with low performance compared to state of the art devices. In particular, a very low current density was observed, and this is now recognized to be due to the complete removal of passivation layer during the patterned plasma etching step. Work on the improvement of the device performance is in progress.

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