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An Ultralow Power Li_xTiO_2 -Based Synaptic Transistor for Scalable Neuromorphic Computing

Ngoc-Anh Nguyen, Olivier Schneegans, Raphaël Salot, Yann Lamy, John Giapintzakis, Van Huy Mai, and Sami Oukassi*

Artificial synapses based on electrochemical synaptic transistors (SynTs) have attracted tremendous attention toward massive parallel computing operations. However, most SynTs still suffer from downscaling limitations and high energy consumption. To overcome such drawbacks, a complementary metal–oxide–semiconductor (CMOS) back-end-of-line compatible solid-state SynT is presented, which includes an ultrathin (10 nm thick) quasiamorphous Li_xTiO_2 channel. A nonvolatile conductance modulation (<75 nS) is achieved through reversible lithium intercalation into the channel, and synaptic functions, such as long-term potentiation/depression involve ultralow switching energy of 2 fJ μm^{-2} . Moreover, this SynT shows excellent endurance (> 10^5 weight updates) and recognition accuracy (>95% on the MNIST data test using crossbar simulations). Furthermore, a comprehensive electrochemical study allows deeper insight into the specific pseudocapacitive mechanism at the origin of conductance modulation. These results underline the high potential of Li_xTiO_2 -based SynTs for energy-efficient neuromorphic applications.

energy consumption and the large number of involved elements and area occupancy prevent efficient downscaling.^[5,6] Thus in recent years, memristors have attracted much interest since the conductance of these (more scalable) devices^[6–8] can be easily modified as a function of external electrical stimuli, hence emulating the evolution of biological synaptic weights. Different types of memristors have been developed, which can be subdivided into two-terminal devices and three-terminal devices.^[9] Each configuration has its own strengths and weaknesses.^[1,10] Specifically, the three-terminal configuration allows decoupling the WRITE operation (synaptic weight modulation, using the gate and source electrodes) from the READ operation (using the source and drain electrodes), which allows better control of conductance tuning^[11] (e.g., better linearity and symmetry of switching, and lower read-write noise).^[12]

Among three-terminal artificial synapses, electrochemical synaptic transistors (SynTs) appear as suitable candidates due to their similarities with biological synapses. In a SynT, the gate dielectric is an electrolyte film, which conducts only ions (but not electrons). When an external voltage pulse (WRITE) is applied between the gate and source, mobile ions intercalate into the channel film through electrochemical reactions, which yields modulation of the channel's electronic conductivity. The aforementioned working mechanism of SynTs shows similarities with that of biological synapses where Ca^{2+} , Na^+ ,

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1. Introduction

The present Von Neumann computing architecture faces huge difficulties in complex tasks, such as recognition or classification problems, which require adaptive information processing. In order to overcome this bottleneck, neuromorphic computing^[1,2] appears as a novel and highly promising architecture,^[3,4] which takes inspiration from the mammalian brain structure. In such a system, artificial neurons and synapses mimic their biological counterparts.

Complementary metal–oxide–semiconductor (CMOS) devices can emulate artificial synapses. However, the high

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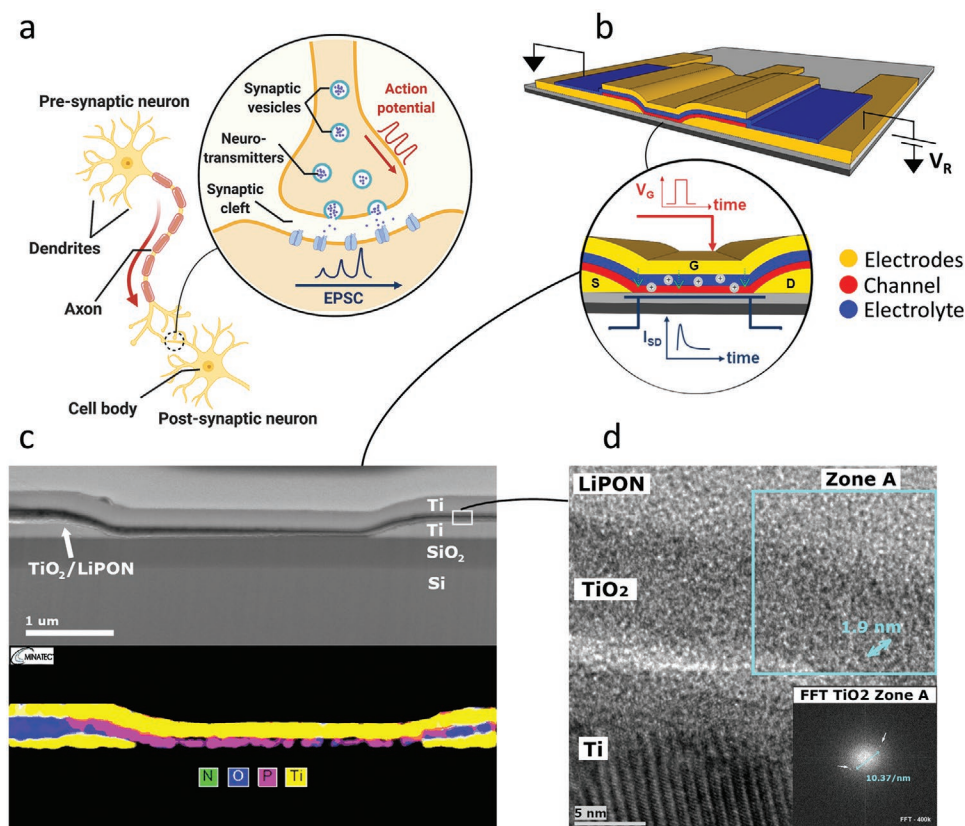


Figure 1. a) Illustration of chemical synapses in a mammalian brain. b) Schematic view of our microfabricated SynT. c) SEM and EDS characterizations of SynT's gate stack. d) HRTEM image with the focus on the neighborhood of TiO₂ channel (inset: FFT on the selected Zone A).

K⁺ ions are mainly used to modify the postsynaptic signals.^[13] This similarity potentially places SynTs in a close position to its inspiration, the biological synapses, in terms of operation, energy, and speed.

However, elaboration of most electrochemical SynTs toward further scalability and CMOS compatibility suffers several kinds of difficulties. Liquid and solid polymer electrolytes (ionic liquids,^[14] ion gels,^[15] PEO-LiClO₄)^[16–19] show clear limitations toward wafer scale integration.^[20] Furthermore, channels composed of mechanically exfoliated layers^[16,18,21] appear not suitable for future elaboration of networks composed of a large number of synaptic components. For these reasons, fabrication of all-solid-state wafer-scale SynTs is highly desirable and is drawing considerable attention.^[22–28] Besides, a comprehensive electrochemical view—clearly missing to date—of ion intercalation into the active material (the main root of conductance modulation) is needed to better explore the full potential of electrochemical SynTs.

In this work, we present an all-solid-state, wafer-scale fabricated SynT composed of an ultrathin (10 nm thick) quasiamorphous Li_xTiO₂ channel and a LiPON electrolyte. This SynT shows excellent synaptic plasticity, with nano-Siemens conductance level, and outstanding low energy consumption per spike (f) μm⁻² range). We also simulated an Artificial Neural Network (ANN) model to analyze the pattern recognition performance on different datasets. Finally, various electrochemical tests were carried out to better understand the mechanism of Li (de)intercalation driving the conductance modulation in our SynT.

2. Results and Discussion

2.1. Artificial Electrochemical Synapse Composition and Configuration

In a mammalian brain, Chemical synapses are by far the most prevalent and are the main player involved in excitatory synapses.^[29] In a nervous system, information is transmitted among neurons via such synapses, as schematically illustrated in **Figure 1a**. Action potentials from the presynaptic neuron propagate along the axon and arrive at synapses where they induce the release of neurotransmitter vesicles into the synaptic cleft. Upon the reception of these chemical messengers (cations), excitatory postsynaptic currents (EPSCs) are stimulated across the postsynaptic region. The bonding strength between two neurons is dictated by its synaptic weight.^[30,31]

The operation mechanism of electrochemical SynTs shares similarities with chemical synapses. Mobile ions are driven by electrical impulses to modulate the strength of the signal transmission. Figure 1b shows an illustrative view of our microfabricated SynT device. The cell core (synaptic element) is a vertical stack consisting of an ultrathin (10 nm) titanium dioxide (TiO₂) channel, an electrolyte (reservoir of Li⁺ ions) made of amorphous lithium phosphorus oxynitride (LiPON), and a top gate made of Ti. This vertical configuration was considered to allow for shorter diffusion path, thus increasing the operational speed.^[17,32]

Amorphous TiO_2 was selected as channel material because of its well-studied intrinsic merits as suitable host for Li-ion intercalation in energy storage applications.^[33–35] Additionally, TiO_2 in its amorphous form is known to exhibit pseudocapacitive characteristics which allow fast, reversible ion intercalation without phase transition.^[36,37] Furthermore, TiO_2 undergoes an insulator-to-metal transition upon ion intercalation, thus making it an appealing material for ion-based SynTs.^[38,39] LiPON has been chosen as solid-state electrolyte for its high chemical and electrochemical stability,^[40–43] and scalability.^[44,45]

The inset of Figure 1b shows a schematic cross-section of the transistor. Square-shaped voltage pulses applied to the gate mimic the biological impulses of the presynaptic neurons. Under these spikes, Li^+ ions are inserted into the channel material (red layer), connecting the source and drain electrodes via the electrolyte (blue layer), hence creating a change in electrical conductance. This conductance change is captured by electrically sampling with a small, constant potential bias (V_R) the current flowing between the source and drain.

From Figure 1c, we can observe that the channel length (between source and drain electrodes) is about 3 μm , using scanning electron microscopy (SEM). The LiPON layer thickness is 200 nm, as desired. The composition of the layers is observed with the help of energy dispersive X-ray spectrometry (EDS), where elements P and O represent the LiPON electrolyte. Furthermore, no interfacial interdiffusion is discerned with the detectable elements. The stoichiometry of the atomic layer deposition (ALD) TiO_2 layer was confirmed with X-ray photoelectron spectroscopy (see Figure S2 in the Supporting Information). High-resolution transmission electron microscopy (HRTEM) has been carried out to inspect the channel's structural properties (Figure 1d). The stacked layers are differentiated based on the thicknesses and their contrasts. The 10 nm thickness of the TiO_2 layer is clearly confirmed from the image. Besides, the HRTEM analysis gives valuable information about channel film properties, indicating the presence of 2 nm size nanocrystallites embedded in the amorphous matrix. We performed the fast Fourier transform (FFT) referencing method on selected zones, and could conclude that the channel was primarily amorphous, and the nanoinclusions were of rutile phase (see Figure S3 in the Supporting Information).

2.2. Working Principles and Electrical Response

Figure 2a depicts the evolution of the SD channel conductance G_{SD} , by application of a bidirectional sweeping gate voltage from -3.0 to 3.0 V (at a rate of 50 mV s^{-1}). A small bias of 0.1 V was applied to read the change in source–drain current (I_{SD}). Initially, G_{SD} was very low ($G_{\text{SD}} \leq 20 \text{ nS}$ at $V_G = 0$ V). Then G_{SD} increased up to a 100 times higher value, reaching 250 nS , due to intercalation of Li^+ ions into the TiO_2 quasiamorphous channel. For the backward sweep (Li^+ extraction), G_{SD} decreased gradually back to its low conductance state, exhibiting a clear counter-clockwise hysteresis pattern. We can see that the highest slopes (which correspond to a more effective conductance variation) are located within the $[-0.5, 1.5 \text{ V}]$ V_G potential region, whereas other regions demonstrated

slow, saturated modification of channel conductance. For this reason, we selected the $[-0.5, 1.5 \text{ V}]$ potential window (inset of Figure 2a) to develop our SynTs. More details on the underlying electrochemistry of the Li^+ doping mechanism under different potential windows will be discussed in a following section.

To demonstrate the ability to modify the analog states required for an artificial synapse, we programmed SynT with a train of 10 voltage pulses with different amplitudes relative to the open-circuit voltage (OCV) measured between the gate and source electrodes at rest. Note that in electrochemical devices, chemical potential gradients are generated by modifying the ionic content of one electrode, and this phenomenon is termed nanobattery effect.^[46] Therefore, it is essential to program SynTs with a gate potential V_G whose amplitude takes into account the OCV values of the cell. After the application of each pulse, the gate terminal was switched OFF for 1 s, when the READ action occurs, to prevent the electron movement and perturbation of the programmed state. Figure 2b illustrates the change of conductance states (ΔG) under the influence of WRITE pulses with the same duration of 0.1 s but different magnitudes (ΔV), from 100 to 300 mV. The pulses of higher amplitude result in a more pronounced change of conductance states. A simple linear fitting better shows the relation between the changes of source–drain conductance (G_{SD}) and the pulse amplitudes. Here, one can observe that by varying the pulse amplitudes, we are driving the SynT channel conductance along the “ Li^+ insertion” conductance curve from Figure 2a but at a different V_G sweeping rate.

Moreover, maintaining the programmed states is of great importance to synaptic elements in an artificial neural network for a high learning precision.^[47] In Figure 2c,d, we demonstrate the retention of the SynTs with both potentiation and depression (increase and decrease of conductance level, respectively). A series of pulses with $\pm 200 \text{ mV}$ magnitude and 0.5 s duration was used for programming the device. The pulses were followed by a resting time of 50 s, while the G_{SD} was recorded. The channel conductance was found to keep the programmed states during the tested periods (further investigation was carried out with a state retention test of over 4000 s, see Figure S4 in the Supporting Information). Hence, the fact that written states could be held stable over a long period of time assures the long-term plasticity characteristic of our SynT.

As shown in Figure 3a, emulation of neuromorphic behavior, such as long-term potentiation (LTP) and long-term depression (LTD) was achieved by alternatively programming the SynT with 50 identical pulses ($\pm 100 \text{ mV}$, 0.1 s) and settling and reading time of 1 s. The conductance states were modified in an analog way from a low conductance level of 28 nS to a high conductance level of 74 nS , which corresponds roughly to a 1 nS increase from one state to the next one. The device-to-device variation was confirmed to be small across SynTs by conducting the same characterization in multiple devices (see Figure S5 in the Supporting Information).

The injected charge over 50 operations has been recorded in order to estimate the amount of energy to program a state to an adjacent one. The energy consumption for SynT devices is calculated by the expression

$$E_w = \Delta Q \times V_w \quad (1)$$

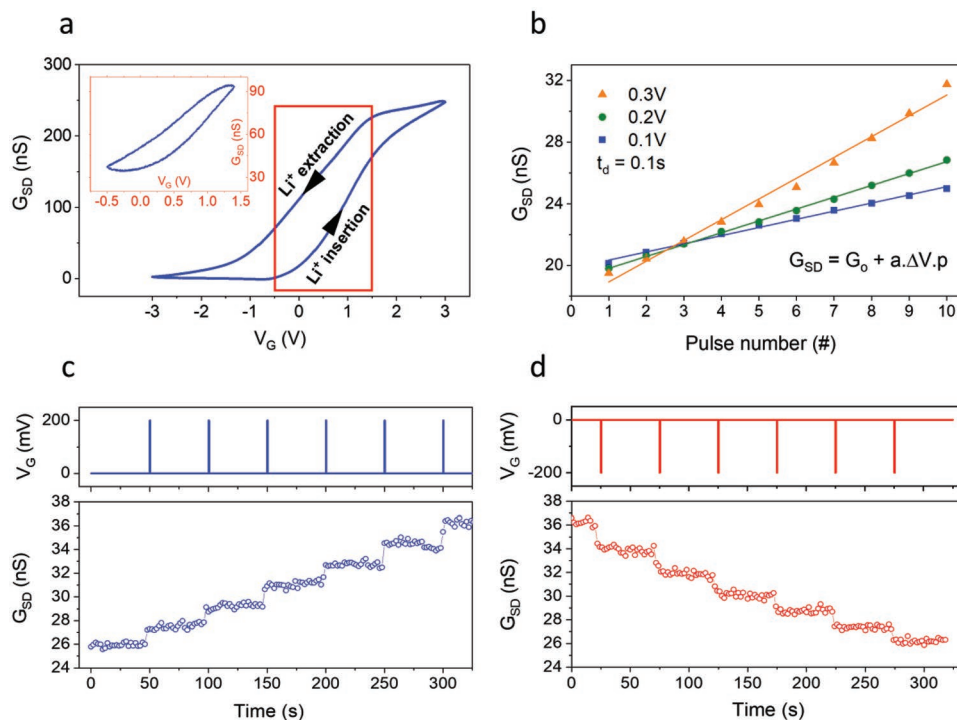


Figure 2. a) Charge transfer curve (channel conductance G_{SD} as a function of gate voltage V_G) with a gate sweep of 50 mV s^{-1} in the potential range $[-3 \text{ V}, 3 \text{ V}]$ (inset: Focused working window of $[-0.5 \text{ V}, 1.5 \text{ V}]$). b) Conductance G_{SD} change under incremental voltage amplitude pulses from 100 mV to 300 mV with a duration t_d of 0.1 s . c) Retention (during 50 s) of G_{SD} after each potentiation pulse (200 mV , 0.5 s), and d) retention of G_{SD} after each depression pulse (-200 mV , 0.5 s). The two experiments are performed on the same device without any disruption.

where ΔQ is the injected charge and V_w is the voltage used for programming. The average charge transferred for SynT was 90 pC , and the voltage used for writing is 0.1 V .

Therefore, 9 pJ is spent for each writing operation. For our SynT with a TiO_2 area of $70 \times 80 \mu\text{m}^2$, we obtain the normalized energy consumption of $1.6 \text{ fJ } \mu\text{m}^{-2}$. Assuming the energy

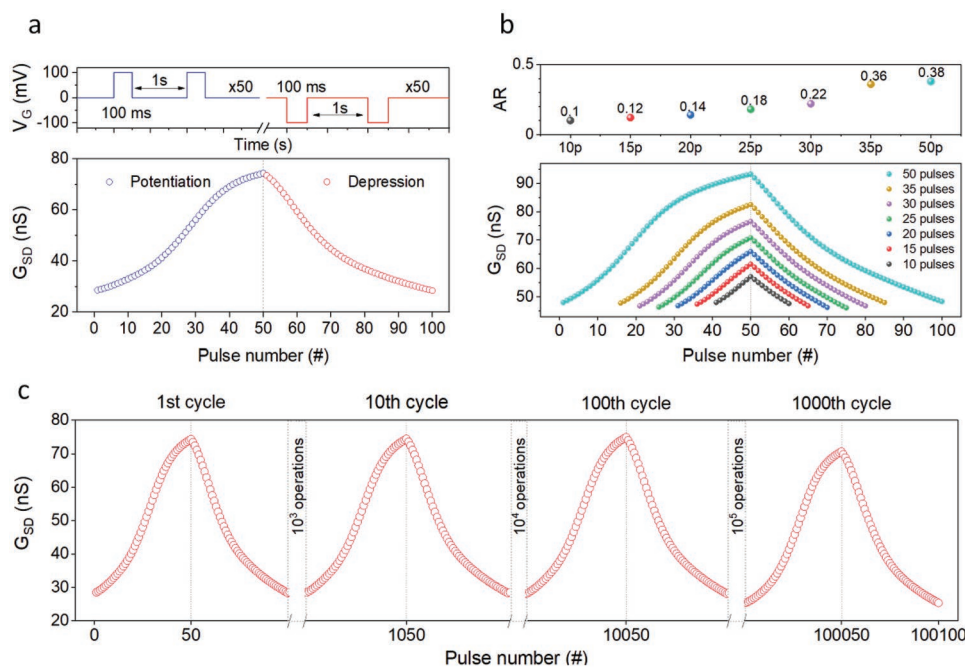


Figure 3. a) Long-term plasticity demonstration with 100 states of potentiation and depression. b) Correlation between the number of states and AR. c) Endurance test with 1000 cycles and 10^5 operations.

per write operation is directly proportional to the channel area, we obtain a projected programming energy of 16 aJ for a scaled $100 \times 100 \text{ nm}^2$ device. Hence, together with the conductance levels in the range of nano-Siemens, our SynT can be considered as one of the most energy-efficient all-solid-state synaptic devices realized in both READ and WRITE operations.

The symmetry property of conductance modulation or the weight update between potentiation and depression processes is characterized by the asymmetric ratio (AR), defined as

$$AR = \left[\frac{\max |G_p(n) - G_d(n)|}{G_p(50) - G_d(50)} \right] \text{ for } n = 1 \text{ to } 50 \quad (2)$$

where $G_p(n)$ and $G_d(n)$ are channel conductance values at the n th state after the potentiation and depression pulses. For our SynT, the AR was calculated to be 0.31 (in Figure 3a) for 100 pulses per cycle, indicating a good symmetry in comparison to results reported in literature.^[32,48]

To analyze the relationship between the number of states per cycle and its AR, we performed a series of programming cycles on a device with a different number of intermediate states and analyzed the corresponding AR (see Figure 3b top). The number of gate pulses increases from 10 to 50 pulses, yielding an increase of AR from 0.1 for 10 pulses to 0.38 for 50 pulses. Thus, one needs to consider the compensation between the desired programming states and their AR for each application.

Figure 3c demonstrates the endurance test of SynT after more than 1000 cycles, with 100 weight update operations in each cycle and with the same pulse scheme as in Figure 3a. The endurance of this device is high since its small change of Max-Min conductance after 1000 cycles is calculated to be

$$\Delta G = (G_{\max} - G_{\min})_{1\text{st}} - (G_{\max} - G_{\min})_{1000\text{th}} = 0.5 \text{ nS} \quad (3)$$

Moreover, the ON/OFF ratio varies only slightly ($\approx 6.2\%$) after 10^5 weight updates (see Figure S6 in the Supporting Information). Although the change of the maximum and minimum states is visible between the 1st and the 1000th cycle, our SynT can keep the reversibility ideally up to 10^5 operations in ambient moisture testing condition (see Figure S7 in the Supporting Information). This endurance is considered largely sufficient for ANN pattern recognition training using artificial synaptic hardware, since not all of the synapses will be repeatedly updated in the course of the training epochs.^[49]

2.3. Neuromorphic Computing Simulation

To underline the low noise and high linearity characteristics of our SynT, we simulated an artificial neural network (Figure 4) with experimental inputs from SynTs to perform supervised learning with a back-propagation algorithm. Two datasets have been used: a small image version (8×8 pixels) of handwritten

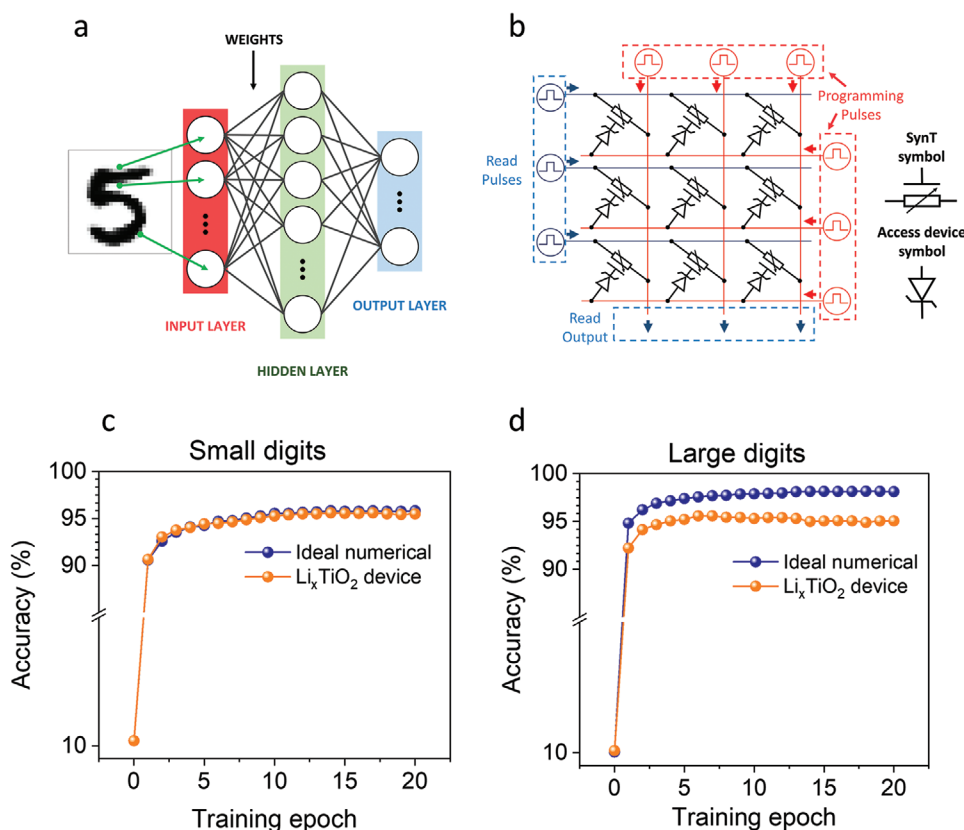


Figure 4. a) Simulated three-layered ANN with one hidden layer. b) Crossbar array representation where SynTs serve as synaptic elements. Accuracy of the MNIST data recognition tests of c) small digits d) large digits.

Table 1. Summary on materials and switching properties of selected works on CMOS compatible, all-solid-state SynTs.

Channel	Electrolyte	G_{SD} [nS]	G_{max}/G_{min}	# States	Prog. Energy [fJ μm^{-2}]	Endurance [Writes]	Refs.
LiCoO ₂	LiPON	290 000	1.56	200	–	$>8 \times 10^3$	[22]
WO ₃	LiPON	24	40	100	100	$>10^5$	[23]
LiCoO ₂	Li ₃ POSe	40	19	80	–	>720	[24]
WO _{2.7}	Li ₃ PO ₄	3500	6.4	60	1.4×10^6	>420	[25]
aNb ₂ O ₅	LiSiO ₂	100	10	100	20	$>10^3$	[26]
WO _x /Al ₂ O ₃	Li ₃ PO ₄	50	2.24	80	–	–	[28]
Li _x TiO ₂	LiPON	75	2.6	100	1.6	$>10^5$	This work

digits from the “Optical Recognition of Handwritten Digits” dataset^[50] and a large image version (28 × 28 pixels) of handwritten digits (MNIST dataset).^[51] The simulation has been done on the CrossSim platform in which neural network modeling can be realized, taking into consideration the linearity and noise characteristics of real devices.^[22,52,53] Figure 4a illustrates the three layers of the simulated neural network, whereas Figure 4b shows schematically a crossbar array of a synaptic weight layer. The SynTs are the synaptic elements at the intersections of the crossbars, whose channel conductance levels were used as the weight update for executing the training. An additional two-terminal selector was employed as a switch to prevent electrons from traveling back to the gate after programming pulses, thus increasing the writing precision. Herein, the crossbar is considered as part of a “neural core” that executes vector-matrix multiplication (inference) and outer-product updates (learning) operations.^[22,52,53] In order to properly simulate the device nonideality, the probability distribution of the change in channel conductance (ΔG) induced by a potentiation or depression pulse was calculated, by taking into account the device noise, nonlinearity, and asymmetry. The recognition accuracies of the simulated networks are shown in Figure 4c,d. For the small digit dataset (Figure 4c), the training accuracy of SynT reaches nearly the ideal numerical limit of 95.5%. For the large digit dataset (Figure 4d), excellent accuracy was also obtained, reaching 95% after 20 training epochs. These classification accuracies are clearly among the highest accuracy values of recently reported SynTs.^[17,18,54]

In **Table 1**, we present the materials and switching properties of the SynT in this work and other reported SynTs. The purpose of this table is to benchmark synaptic devices following wafer scale integration, and using microfabrication techniques and materials that are compatible with CMOS BEOL integration.

By scaling down the channel to 10 nm, our amorphous TiO₂ film exhibits extrinsic pseudocapacitive behavior, which allows simultaneously for ultralow energy consumption and fast/reversible conductance modulation. Both features are indispensable for artificial synapse application. We can observe that low power dissipation is the highlight that this artificial synapse offers. The operational conductance (a few tens of nS) is comparable or lower than other types of three-terminal SynTs. In addition, by reaching an outstanding low energy consumption per spike (1.6 fJ μm^{-2}), close to the biological energy range of femtojoule, our present SynTs appear as an excellent candidate for large-scale energy-efficient neural networks. This high energy-efficient property stems from the choice of a resistive

yet ion-intercalation-sensitive channel material TiO₂. Furthermore, with a 10 nm TiO₂, the intercalation process of Li ion happens at a fast pace without the solid-state diffusion limit. This has an important effect for SynTs because the conductance modulation can be stimulated by fast gate voltage pulses. This important phenomenon will be discussed thoroughly in Section 2.4.

2.4. Electrochemical Analysis of Li⁺ Intercalation

In the specific context of SynTs there is a correlation between conductance modulation and the various ion exchange reactions taking place in the electrodes' bulk and at the interfaces with the solid electrolyte.^[55] In the following, the study of a vertical Li_xTiO₂/LiPON/Li structure has been carried out in an effort to investigate the channel Li_xTiO₂ electrochemical reactions and the relative uncorrelated effects on our SynT electrical response. The corresponding results are presented in **Figure 5**.

The vertical structures (Figure 5a) showed an average OCV around 1.5 V after fabrication, thus substantiating a diffusion of Li⁺ ions into TiO₂ during LiPON deposition.^[41,56,57] A first charge (delithiation) capacity corresponding to an initial Li_{0.32}TiO₂ stoichiometry (Figure 5b) corroborated this fact and agreed with values obtained at the SynT level (Figure S8 in the Supporting Information). Furthermore, the following discharge (lithiation) exhibited an unexpected potential profile (1 V plateau) and a high (Li_{1.3}TiO₂) capacity; both characteristics have been already reported^[36,37] and attributed to an activation process.^[58] Subsequent cycling curves have consistent features, revealing the highly reversible ion (de)intercalation reactions.

Figure 5c presents results of cyclic voltammetry (CV) analysis that has been carried out in order to compare the TiO₂ response upon ion (de)intercalation in two configurations: lithium excess (vertical structure) and deficiency (SynT). Li⁺ ions can be intercalated into TiO₂ with the consecutive reduction of Ti(IV) to Ti(III) redox centers, given as



with $0 \leq x \leq 1$. In a lithium excess configuration, TiO₂ films show broad anodic and cathodic peaks (at 1.88 and 1.66 V, respectively) corresponding to Li⁺ ion intercalation. However, in a lithium deficiency configuration, anodic and cathodic peaks

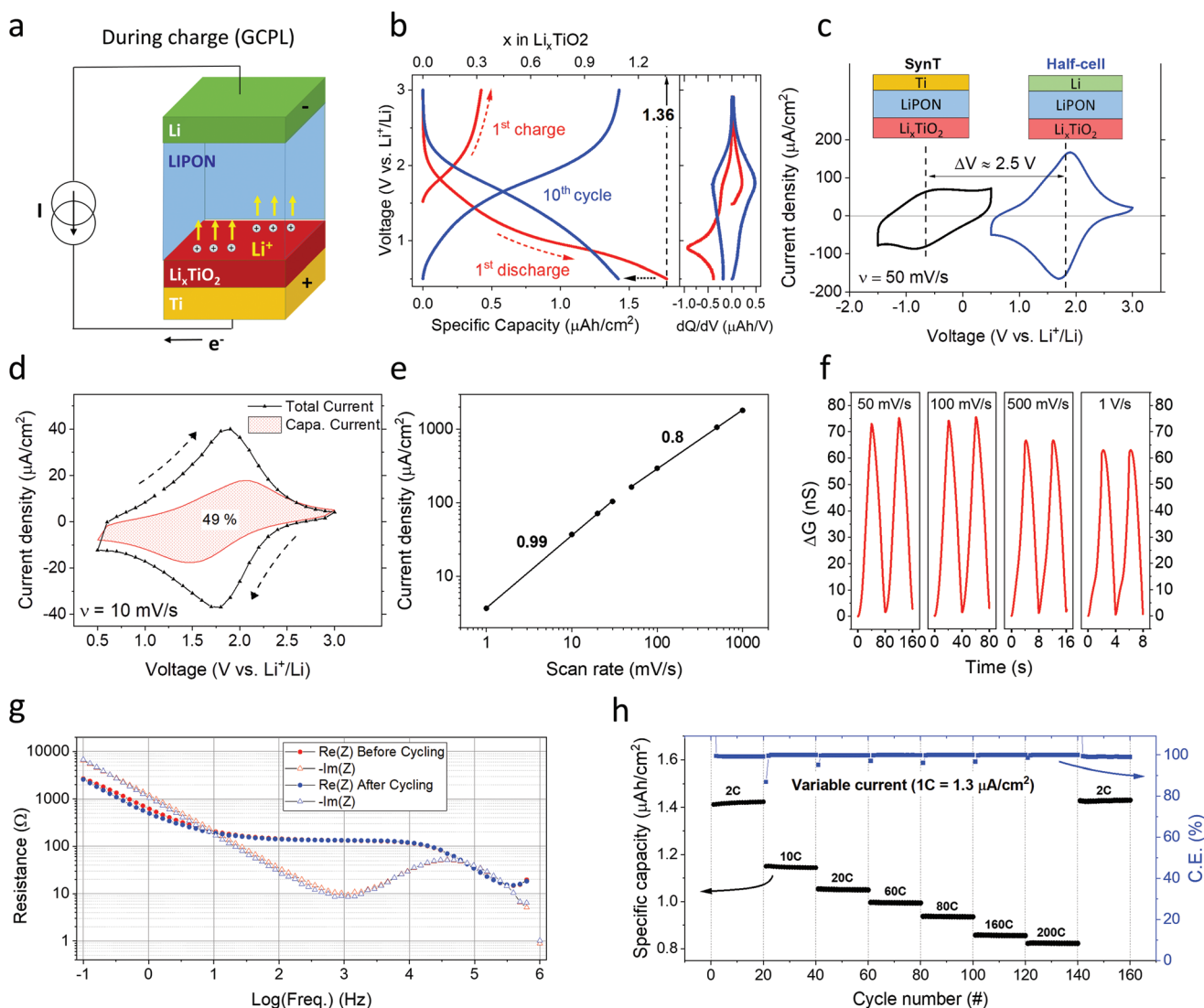


Figure 5. a) Schematic view of Ti/Li_xTiO₂/LiPON/Li vertical structure during GCPL charge process. b) Comparison of 1st and 10th cycle upon GCPL (The cell is charged to 3.0 V and discharged to 0.5 V with the current density of ±2.6 μA cm⁻²). c) Voltammogram comparison of transistors and vertical structure. d) CV study at 10 mV s⁻¹ and the calculated pseudocapacitive current contribution. e) Logarithmic relationship between cathodic peak current (Li⁺ insertion) and scan rates between 1 mV s⁻¹ and 1 V s⁻¹. f) The source–drain conductance modulation under the increasing Gate voltage scan rates from 50 mV s⁻¹ to 1 V s⁻¹. g) EIS spectra (at V = 1.2 V) before and after 100 CV cycles. h) Specific capacity and Coulombic efficiency variation with current density and cycle number.

(−0.5 and 0.8 V, respectively, see Figure S9 in the Supporting Information, for peak potential explanation) exhibit lower current densities due to insufficient ion quantity for a complete (de)intercalation reaction ($x_{\text{available}} = 0.32$). Notwithstanding, the potential window of the redox peaks corresponds to the largest variation of electronic conductance, highlighting the correlation between both phenomena (Figure S10 in the Supporting Information).

To further investigate the Li⁺ ion (de)intercalation kinetics, additional CV experiments of vertical structures were performed at varying scan rates (Figure 5d,e). The reaction kinetics is resolved by examining the variation of peak current (i_p) with scan rate (ν) using the power-law relationship^[59]

$$i_p = a\nu^b \quad (5)$$

where the b -value of 0.5 indicates a diffusion-controlled process and the value of 1 suggests a surface-controlled or diffusion-irrelevant capacitive behavior.

An examination of the CV scan rate dependence allows discriminating quantitatively the contributions of diffusion and surface controlled processes to the current response at a fixed potential (Figure 5d; and Figure S11 in the Supporting Information) following^[60]

$$i(V) = k_1\sqrt{\nu} + k_2\nu \quad (6)$$

Interestingly, pseudocapacitive contribution dominates, overwhelmingly, the stored charge in TiO₂ over the entire potential window at scan rates between 10 mV s⁻¹ and 1 V s⁻¹ (51% and 90%, respectively). Consequently, a higher SynT performance

is expected using such channel material insofar as diffusion-controlled processes are completely inefficient in these conditions. The high rate incorporation of Li into amorphous TiO₂ is a unique characteristic that allows fast conductance modification at the channel of SynT. Figure 5e presents a plot of log (i) versus log (v) for the redox peaks of TiO₂. It is shown that the material exhibits fast surface driven intercalation ($b = 0.99$) up to 50 mV s⁻¹ and remains the predominant contribution ($b = 0.8$) up to 1 V s⁻¹, which is consistent with the extrinsic pseudocapacitive intercalation in amorphous TiO₂.^[36,37,61,62] In the literature, a mixed intercalation process was reported for this system. Ye et al. suggested that the separation of b values for amorphous TiO₂ is due to deeper sites in bulk being inaccessible for Li⁺ ion intercalation on higher scan rates, thus decreasing the gravimetric current response with the increase of the thicknesses.^[37]

Figure 5f depicts the recorded variation of G_{SD} and its change of maximum conductance when experiencing increasing sweeping rates of V_G within the voltage range of $V_G = [-0.5, 1.5 \text{ V}]$. For a full programming cycle (50 states of potentiation and 50 states of depression, in this voltage range), the average voltage difference between two adjacent states is calculated to be 40 mV. Thus, with such potential gap, the switching time for 50 mV s⁻¹ sweeping rate is 0.8 s. Similarly, we have 4 ms switching operations at 1 V s⁻¹, while maintaining the “M-shaped” conductance modulation with only a 7% decrease of G_{max} . This observation highlights the beneficial effect of TiO₂ pseudocapacitive behavior to alleviate kinetic inhibition in all-solid state configuration. In addition to TiO₂, other intercalation materials serving as channels (LiCoO₂, WO₃, etc.) can be engineered to be “extrinsic pseudocapacitive” materials by thinning their film thickness to a few nanometers, thus significantly reducing the ion diffusion length and making the whole system more agile in terms of operation.^[63] The electrochemical impedance spectroscopy (EIS) plots remain unchanged over 100 cycles (Figure 5g), proving consistency with a major and stable ion conductor contribution (ion conductivity $\sigma_{LiPON} = 0.5 \mu\text{S cm}^{-1}$, characteristic frequency $f_{cLiPON} = 38 \text{ kHz}$, see extraction details in Figure S12, Supporting Information).

The specific capacity and coulombic efficiency (CE) per cycle are shown in Figure 5h (Supporting Information). CE is the ratio of total charge extracted out of active material to the total charge inserted into the active material over a cycle. Here we demonstrated a high rate capability of TiO₂ electrode with a capacity fading less than 50% for a 100 times current rate increase. As the current density was switched back to the low current rate, the capacity recovered its initial value. This recovery of the total capacity indicated that the capacity fading with incremental current rate was only related to kinetics limitation, and not material degradation or parasitic reactions. This high rate and reversibility were also confirmed by $\approx 100\%$ CE. These characteristics of TiO₂ confirmed a high-quality channel material for fast intercalation operations and high endurance.

Overall, the electrochemical study allowed proving that i) TiO₂ was initially lithiated up to 0.32 Li, ii) the initial lithiation was reversible, iii) the electronic conductance modulation was correlated to (de)intercalation reactions of Li⁺ ions in TiO₂, and iv) TiO₂ exhibited a pseudocapacitive behavior, with a fast and

reversible (de)intercalation thus conferring to SynTs high performances in terms of response time and endurance.^[64]

3. Conclusion

In summary, we report a low energy consumption, all-solid-state SynT prepared with wafer-scale microfabrication processes. The devices were assembled with an amorphous 10 nm thick TiO₂ channel and a LiPON electrolyte in a vertical configuration facilitating fast ions doping, nano-Siemens conducting level, and femtojoule writing energy. Synaptic plasticity characteristics required for an artificial synaptic component are also demonstrated. The stability and endurance of the transistors are confirmed by more than 1000 cycles and 10⁵ reversible programming states in ambient conditions. With the SynTs' experimental results as inputs, the simulated crossbar array obtained high accuracy of 95.5% on MNIST pattern recognition tests.

We proposed a systematic study of the vertical structures, involving several kinds of electrochemical characterizations. These investigations revealed valuable information on the electrochemical reactions which occur: i) contribution of the channel bulk and its interfacial region, ii) electrolyte contribution, and iii) the reaction mechanism reversibility. Therefore, we can make a clear correlation between electrochemical reactions and the performance characteristics of our Li_xTiO₂-based three-terminal devices. The fast operation rate stemmed from the rapid Li diffusion into the pseudocapacitive amorphous TiO₂ layer, while high ionic activities around the potential 1.68 V versus Li⁺/Li suggested a highly efficient working voltage range. The EIS and rate capability tests further confirmed the TiO₂ thin film's resilience under different sweeping rates, thus making it an appropriate channel material for SynTs used for online training and high-speed, low-power neuromorphic systems.

In future work, the writing energy can be reduced by shrinking the dimensions of the devices. Miniaturization of the area for the gate stack has been reported to be practical to reduce the power spent on programming SynTs.^[23] Similarly, by thinning the TiO₂ amorphous channel, the electrical conductivity is lower horizontally and faster vertically in terms of Li incorporation into ultrathin pseudocapacitive films. However, to assure the amount of mobile Li in the system, a stoichiometric LiTiO₂ is compulsory. Instead of relying on the passive Li diffusion after the PVD LiPON step, we will develop an ALD technique that allows depositing lithiated TiO₂ film.

4. Experimental Section

Elaboration of SynT and EC Half-Cell: All the devices used on this study were fabricated on 8" Si wafers with 300 nm SiO₂ grown thermally to serve as a dielectric insulator layer. The transistor is composed of several different layers, namely 300 nm Ti bottom metal, 10 nm TiO₂ channel, 200 nm LiPON electrolyte, and 300 nm Ti top metal. While Ti and LiPON layers were deposited by physical vapor deposition (CVD) in an Endura PVD 200 mm tool (Applied Materials) equipped with Ti and LiPO₄ sputtering targets, ALD of thin film TiO₂ was performed in Savannah ALD tool (Cambridge NanoTech) with Tetrakis(dimethylamido) titanium (TDMAT) as precursor and water as oxidant. The devices were

prepared by successive deposition and patterning of each layer using UV photolithography and etching, details can be found in Figure S1 of the Supporting Information. Photoresists employed to realize the photomask are positive MICROPPOSIT S1818 and Shipley SPR 220. Bottom Ti metal electrodes were formed using $1\text{H}_2\text{O}_2:1\text{H}_2\text{O}:1\text{NH}_4\text{OH}$ etching solution. TiO_2 was patterned using Reactive Ion Etching (RIE) technique with CHF_3/Ar plasma inside the reactor of a Corial tool (Plasma-Therm). The wafer was then annealed with Rapid Thermal Annealing (RTP) at $400\text{ }^\circ\text{C}$ for 30 min under air exposure. After depositing both layers LiPON and Ti on top of TiO_2 layer to form a vertical gate stack, the Ti gate metal was etched using the same RIE method. The transistor was completed by patterning the electrolyte LiPON with a TMAH aqueous solution. For the half-cell devices, bottom electrode Ti and active material TiO_2 were patterned in a similar manner. LiPON electrolyte and Li metal were deposited on the wafer via shadow masking by RF-magnetron sputtering and thermal vaporization, respectively.

Physical Characterization Methods: A cross section of SynT was imaged with a MERLIN scanning electron microscope (ZEISS) coupled with focused ion beam (FIB) (HELIOS 450 S). The image was taken with a 45° tilted sample using 6 kV electron beam energy and 1.1 nA beam current. A 9 nm carbon layer was locally deposited to avoid electrostatic charging and improve the quality of the images. The elemental distribution of sample was subsequently analyzed by energy-dispersive X-ray spectroscopy (EDS) with secondary electron detector (HESE2) and energy selective backscattered detector (ESB). A closed-up image of the Ti/ TiO_2 /LiPON stack to visualize the thin TiO_2 channel was obtained by performing high-resolution transmission electron microscopy (HRTEM) technique (Jeol 3010) at 400 kV.

Electrical Characterizations: The electrical and electrochemical experiments were carried out using a VMP3 potentiostat (Biologic), and controlled by EC-lab program. For the transistors, the tests were done using a low current measurement set up placed inside a Faraday cage to eliminate the possible electromagnetic noise. SynTs were characterized under ambient testing conditions at $25\text{ }^\circ\text{C}$ and ambient humidity. Half-cell electrochemical characterizations were conducted in an Ar glovebox (O_2 and H_2O level at 1 ppm) at $25\text{ }^\circ\text{C}$ to avoid air exposure of Li and LiPON. Electrochemical study was done on the half-cell devices with 23.7 and 37.5 mm^2 top electrode area. To quantify the amount of diffused Li inside TiO_2 layer, Galvanostatic Cycling with Potential Limit (GCPL) was employed. A constant current of $1\text{ }\mu\text{A}$ has been applied to a cell with 37.5 mm^2 top electrode area, giving a density current of $2.67\text{ }\mu\text{A cm}^{-2}$, to extract Li from the Li_xTiO_2 layer with the potential limit from cell's OCV to 3 V (the charge process). The subsequent intercalation of Li^+ was driven by a current of $-1\text{ }\mu\text{A}$ until the cell potential reached 0.5 V (the discharge process). A threshold of 0.5 V versus Li^+/Li was established as in the half-cell configuration, decreasing OCV further can affect the cell performance due to over flooding the active layer with Li (overdischarge).^[65,66] In the rate capability test, the cell with increasing current densities of 2.67, 26.7, 53.4, 80.1, 106.8, 213.6, $267\text{ }\mu\text{A cm}^{-2}$, and each current step was cycled 20 times, was charged and discharged.

Crossbar Simulation: The crossbar simulation was performed on the CrossSim platform.^[22,52,53] It provides a python-based simulator that allows different algorithms to be built upon resistive memory crossbars, while taking into account the realistic features of artificial synaptic devices. Supervised learning was executed on a three-layer neural network with one hidden layer using two data sets: a small image version (8×8 pixels) of handwritten digits from the "Optical Recognition of Handwritten Digits" dataset and MNIST dataset, a large image version (28×28 pixels) of handwritten digits. The simulation was based on backpropagation algorithm using experimental long-term synaptic plasticity (LTP, LTD) characteristics.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

electrochemical reactions, electronic devices, neuromorphic computing, surfaces interfaces and thin films, synaptic transistors

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