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Voltage Offset Compensation in CMOS OTAs: Novel Approaches for Temperature Drift Improvement

Vratislav MICHAL
STMicroelectronics, Imaging division, 12 rue Jules Horowitz, France
vratislav.michal@st.com

***Abstract* — This invited paper introduces novel approaches for trimming the voltage offset of CMOS operational amplifiers and comparators. The presented methods can be applied either to a one-time trimming during production testing, or *via* periodic calibration during circuit operation. The primary focus of this paper is to optimize the temperature drift of the trimmed and untrimmed offset voltage, V_{OS}. The paper discusses various approaches to achieve this goal, including *a*) constant current injection, *b*) MOS physical size programming, and *c*) tail offset voltage trimming. Furthermore, the paper introduces new techniques that enhance temperature drift performance: *d*) temperature compensated current offset injection, *e*) temperature compensated active load trimming, *f*) constant-resistance tail offset voltage trimming, and *g*) series input-referred voltage generator. Additionally, the paper introduces the concept of transconductance temperature characteristic dumping, which has the potential to improve the residual temperature drift of the OTA. Simulation in 130nm CMOS demonstrating the effectiveness of the presented methods are provided.**

***Index Terms*—Voltage offset trimming, OTA offset-voltage temperature drift, static offset compensation, low-offset design. transconductance temperature characteristics dumping.**

I. INTRODUCTION

Analog comparators and operational amplifiers play a crucial role in CMOS analog circuit design. However, the accuracy of related analog functions is limited by the input-referred offset voltage, V_{OS}, which arises from device mismatch. Traditional source-coupled differential pairs used in such devices typically achieve an input offset voltage V_{OS} below ±5mV [1 - 4]. To attain desired circuit performance, offset compensation (trimming) is employed to reduce V_{OS}.

Random offset voltage arises from the mismatch due to the process variations in a supposedly identical pair of devices. In the most widely used OTAs depicted in *Fig. 1,* which form the base of the majority of operational amplifiers and comparators, input offset voltage V_{OS} is primarily caused by the mismatch in the differential pair $M_{1,2}$, and in the active load composed of current mirrors $M_{(3,4),(5,6),(7,8)}$. The main contributors to the mismatch are the parameters associated with the first-order saturated drain current equation [1]:

$$I_D = \frac{1}{2}\mu_x C_{ox}\frac{W}{L}\left(V_{GS}-|V_{TH}|\right)^2 = \frac{\beta}{2}\frac{W}{L}\left(V_{GS}-|V_{TH}|\right)^2 \quad (1)$$

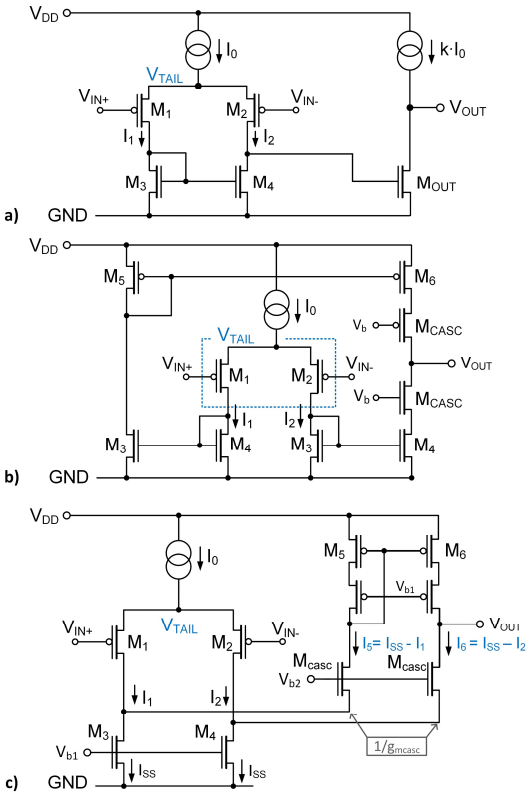

Fig. 1. Basic OTA structures used as the basis for operational amplifiers and comparators [1], [2]: *a*) two gain stages Miller OTA, *b*) single gain stage symmetrical OTA and *c*) folded cascode OTA with single gain stage.

namely threshold voltage V_{TH} and transconductance parameter $\beta = \mu_{n,p}C_{ox}(W/L)$. The parameter β depends on the electron/hole mobility $\mu_{n,p}$, gate oxide capacitance per unit area C_{ox}, and channel aspect ratio W/L. In saturation, the gate source voltage, V_{GS}, can be expressed from (1) as:

$$V_{GS} = V_{TH} + V_{OV} = V_{TH} + \sqrt{\frac{2I_D}{\mu_{n,p}C_{ox}}\frac{L}{W}} \quad (2)$$

A small change ΔV_{GS} leads to a corresponding change ΔI_D, which can be determined by evaluating the transconductance, g_m, obtained as the derivative of (1):

$$g_m = \sqrt{2\mu_{n,p}Cox\frac{W}{L}I_D} = \sqrt{2\beta I_D} \quad (3)$$

Besides the layout quality, matching errors roughly follow the Pelgrom model [3], [4] associating contributions $\sigma(\Delta V_T)$ and $\sigma\,(\Delta\beta/\beta)$ with transistor effective area $W{\cdot}L$:

$$\sigma(\Delta V_T) = \frac{A_{VT}}{\sqrt{WL}}, \quad \sigma\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta}{\sqrt{WL}} \quad (4)$$

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In this model, A_{VT} and A_{β} are mismatched parameters. In some specific cases (*e.g.,* sub-µm devices with halo implant), area $W{\cdot}L$ refers only to the implant pocket active area that has a dominant mismatch contribution. Improving matching by increasing differential pair area implies severe increase in parasitic capacitance and silicon area. Compared to this, offset reduction by circuit design allows to preserve reasonable area efficiency and the frequency characteristic of the operational amplifier or comparator.

Generally, offset reduction is implemented by static or dynamic offset compensation [1], [4], [5]. Dynamic cancellation involves periodic offset sampling and subtracting it from the input signal. This technique enables the offset to be reduced to extremely low levels, even in the sub-µV range [6]. However, despite its advantages, dynamic offset compensation through sampling or chopping leads to reduced bandwidth, introduction of spurious noise components, and increased power consumption.

The static compensation methods discussed in this paper aim to perform the offset calibration once, *e.g.* during circuit post-fabrication test at EWS (Electrical Wafer Sort), during circuit power-on, or with a slow rate during circuit operation [4], [7]. The offset voltage is being reduced by a modification of the OTA DC operating point. Due to the discrete steps, the trimming has limited resolution, usually fraction of mV. Static compensation also exhibits temperature drift dV_{OS}/dT, which originates from uncorrelated temperature contributions ΔV_T and the transconductance parameter $\beta_{n,p}$ of (1) [1].

The remainder of this paper is organized as follows: In *section II* a list of methods allowing the offset compensation is introduced. *Section III* presents the general offset equations and fundamental thermal characteristics of the MOS transistor. The following *sections, IV – IX,* present, one by one, the methods listed in *section II* and also describe the resulting thermal behavior of V_{OS}. The primary emphasis is placed on the description of the new methods presented in *sections IV. B, V.B, VII. B, VIII., and IX*, which offer significant improvement in temperature drift and reliable improvements in offset voltage trimming.

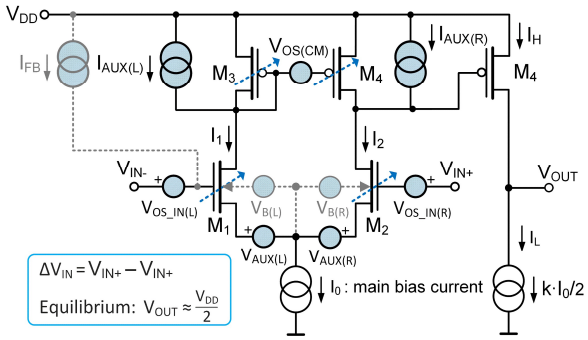

Fig. 2. Structure of NMOS Miller OTA from *Fig. 1 a*) with programmable auxiliary offset generators allowing to compensate static offset voltage V_{OS}.

II. Methods of Static Offset Compensation

The mismatch in both differential pair and active load introduces an imbalance in the DC operating point of the operational transconductance amplifier (OTA). This imbalance manifests as an offset between the currents flowing through the output branches, I_H and I_L, when $\Delta V_{IN} = 0$. At given temperature, static compensation of the offset voltage V_{OS} relies on the use of any sort of auxiliary offset generator allowing to restore the balance of I_H and I_L, resulting in $V_{OUT} \approx V_{DD}/2$ for $\Delta V_{IN} = 0$.

Fig. 2 illustrates Miller OTA with adjustable parameters, enabling effective compensation of the offset voltage V_{OS}. Methods discussed in the next chapters refer to these parameters and are listed below with corresponding section references:

- $I_{AUX(L,R)}$ *constant current injection* (*IV. A*)
- $I_{AUX(L,R)}(T)$ *temperature compensated current injection* (*IV. B*)
- W_{CM} *active load current mirror width adjustment* (*V. A*)
- $V_{OS(CM)}(T)$ *temperature compensated active load current mirror adjustment* (*V. B*)
- W_{IN} *differential pair symmetry adjustment* (*VI*)
- $V_{OS(L,R)}$ *tail offset generator with variable resistances* (*VII. A*)
- $V_{OS(L,R)}$ *constant resistance tail voltage generator* (*VII. B*)
- $V_{OS\_IN(L,R)}$ *series input-referred voltage generator* (*VIII*)
- *Transconductance temperature dumping* (*IX*).

In addition to these parameters, *Fig. 2* also incorporates the sources $V_{B(L,R)}$ and I_{FB}, which can contribute to the reduction of V_{OS}. These sources achieve the offset reduction by either programming the body-bias voltages $V_{B(L,R)}$ or by injecting I_{FB} into the feedback network of the operational amplifier. While both methods have been extensively discussed in available literature, this paper does not provide a detailed analysis of these techniques. Briefly, body-bias trimming [8] aims to adjust V_{TH} of differential pair transistors. While the trimming offset $\Delta V_{TH}/V_{B(L,R)}$ exhibits typically non-negligible temperature dependency, it provides a noticeable temperature drift of compensated V_{OS}. The method of injecting programmable current, $I_{FB,}$ into the feedback network is used for operational amplifiers that incorporate feedback resistance R_{FB} between input terminal $V_{IN(-)}$ and V_{OUT} [9]. I_{FB} circulating in R_{FB} produces an output voltage offset $\Delta V_{OUT} = I_{FB}{\cdot}R_{FB}$, that can provide reliable compensation of the output voltage offset given by the gain of the feedback network and V_{OS} of the OTA.

Offset trimming can be implemented in various ways [4], [7]. The most straightforward is a digital sweep of one of the above-mentioned parameters, while the OTA is in an open-loop configuration (*e.g.*, as comparator), and with shorted inputs. Trimming is completed with the transition of V_{OUT}. Demonstrations presented in this paper use this technique and are based on infinitesimal LSB trimming steps, ideal trimming resistances R_{OS}, and transistors with shorted source-bulk terminals. These simplifications allow to highlight the ideal limits of the presented offset compensation methods.

Offset compensation can also be implemented at the system level, such as by trimming the reference voltage of a signal processing chain. In such scenarios, it becomes important to minimize the temperature drift of the OTA's V_{OS}, without requiring the offset compensation. This aspect is addressed in *Section IX*.

III. Offset Sources in CMOS OTA

The 1st gain stage of a typical CMOS comparator or operational amplifier contains a source-coupled differential pair and one or more current mirrors operating as an active load (*Fig. 1*) [1], [2]. Ideally, when $\Delta V_{IN} = 0$, currents at the output branch are balanced and $V_{OUT} \approx V_{DD}/2$.

When hysteresis is incorporated into the comparator, V_{OS} relates also to the accuracy of the hysteresis window. Satisfactory accuracy can be provided by resistive feedback hysteresis. However, if the hysteresis is implemented within the OTA structure (*e.g.*, through positive feedback in the

active load), the hysteresis window may experience variations and thermal drift that exceed the initial V_{OS}. In such a case, unipolar hysteresis, or digital post-processing can be envisaged to improve accuracy [4].

A. General input reffered offset equation

Input referred offset V_{OS} originating from $\Delta V_{TH(IN)}$ and $\Delta(\beta/\beta)_{IN}$ of M_1 and M_2 can be expressed as:

$$V_{OS(IN)} = -\frac{\Delta\beta_{IN}}{\beta_{IN}}\frac{V_{GS(IN)} - V_{TH(IN)}}{2} + \Delta V_{TH(IN)} \quad (5)$$

Usually large aspect ratio $(W/L)_{IN}$ results in relatively low overdrive voltage V_{OV} of M_1 and M_2 (2). In this case, dominant component of (5) is $\Delta V_{TH(IN)}$. In a case of a large $(W/L)_{IN}$ and lower differential pair bias current, the differential pair may operate in the subthreshold region. In this case, (5) is no longer applicable. While the subthreshold operation can offer advantages such as improved differential pair transconductance $g_{m(IN)}$ (14), it may also result in a slight degradation of the temperature drift of V_{OS}.

The mismatch $\Delta V_{TH(CM)}$ and $\Delta(\beta/\beta)_{CM}$ in the active load current mirror generates offset between I_1 and I_2. Offset $\Delta I_{CM}/I_{D(0)}$ in OTA current mirror can be written as:

$$\frac{\Delta I_{CM}}{I_{D(0)}} = \frac{\Delta\beta_{CM}}{\beta_{CM}} - \frac{2\Delta V_{TH(CM)}}{V_{GS(CM)} - V_{TH(CM)}} \quad (6)$$

where $I_{D(0)}$ refers to the drain current *e.g.*, $I_{D(0)} = 0.5 \cdot I_0$ in *Fig. 2* OTA. Compared to the differential pair, current mirror preferably operates with high overdrive (low W/L and therefore low current mirror transconductance $g_{m(CM)}$), which helps to minimize the offset ΔI_{CM}. The folded cascode OTA shown in *Fig. 1 c*) advantageously reduces $I_{D(0)}$ of the current mirror $M_{5,6}$. The offset ΔI_{CM} is referred to the input V_{OS} as:

$$V_{OS} = V_{OS(IN)} + \frac{\Delta I_{CM(1)}}{g_{m(IN)}} + \frac{\Delta I_{CM(2)}}{g_{m(IN)}} \quad \ldots \quad (7)$$

where $\Delta I_{CM(n)}$ corresponds to the contribution of respective current mirror in the OTA.

Eqs. (5), (6) and (7) can be rewritten to emphasize their dependence on the bias current I_0. The offset (5) generate by the differential pair in saturation can be re-written as:

$$V_{OS} = -\frac{\Delta\beta_{IN}}{\beta_{IN}}\frac{\sqrt{I_0}}{2\sqrt{\beta_{IN}}} + \Delta V_{TH(IN)} \quad (8)$$

and then offset (6) generated by the current mirror as:

$$\Delta I_{CM} = \frac{I_0}{2}\left(\frac{\Delta\beta_{CM}}{\beta_{CM}} - \frac{2\sqrt{\beta_{CM}}}{\sqrt{I_0}} \cdot \Delta V_{TH(CM)}\right) \quad (9)$$

Previous equations combined by using (7) express the total input-referred offset V_{OS} as a function of uncorrelated contributions of design variables β, I_0, and matching errors $\Delta(\beta/\beta)_{IN,CMn}$ and $\Delta V_{TH(IN,CMn)}$. This results in a general offset formula of an OTA with transistors operating in saturation:

$$V_{OS} = \Delta V_{TH(IN)} + \frac{\sqrt{I_0}}{2\sqrt{\beta_{IN}}}\left\{\frac{\Delta\beta_{CMn}}{\beta_{CMn}} - \frac{\Delta\beta_{IN}}{\beta_{IN}}\right\} - \frac{\sqrt{\beta_{CM} I_D}}{\sqrt{\beta_{IN} I_0}}\Delta V_{TH(CMn)} \quad (10)$$

For OTA with n current mirrors, $\Delta(\beta_{CMn}/\beta_{CMn})$, and $\Delta V_{TH(CMn)}$ scaled by appropriate $I_{D(0)}$ should be included in (10). In subsequent discussions, ΔV_{TH}, $\Delta\beta/\beta$, and I_0 are considered, to the first order, temperature and bias current independent. Compared to this, β_{IN} and β_{CM} have strong temperature dependency [1]. Generally, temperature behavior of the terms in *Eq*.(10) can be described as:

a) For differential pair with low overdrive, or in subtreshold region, $\Delta V_{TH(IN)}$ is the primary factor contributing to V_{OS}. It represents the V_{TH} difference between differential pair transistors $M_1 - M_2$. Its value depends on the area $(W \cdot L)_{IN}$ (4). As detailed in *section III. B*., $\Delta V_{TH(IN)}$ exhibits very good temperature stability, leading to a low drift $dV_{OS}/d\mathrm{T}$ of the uncompensated V_{OS}, as demonstrated in *Fig. 4*.

b) Mismatch $\Delta\beta_{IN}/\beta_{IN}$ and $\Delta\beta_{CMn}/\beta_{CMn}$ arises from lithographic inaccuracies and carrier mobility spatial gradient, and are both weighted by $\sqrt{(I_{0,D(0)}/(4\beta_{IN}))}$. Theirs contribution depends on the bias current I_0 or $I_{D(0)}$, transconductance parameter $\beta_{IN} = \mu_{n,p}C_{ox}(W/L)_{IN}$ and the area of the input differential pair and coresponding current mirror transistors. In case of low-overdrive differential pair and high-overdrive current mirror, the overall contribution of this term is relatively small.

c) $\Delta V_{TH(CMn)}$ coresponds to the threshold voltage offset of the current mirror n. $\Delta V_{TH(CMn)}$ is reffered to the input by the transconductance ratio $g_{m(CMn)}/g_{m(IN)}$, coresponding to the voltage gain between the gates of the current mirror n and the input terminals. While this ratio is usually lower thean unity, the overall contribution of all $\Delta V_{TH(CMn)}$ is lower than $\Delta V_{TH(IN)}$. The dependency of $g_{m(CMn)}$ on $\sqrt{\mu_{n,p}}$ eliminates the temperature contribution of $\sqrt{\beta_{CM}/\beta_{IN}}$ term when the channel dopping polarity of the differential pair and the current mirror n is identical. In such a case, $\Delta V_{TH(CMn)}$ contributes to V_{OS} with very low temperature drift, similar to $\Delta V_{TH(IN)}$. In the opposite case, the temperature characteristic of $\sqrt{\beta_{CM}/\beta_{IN}}$ arises from the ratio $\sqrt{\mu_{CM}/\mu_{IN}}$, which is specific for a given process*.

B. Thermal characteristic of the differential pair

The drain current described by the quadratic equation (1) and its corresponding V_{GS} (2) and g_m (3) are affected by various process parameters, including the electron or hole mobility $\mu_{n,p}$, oxide capacitance C_{OX}, aspect ratio W/L, and V_{TH}. Among these parameters, W/L is associated with the physical channel dimensions, while C_{OX} relates to the dielectric thickness and permittivity, both of which exhibit minimal temperature dependency and are considered as inherently temperature stable.

In contrast to that, $\beta_{n,p}$ and consequently g_m (3) is a function of the carrier mobility $\mu_{n,p}$. Its temperature dependency is typically described as [10], [11]:

$$\mu_{n,p}(T) = \mu_{n,p}(T_0)\left(\frac{T}{T_0}\right)^{-x} \quad (11)$$

where x is a process-depended constant $x \approx 1.5$. By exploring $\mu_{n,p}(\mathrm{T})$, an increase of the mobility can be observed at low temperature. Although both μ_n and μ_p results from different scattering mechanism, their temperature evolution tends to be similar for given process. In this favorable case, it enables the attenuation of the contribution related to $\Delta V_{TH(CM)}$ in (10).

Temperature shift of V_{TH} originates from the physical processes occurring in the MOS capacitor. Fairly precise model of $V_{TH}(\mathrm{T})$ is a linear function with constant temperature drift of – (1 to 4) $mV/^{o}C$ [11]:

$$V_{TH}(T) = V_{TH}(T_0)\left[1 + \alpha_{THX} \cdot (T - T_0)\right] \quad (12)$$

*As example, $\sqrt{\mu_n/\mu_p}$ corresponding to PMOS differential pair and NMOS current mirror reach value of ≈ 1.8. For the temperature range of –40ºC to +125ºC, it exhibits a variation in range of approx. +5% to –5%. Considering $g_{m(CM)}/g_{m(IN)} = 0.2$, $\Delta V_{GS(CM)}$ of 5mV contribute to the temperature drift of V_{OS} by ±50µV in given temperature range. Lowering this contribution can be achieved by decreasing $\Delta V_{GS(CM)}$, increasing $g_{m(IN)}/g_{m(CM)}$ ratio or eventually by use the method of the transconductance temperature dumping described in *section IX*.

Example of the temperature characteristics of the differential pair with intentionally introduced mismatch $\Delta V_{TH(IN)}$ and $\Delta\beta_{(IN)}$ is shown in *Fig. 3*. In this figure, difference $\Delta g_{m(M1,2)}$, $\Delta V_{TH(M1,2)}$, and $\Delta I_{M1,2}$ can be observed. While $\Delta\beta_{IN}$ is partly responsible for $\Delta g_{m(M1,2)}$, primary factor responsible for this difference is the unequal drain currents $I_{1,2}$ of M_1 and M_2, originating from $\Delta V_{TH(IN)} \cdot g_{m(IN)}$.

On the other hand, both $V_{TH(M1)}$ and $V_{TH(M2)}$ exhibit thermal dependency described by identical (12). As a result, changes in ambient temperature do not significantly affect their difference $\Delta V_{TH(IN)}$. Generally, transistor statistical models ignore this parameter, as shown in *Fig. 3*, where the temperature drift of $\Delta V_{TH(IN)}$ is only 76nV. Consequently, the differential pair with a low V_{OV} exhibits low temperature drift of the uncompensated offset voltage V_{OS}, when compared to the overall range of V_{OS} (see *Fig. 4* in the next section).

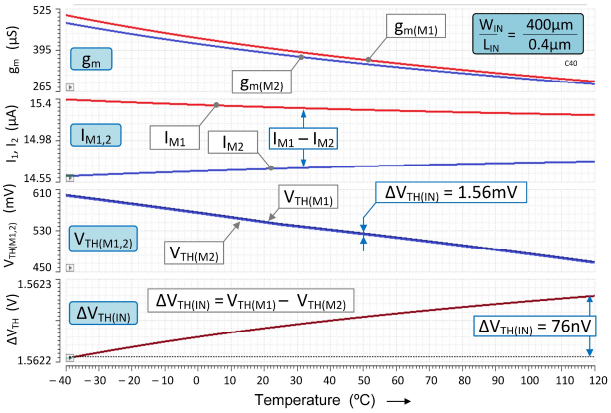

Fig. 3. Parameters of a PMOS differential pair vs. temperature for zero differential input voltage. A mismatch between M_1 and M_2 was introduced by a Monte-Carlo simulation.

C. *Simulation example of uncompensated OTA*

An example simulation of the input offset voltage V_{OS} originating from random process parameters variation (Monte-Carlo simulation) is shown in *Fig. 4*. The figure shows V_{OS} *vs*. temperature characteristic revealing offset peak values ranging from –3.5mV to +3.5mV (σ = 950µV). Compared to this, the temperature drift dV_{OS}/dT of the offset voltage is relatively small due to stable $\Delta V_{TH(IN)}$.

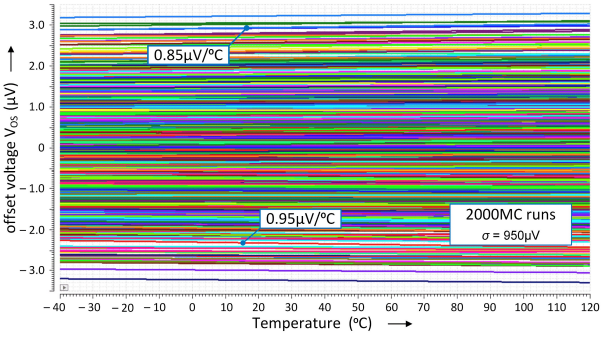

Fig. 4. Simulated temperature characteristic of uncompensated offset voltage V_{OS} of the OTA with PMOS differential pair. Simulation parameters were: $W/L_{1,2}$ = 160µ/1µ, $W/L_{5,6}$ = 40µ/2µ, $W/L_{5,6}$ = 20µ/2µ, I_0 = 30µA.

The simulation was conducted using the folded cascode OTA illustrated in *Fig. 1 c*). This folded cascode includes a gain stage based on the current mirror $M_{5,6}$ with the same channel polarity as the input differential pair (*i.e.* PMOS in *Fig. 1 c*). This ensures temperature stable term $\sqrt{\mu_{CM}/\mu_{IN}}$ and thus a stable contribution of $\Delta V_{TH(CM5,6)}$ in (10), which is further reduced by the low bias current $I_{D(5,6)}$. To eliminate term $\sqrt{\mu_n/\mu_p}$ associated with the NMOS current mirror $M_{3,4}$, area and V_{OV} of $M_{3,4}$ can be increased. Resulting increased capacitance of $M_{3,4}$ can be eliminated by a low $1/g_{mcas}$, as illustrated in *Fig. 1 c*).

IV. Offset Compensation by a Programable Offset Current Sources I_{AUX}.

A. $I_{AUX(L,R)}$ *constant current injection*

Injecting a programmable current, $I_{AUX(L,R)}$, into one of the differential pair drain terminals allows to reach the equilibrium, $V_{OUT} \approx V_{DD}/2$, for zero input voltage, $\Delta V_{IN} = 0$ [12]. Adjustable current sources $I_{AUX(L,R)}$ are usually implemented as current steering DACs with discrete steps. The value of discrete step is determined by required LSB offset trimming step and can be very small, reaching nA range. I_{AUX} can be implemented either as a bipolar (*i.e.* delivering positive or negative current $\pm I_{AUX}$) or, more effectively, as two unipolar current sources depicted also in *Fig. 2*. In this configuration, each current source I_{AUX} L or R is intended to compensate for the respective polarity of V_{OS}.

As the result of I_{AUX} current injection, an offset voltage, $V_{OS(IAUX)}$, appears between the input terminals V_{IN+} and V_{IN-}:

$$V_{OS(IAUX)} = \frac{\pm I_{AUX}}{g_{m(IN)}} \tag{13}$$

where $g_{m(IN)}$ is the differential pair transconductance:

$$g_{m(IN)} = \sqrt{2\mu_{n,p}Cox\left(\frac{W}{L}\right)_{IN} I_D} = \sqrt{2\beta_{IN} I_D} \tag{14}$$

For $V_{OS(IAUX)} = -V_{OS}$, compensation of the offset is achieved.

As discussed earlier, the offset voltage V_{OS} is primarily determined by thermally stable $\Delta V_{TH(IN)}$. On the other hand, differential pair transconductance $g_{m(IN)}$ contains temperature dependent term $\mu_{n,p}(T)$ related to the carrier mobility (11). This implies that the compensation (13) introduces a high temperature drift in the compensated V_{OS}.

Fig. 5 illustrates an example of the trimming outcome realized by the constant current injection trimming, using identical OTA as the simulation shown in *Fig. 4*. The offset is reduced down to µV level at the trimming temperature but increases rapidly at other temperatures. Consequently, compensating thermally stable offset $\Delta V_{TH(IN)}$ through thermally unstable transconductance $g_{m(IN)}$ leads to a significant thermal drift dV_{OS}/dT compared to the initial uncompensated V_{OS} shown in *Fig. 4*. In practical applications, automatic trimming by constant current injection should be performed periodically, or in response to changes in IC temperature.

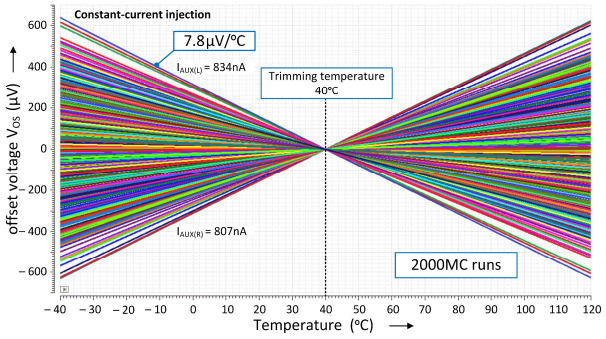

Fig. 5. Example of the compensated V_{OS} versus temperature obtained with constant current injection method. Simulation done with the identical OTA as the example from *Fig. 4*.

B. $I_{AUX(L,R)}(T)$ temperature compensated current injection

Providing $I_{AUX(L,R)}(T)$ with an appropriate thermal function improves the temperature drift of the compensation shown in the previous *section IV. A.* As a result from (13), the preferred temperature characteristic of $I_{AUX(L,R)}(T)$ is to be identical to the temperature characteristic of the input differential pair transconductance, $g_{m(IN)}(T)$ (14). In this way, compensating current $I_{AUX(L,R)}(T)$ generates a temperature-stable input offset $V_{OS(AUX)}$, that can effectively compensate temperature-stable terms in (10) .

Ref. [7] presents an OTA that incorporates an additional differential pair, generating a current, which may have the desired temperature behavior. However, it is worth noting that this approach, as discussed in the reference, necessitates the application of inconveniently small trimming voltages in the microvolt (μV) range and requires complex control of the trimming voltage common mode.

Method introduced in this section relies on the generation of the temperature pre-compensated currents $I_{AUX(L,R)}(T)$ generated by a supplementary current mirror $M_R - M_S$. This current mirror contains an auxiliary offset $V_{OS(CM)}$, applied between the gates of the reference and source transistors M_R and M_S. As shown in *Fig. 6,* the drain current of each of M_S (M_A or M_B in *Fig. 7*) will experience a shift with respect to the reference current denoted as $I_{OS}(T) = I_{REF} - I_S(T)$.

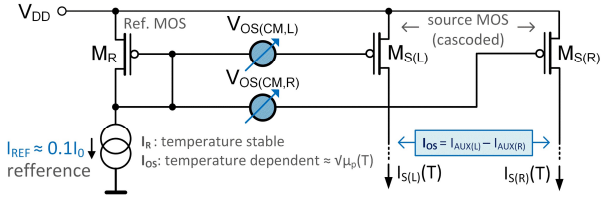

Fig. 6. Temperature pre-compensated current source generating $I_{OS}(T)$ compensating $1/g_{m(IN)}$ temperature variation of PMOS differential pair.

The shift in I_{OS} for a given temperature can be determined using the drain current formula (1) re-written for I_{REF} as:

$$I_{REF} = \frac{\mu_{n,p} C_{ox}}{2}\left(\frac{W}{L}\right)_{R,S}\left(V_{GS(R)} - V_{TH}\right)^2 \tag{15}$$

For given I_{REF}, $V_{GS(R)}$ of M_R can be isolated from (15):

$$V_{GS(R)} = V_{TH} + \sqrt{\frac{2I_{REF}}{\mu_{n,p} C_{ox}}\left(\frac{L}{W}\right)_{R,S}} \tag{16}$$

The drain current of M_S results from $V_{GS(R)} + V_{OS(CM)}$:

$$I_S = \frac{\mu_{n,p} C_{ox}}{2}\left(\frac{W}{L}\right)_{R,S}\left(V_{GS(R)} + V_{OS(CM)} - V_{TH}\right)^2 \tag{17}$$

Merging (16) and (17), and subtracting the result from I_R yields the current difference $I_{OS} = I_{REF} - I_S$:

$$I_{OS} = 2V_{OS(CM)}\sqrt{\mu_{n,p} C_{ox} I_{REF}\left(\frac{W}{L}\right)_{R,S}} - V_{OS(CM)}^2 \mu_{n,p} C_{ox}\left(\frac{W}{L}\right)_{R,S} \tag{18}$$

Here, term with $V_{OS(CM)}^2$ can be neglected. It can be observed that the remaining 1st term in (18) is comparable to the transconductance $g_{m(IN)}$ (14). By injecting I_{OS} into the differential pair, an input offset $V_{OS(AUX)}$ is induced between the input terminals V_{IN+} and V_{IN-}. This offset arises from $I_{OS}/g_{m(IN)}$ and can be expressed from (14) and (18) as:

$$V_{OS(AUX)} = 2V_{OS(CM)}\sqrt{\frac{\left(\mu_{n,p} C_{ox} I_{REF}\right)_{R,S}(W/L)_{R,S}}{\left(\mu_{n,p} C_{ox} I_0\right)_{IN}(W/L)_{IN}}} \tag{19}$$

In this equation, W/L, C_{OX}, I_{REF} and I_0 are constant terms with no temperature contribution. When considering the identical channel polarity of the differential pair and current mirror

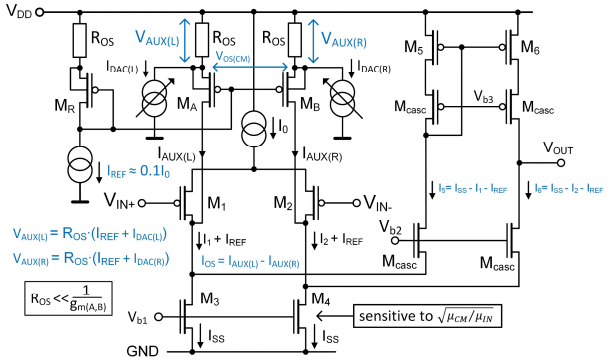

Fig. 7. Compensation by $I_{AUX(L,R)}(T)$ current injection implemented by current source M_R, M_A and M_B. $M_{A,B}$ correspond to M_S in previous equations. $R_{OS} << 1/g_{mA,B}$ allows to preserve desired $\sqrt{\mu_p}$ temperature dependency of I_{OS} (see *section IX*). Bulk terminals of $M_{A,B}$ are tied to the sources to eliminate the substrate effect.

$M_{R,S}$, the nominator and denominator terms $\mu_{n,p}$ cancel each other. In this case, (19) can be simplified to:

$$V_{OS(AUX)} = V_{OS(CM)}\alpha\sqrt{\frac{(W/L)_{R,S}}{(W/L)_{IN}}} \tag{20}$$

Here, α represents constant terms in (19). In addition to the compensation of $\Delta V_{TH(IN)}$, $I_{OS}(T)$ provides temperature-stable compensation for the $\Delta V_{TH(CM5,6)}$ term in (10) when referring to *Fig. 7* OTA. This is because $M_{5,6}$ have an identical channel polarity to the transistors $M_{1,2}$ and $M_{R,S}$. On the other hand, the $\Delta V_{TH(3,4)}$ term may originate in a residual thermal drift related to $\sqrt{\mu_n/\mu_p}$. As mentioned in *section III.A*, this contribution depends on the specific process parameters and can be reduced a large $g_{m(IN)}/g_{m(CM3,4)}$ ratio.

As shown in *ref.* [13] addressing a different application, the implementation of $V_{OS(CM)}$ between the current mirror gates is inconvenient and requires a significant number of additional biasing circuits. To address this limitation, *Fig. 7* introduces a current mirror $M_{R,A,B}$ with additional source resistances R_{OS} and programmable current sources $I_{DAC(L,R)}$. These current sources adjust the voltages $V_{AUX(L,R)}$. For unipolar current sources $I_{DAC(L,R)}$, $V_{AUX(L,R)}$ is adjusted on either the left or right R_{OS}, depending on the initial polarity of V_{OS}. Similarly to the structure shown in *Fig. 6*, the value of I_{OS} (18) is determined by the difference $I_{AUX(L)} - I_{AUX(R)}$.

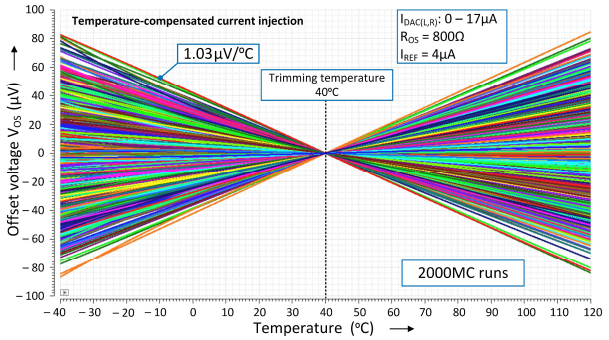

Fig. 8. Outcome of the offset compensation by $I_{AUX(L,R)}(T)$ temperature compensated current source M_R, M_A and M_B.

As described in the upcoming *Section IX*, the additional source resistances R_{OS} produce transconductance temperature dumping, which may result in degradation, but in some cases also contribute to the improvement of the temperature offset compensation effectiveness. In order to accurately reproduce the temperature behavior of $g_{m(IN)}(T)$, a small value of R_{OS}

(R_{OS} << $1/g_{m(A,B)}$) may be necessary. However, this may require a large trimming current $I_{DAC(L,R)}$. To minimize this current, a tradeoff between I_{REF}, R_{OS}, and $W/L_{(R,A,B)}$ needs to be determined through a dedicated simulations. An alternative reduction of the trimming current can be achieved by optimization *via* transconductance temperature damping method described in *Section IX*.

The simulated outcome of the offset voltage trimming is presented in *Fig. 8*. Compared to the constant current injection characteristic from *Fig. 5*, this method significantly reduces the temperature drift dV_{OS}/dT. In the case when a different structure of the OTA is used (*e.g.,* Miller OTA shown in *Fig. 1 a*)), it is necessary to provide the injection of the constant reference current I_{REF} into the output node as well. This prevents additional offset originated from the current difference between $M_{5,6}$ and M_{OUT} (see *Fig. 18*).

V. Active Load Current Mirror Adjustement

Adjusting the current mirror gain introduces a current offset, which enables reaching the equilibrium $V_{OUT} \approx V_{DD}/2$ for $\Delta V_{IN} = 0$. An example of the trimming based on the current mirror adjustment is shown *e.g.* in *ref.* [8].

A. W_{CM} active load current mirror width adjustment

Considering a programable current mirror shown in *Fig. 2* and detailed in *Fig. 9 a*) [13], a current gain parameter $k_{os} = W_{M4}/W_{M3}$ can be introduced. This parameter k_{os} is driven by a digital signal [0] – [n], enabling elementary current mirror segments [*x*]. For a given bias current I_0, the left and right currents I_L, I_R can be expressed as $I_L = I_0/(1+k_{os})$ and $I_R = k_{os}I_0/(1+k_{os})$. For the folded cascode OTA, the term $\frac{1}{2}I_0$ is to be substituted by the actual current mirror bias current. A difference $I_{OS} = I_L - I_R$ related to the parameter k_{os} can be expressed from I_R and I_L:

$$I_{OS} = \frac{1-k_{OS}}{1+k_{OS}} I_0 \tag{21}$$

This offset current can be referred to the input as $I_{OS}/g_{m(IN)}$:

$$V_{OS(AUX)} = \frac{I_0}{g_{m(IN)}} \frac{1-k_{OS}}{1+k_{OS}} \tag{22}$$

As mentioned earlier, the input differential pair transconductance $g_{m(IN)}$ exhibits strong temperature dependency. The temperature drift obtained by the current mirror width adjustment is therefore similar to the temperature drift obtained by the constant current injection method presented in *section IV. A*. In practical application, offset trimming is to be performed periodically or with the temperature change of the integrated circuit.

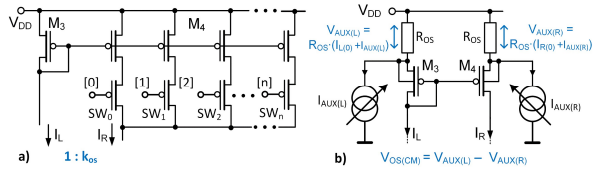

Fig. 9. Adjustment of the active load current mirror: a) adjusting the physical size (W) [13], and b) by adjusting the gate offset voltage $V_{OS(CM)}$. R_{OS} << $1/g_{m3,4}$ is required to preserve $\sqrt{\mu_p}$ temperature dependency of I_{OS}. Bulk terminals in *b*) are tied to sources to eliminate the substrate effect of $M_{3,4}$.

B. $V_{OS(CM)}$(T) *temperature compensated active load current mirror adjustement*

Another efficient method providing low temperature drift dV_{OS}/dT of the compensated offset voltage can be realized by adjusting the voltage $V_{OS(CM)}$ between the gates of the current mirror, preferably current mirror with identical channel doping polarity to the differential pair transistors $M_{1,2}$.

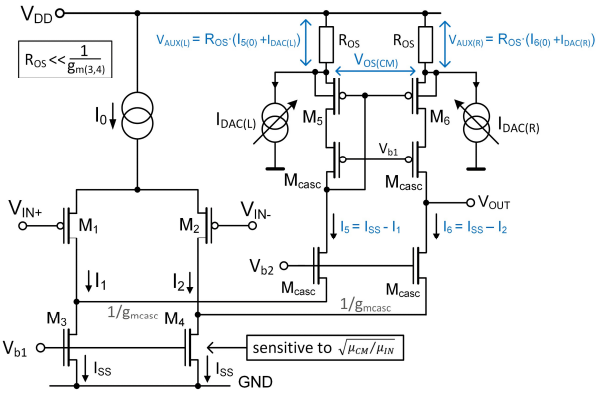

Fig. 10. Offset trimming setup for $V_{OS(CM)}$(T) temperature-compensated active load current mirror adjustment method, based on the folded cascode.

In the OTA from *Fig. 2*, $V_{OS(CM)}$ is generated between the gates of the current mirror $M_{3,4}$. Similarly, as depicted in *Fig. 7*, a more convenient implementation relies on the use of additional source resistances R_{OS}, and unipolar current sources $I_{DAC(L,R)}$. An example of this implementation is detailed in *Fig. 9 b*). Here, $V_{OS(CM)}$ results from the difference between voltage drop on the left and right resistances R_{OS}, *i.e.* $V_{OS(CM)} = V_{AUX(L)} - V_{AUX(R)}$. For $I_{DAC(L,R)} = 0$, $V_{AUX(L,R)}$ are solely determined by DC bias currents of $M_{5,6}$, and are equals.

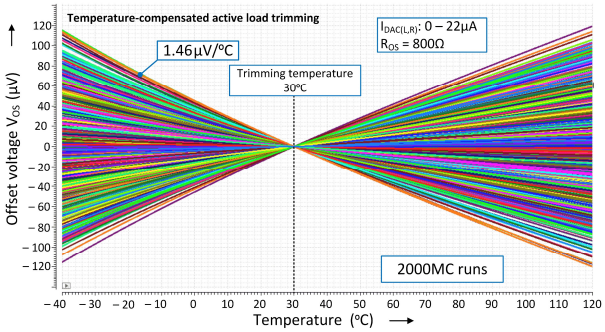

Fig. 11. Outcome of the offset compensation by the trimming of the active-load gate voltage $V_{OS(CM)}$, based on OTA from Fig. 10.

The mathematical formulation and resulting temperature characteristics of $I_{OS} = I_L - I_R$ are equivalent to the description of thermally compensated current injection described in *section IV.B*. In the equations presented in *section IV. B*, the reference current I_{REF} is to be replaced by the active load bias current, (*e.g.,* $I_{CASC} = I_{SS} - I_0/2$ in *Fig. 10* OTA). Similarly as given by (19), I_{OS} generated by the current mirror $M_{5,6}$ can be referred to the input as $I_{OS}/g_{m(IN)}$:

$$V_{OS(AUX)} = 2V_{OS(CM)} \sqrt{\frac{\left(\mu_{n,p} C_{ox} I_{CASC}\right)_{CM} (W/L)_{CM}}{\left(\mu_{n,p} C_{ox} I_0\right)_{IN} (W/L)_{IN}}} \tag{23}$$

where W/L, C_{OX} and I_0 have no temperature contribution. Compared to the realization from *section IV.B*, the mobility ratio terms $\sqrt{\mu_p/\mu_n}$ or $\sqrt{\mu_n/\mu_p}$ may remain in (23) for a configuration with a different channel polarity of the current-mirror and differential-pair. This is the case for the OTA from *Fig. 2*, where the NMOS differential pair $g_{m(IN)} \approx \sqrt{\mu_n}$ and PMOS active load $g_{m(CM)} \approx \sqrt{\mu_p}$. In such a configuration, (23) contain the term $\sqrt{\mu_p/\mu_n}$. The temperature dependency of this term can be reduced by increasing the ratio $g_{m(IN)}/g_{m(CM)}$.

In a more efficient way, the residual offset originating from the mobility ratio $\sqrt{\mu_p/\mu_n}$ can be eliminated by using an OTA where both the differential pair and the current mirror

used for trimming have the same channel polarity. For example, this is the case for the symmetrical OTA from *Fig. 1 b*) or the folded cascode OTA from *Fig. 1 c*), where both $M_{5,6}$ and differential pair are implemented by the PMOS transistors. In these cases, (23) can be simplified to:

$$V_{OS(AUX)} = V_{OS(CM)}\alpha\sqrt{\frac{(W/L)_{CM}}{(W/L)_{IN}}} \tag{24}$$

where α represents constant terms in (23). An example of the temperature characteristic of the compensated offset voltage realized with the OTA from *Fig. 10* is shown in *Fig. 11*.

Similarly to the method described in *Section IV.B*, the presence of R_{OS} can influence the temperature characteristics of the current mirror employed for trimming. As a result, the temperature compensation described by (23) and (24) may be less efficient for large R_{OS}, resulting in increased temperature drift. To preserve the temperature characteristic $g_{m(CM)}(T)$, using a small value of $R_{OS} << 1/g_{m(CM)}$ is preferred. However, this may result in high trimming current, $I_{DAC(L,R)}$. Similarly to the method described in *Section IV. B,* the approach described in *section IX* may improve the temperature drift for larger values of R_{OS}.

VI. Differential Pair Symmetry Adjustment

Similarly to the adjustment of the current mirror symmetry described in previous *section V. A.*, the channel width ratio of the differential pair transistors can also be adjusted. This is illustrated by using arrows in *Fig. 2*, and a silicon implementation example is presented in [14]. Unlike the previous case from *section V. A*, the offset introduced between I_1 and I_2 is not related to the channel width ratio of $M_{1,2}$, but results from the difference between respective transconductances g_{m1} and g_{m2}.

An offset current $I_{AUX} = I_1 - I_2$ originating from $g_{m1} - g_{m2}$ can be calculated using the small signal transistor model. For $\Delta V_{IN} = 0$, the offset current I_{AUX} is a linear function of the bias current I_0, and $g_{m1,2}$, and can be expressed as follows:

$$I_{AUX} = I_1 - I_2 = I_0\frac{g_{m1} - g_{m2}}{g_{m1} + g_{m2}} \tag{25}$$

Similarly to (13), I_{AUX} can be referred to the input terminals *via* the value of the differential pair transconductance $g_{m(IN)}$. When $g_{m1} \neq g_{m2}$, the value of $g_{m(IN)}$ can be expressed as:

$$g_{m(IN)} = \frac{I_{AUX}}{\Delta V_{IN}} = 2\frac{g_{m1}g_{m2}}{g_{m1} + g_{m2}} \tag{26}$$

The offset voltage introduced to the input terminals results from (25) and (26) as:

$$V_{OS(AUX)} = \frac{I_{AUX}}{g_{m(IN)}} = \frac{I_0}{2}\frac{g_{m2} - g_{m1}}{g_{m1}g_{m2}} \tag{27}$$

Here, an inconvenient $\approx 1/g_{m(IN)}$ dependency can be observed, as already seen in the constant current injection and active load current-mirror ratio trimming methods. As a consequence, the compensated V_{OS} exhibits a non-negligible temperature drift comparable to the characteristis shown in *Fig. 5*. The non-negligible residualt temperature drift is also demonstrated in [14].

VII. Tail Offset Voltage Generators

Adding resistive voltage generators between the source terminals of the input differential pair is a commonly employed method to compensate the input offset voltage [15]. It can be shown that voltage sources $V_{AUX(L,R)}$ in *Fig. 2* are referred to the OTA inputs with nearly unitary gain. As a result, providing thermally stable voltages $V_{AUX(L,R)}$ provides high attenuation of the temperature stable term in (10).

Similarly to the structure of a degenerated differential pair utilized to enhance the linearity of operational amplifiers, the source resistance reduces the value of $g_{m(IN)}$ [1]. As a consequence, the OTA gain and bandwidth are also reduced.

A. Programmable tail resistance method

Tail offset voltage trimming is usually implemented by a programmable series resistive network shown in *Fig. 12,* or by a laser adjustable resistance [15]. The resistive network shown in *Fig. 12* is composed of small elements R_{OS} and is biased by the current source I_0. Current mirror voltage V_{CM} is connected to one or more junctions of adjacent resistors *via* analog switches SW_x. The offset trimming is typically driven by a binary, or a bi-directional thermometric search algorithm represented by a trimming sequences example in *Fig. 13*.

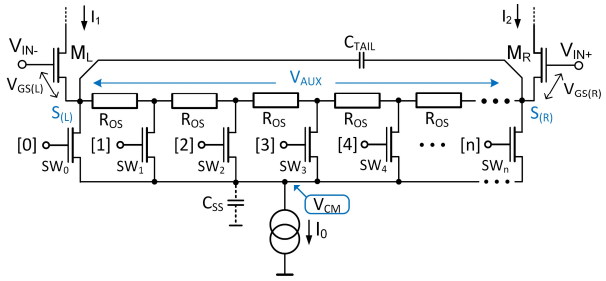

Fig. 12. Tail offset voltage generation implemented by series resistances segments R_{OS} and analog multiplexer SW_x [15]. Capacitor C_{TAIL} can be added to increase degenerated $g_{m(IN)}$ at higher frequencies .

The difference between both methods is that for the binary algorithm, both $V_{AUX(L,R)}$ are simultaneously added to the terminals $S_{(L,R)}$, whereas for bi-directional thermometric search, only one of $V_{AUX(L)}$ or $V_{AUX(R)}$ is added between V_{CM} and one of the source terminal $S_{(L,R)}$, depending on V_{OS} polarity. While the resistance between $S_{(L)}$ and $S_{(R)}$ remains independent on the trimming code for binary search, $g_{m(IN)}$ is lower, but constant over the trimming range. Trimming by bi-directional thermometric search algorithm improves the transconductance for small offset correction, but decreases $g_{m(IN)}$ for larger corrections. Additionally, the bi-directional thermometric search improves the common-mode range for moderate offset correction by reducing the drop between $S_{(L,R)}$ and V_{CM}. For extreme cases where only SW_0 or SW_n are conducting, both methods yield the same results (see *Fig. 13*).

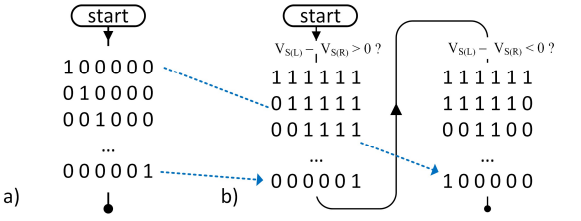

Fig. 13. Comparison of the trimming sequences of *a*) binary search and *b*) bi-directional thermometric search algorithm. "1" and "0", correspond to the conducting and non-conducting switches SWx.

In the binary search algorithm, only one of SW_x is on, and the trimming process sweeps from $x = 0$ to $x = n$. The outcome of the trimming are voltages $V_{AUX(L)} = (S_{(L)} - V_{CM})$ and $V_{AUX(R)} = (S_{(R)} - V_{CM})$ given as $\frac{1}{2}I_0 \cdot R_{L,R}$. Here, R_L, R_R are resistances between node V_{CM} and respective nodes $S_{(L)}$ or $S_{(R)}$. The offset $V_{AUX} = V_{S(L)} - V_{S(R)}$ can be approximated by assuming the equilibrium condition as $I_1 = I_2$:

$$V_{AUX} = \frac{I_0}{2} R_{OS} \{x - (n-x)\} = \frac{I_0}{2} R_{OS} \{2x - n\} \quad (28)$$

Here, x is the number of segments between V_{CM} and $S_{(L)}$, and $(n - x)$ is the number of segments between V_{CM} and $S_{(R)}$.

A bi-directional thermometric search algorithm generates V_{AUX} only on the source of one transistor, depending on the polarity of V_{OS}. This signifies that either $S_{(L)}$ or $S_{(R)}$ is connected to V_{CM}, while the other source voltage is increased by V_{AUX}. Offset $V_{AUX} = V_{S(L)} - V_{S(R)}$ can be calculated for both polarities of the compensation as:

$$V_{AUX(+)} = \frac{I_0}{2} R_{OS} x \quad or \quad V_{AUX(-)} = -\frac{I_0}{2} R_{OS} (n-x) \quad (29)$$

Due to the usually small bias current I_0 and required LSB trimming step, R_{OS} value may be very small, often in the order of ohms. Implementing such temperature stable resistors in CMOS can be difficult. Moreover, a large number of switches SW_x introduces significant capacitance C_{ss}, which leads to a degradation of the power-supply rejection ratio (PSRR).

B. $V_{OS(L,R)}$ constant resistance tail offset voltage generator

Significant simplification and improvement of some parameters can be achieved by realization shown in *Fig. 14* containing *a*) single or *b*) two resistor R_{OS}, both of more convenient value when compared to R_{OS} elements from *Fig. 12*. In configuration *a*), OTA bias current I_0 is split into two current sources $\frac{1}{2} I_0$, and two programmable currents $I_{AUX(L,R)}$ are added to the source terminals $S_{(L)}$, $S_{(R)}$ of the input differential pair. Compared to that, solution *b*) maintains both programmable currents $I_{AUX(L,R)}$ tied to the source terminals $S_{(L)}$, $S_{(R)}$ but contains single bias current I_0.

Current sources I_{AUX} can be implemented as bipolar, providing positive and/or negative current to one or both nodes $S_{(L)}$ and $S_{(R)}$, or more convenient as unipolar, where $I_{AUX(L)}$ or $I_{AUX(R)}$ provides a single polarity compensating current to one of $S_{(L)}$ or $S_{(R)}$ terminals. In the latter case shown in both *Fig. 14 a)* and *b)*, only one of the left or right DAC is used to compensate for the respective polarity of V_{OS}. It has to be noted that unipolar current sources $I_{AUX(L,R)}$ increase the differential pair bias current by $\frac{1}{2} I_{AUX}$. Therefore, for $\Delta V_{OS} \approx 0$, I_1 and I_2 are ideally equals to $I_0/2 + I_{AUX}/2$ instead of $I_0/2$.

For unipolar current sources $I_{AUX(L,R)}$, voltage $V_{AUX} = V_{S(R)} - V_{S(L)}$ can be obtained from the simplified equilibrium condition $I_1 = I_2$ as:

$$V_{AUX} = \pm \frac{1}{2} I_{AUX} R_{OS} \quad (30)$$

Besides the possibility of the temperature drift improvement that will be described in the upcoming *section IX*, the solution from *Fig. 14 a*, *b*) has the advantage of very low C_{SS} compared to the solution from *section VII. A*, allowing to improve the CMRR. It also allows for the use of R_{OS} with a more practical value, which in turn enables the scaling of the LSB step of I_{AUX}. Implementation from *Fig. 14 a*, *b*) also provides constant transconductance $g_{m(IN)}$ for the entire offset trimming range.

Comparing the implementations from *Fig. 14 a*) and *b*), the configuration with split bias current sources $\frac{1}{2} I_0$ improves the common mode voltage range. This is due to the fact, that only $\approx I_{AUX}/2$ flows through R_{OS} in the equilibrium. However, obtaining efficient voltage offset compensation necessitates precise matching between the left and right current sources $\frac{1}{2} I_0$. Any offset between these sources, especially in terms of temperature drift, can deteriorate the overall temperature stability of the solution from *Fig. 14 a*). If the common mode voltage headroom is sufficient, a solution with a single current source I_0 depicted in *Fig. 14 b*) is preferred.

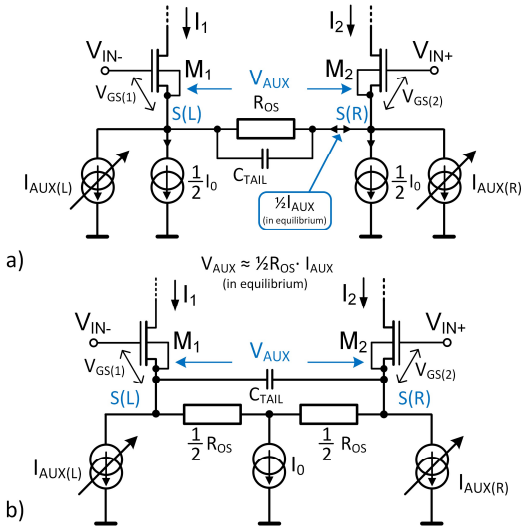

Fig. 14. Implementation of the constant resistance tail offset voltage generator. The OTA bias current I_0 is *a*) split into two $I_0/2$ current sources which improves the dynamic range, or *b*) is connected to spit R_{OS}, reducing additional offset originating from the mismatch of $\frac{1}{2} I_0$ current sources from *Fig. a*). Capacitor C_{TAIL} can be added to improve $g_{m(IN)}$ at higher frequencies.

An example of the performances provided with the PMOS differential pair implemented according to *Fig. 14 b*) is shown in *Fig.15*. The simulation was performed using a folded cascode OTA, and provides similar performance compared to the results presented in *sections IV.B* and *V.B*.

Depending on the process parameters and on the value of R_{OS}, this method can yield an improvement of dV_{OS}/dT, attributed to the improved matching of $\sqrt{\mu_n/\mu_p}$. However, this improvement is not always achieved, and R_{OS} may also result in the degradation of the temperature drift. In this case, a small value of $R_{OS} << 1/g_{m(A,B)}$ may be required to preserve original temperature characteristic of $g_{m(IN)}(T)$. However, using a low R_{OS} value implies an increase in the trimming current $I_{AUX(L,R)}$. A method for reducing this trimming current is presented in *section IX*.

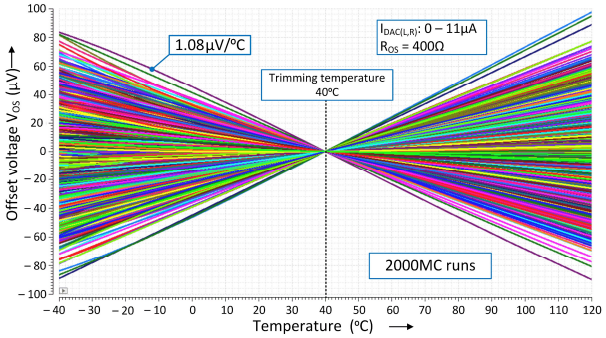

Fig.15. Example of the characteristic obtained with the single resistance tail offset voltage generator, variant from *Fig. 14. b*).

VIII. Series Input-Referred Voltage Generator

In specific cases where the output resistance of the voltage source is relatively small, offset voltage V_{AUX} can be generated directly between one or both gates of the input differential pair, and the voltage source terminal. This is schematically shown in *Fig.16*.

In this figure, the programmable current source $I_{AUX(L,R)}$ injects current into the shunt resistance R_{OS} which in turn generates a voltage drop V_{AUX} between the gate and the voltage source. Considering the temperature stable resistance

R_{OS}, this trimming method provides reliable compensation for the temperature-constant terms in (10), comparable to the methods described in *sections IV. B, V.B and VIII. A,B.*

The requirements of the voltage source low output resistance limit the application scale to, for example, voltage sources realized by an voltage feedback operational amplifier, or to applications in power electronics, where a small offset current does not alter the measured value.

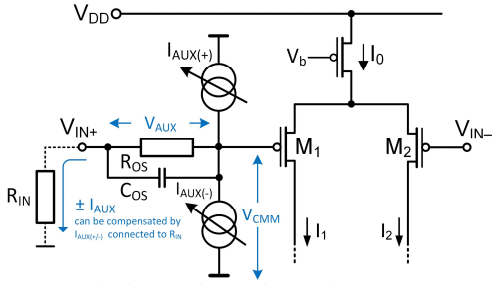

Fig.16. Compensation by gate shunt resistor and current source $I_{AUX(\pm)}$.

IX. Matching Improvements of the NMOS and PMOS Temperature Characteristics

Both *Eq*. (10) and the description in *Section III.B* address the temperature-dependent term related to the gain between $\Delta V_{TH(CMn)}$ and ΔV_{IN}. Although the electron and hole mobility μ_n and μ_p results from different scattering mechanisms, their temperature dependencies tend to be similar for a given process. However, in certain cases, mutual ratio of the transconductances can exhibit a noticeable temperature drift. For instance, this may occur when different types of devices are used within the OTA, when the differential pair operates in the subthreshold region where the transconductance differs from (3), or when the resulting transconductance is affected by a high channel length modulation effect. In such scenarios, the last term in (10) can introduce significant temperature instability resulting in a higher voltage drift of the compensated and uncompensated V_{OS}.

In certain cases, temperature stability of the transconductance ratio $g_{m(CMn)}/g_{m(IN)}$, can be improved by selectively applying temperature transconductance damping to either the PMOS or NMOS transistors in the OTA. The effectiveness of the improvement depends on the process parameters, but also on the OTA DC operating point. Incorporation of the temperature damping can improve resulting trimming performance, but it can also effectively reduce the temperature drift exhibited by the uncompensated OTA. This feature proves to be particularly advantageous for systems where the offset of the signal processing chain is trimmed externally, *i.e.* by the reference voltage source.

The temperature transconductance damping relies on the adjustment achieved by an additional element with distinct temperature characteristics compared to the MOS transistor. This element can be for instance a temperature-stable resistor R_{OS} connected to the source of a MOS transistor. As a consequence, the resulting transconductance becomes proportionally dependent on the temperature characteristic of both elements: the MOS transistor and the resistor. As an example, the differential pairs shown in *Fig. 14* contain the source resistance R_{OS} that modifies the temperature characteristic of the $g_{m(IN)}(T)$. Modified (degenerated) transconductance of the differential pair resulting from the presence of R_{OS} can be described by following equation:

$$g_{m(IN)}(T) = \frac{g_{m1,2}(T)}{g_{m1,2}(T)R_{OS}+1} \tag{31}$$

where $g_{m1,2}$ refers to $M_{1,2}$. Similarly, temperature behavior $g_{m(CM)}(T)$ of the active load current mirror can also be adjusted by an additional serial source resistance.

The adjustment of $g_{m(CMn)}/g_{m(IN)}$ temperature stability, achieved *via* temperature transconductance damping, is demonstrated in *Fig. 17*. This figure shows a comparison between an NMOS transistor in saturation without series resistance and a PMOS transistor operating in the subthreshold regime with variable source series resistance R_P. It can be observed that the temperature slope of the $g_{m(N)}/g_{m(P)}$ term exhibits an increasing tendency as the value of R_P increases. When R_P = 4kΩ, temperature compensation of $g_{m(N)}/g_{m(P)}$ is achieved, resulting in $\Delta V_{TH(CM)}$ in (10) being referred to the OTA input terminal with a temperature-constant gain. This is obtained at the cost of an acceptable degradation of g_{mP} for R_P = 0 → 4kΩ by –18% at 27°C.

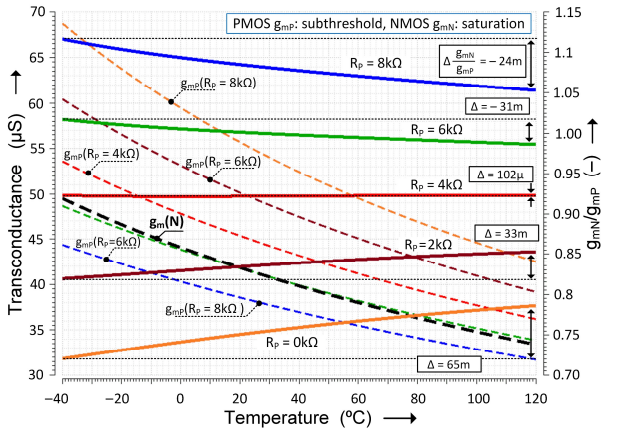

Fig. 17. *a*) Transconductances of PMOS transistor with various source resistance R_P, and NMOS transconductance g_{mN}, *b*) g_{mN}/g_{mP} ratio for various R_P, corresponding to the gain $\Delta V_{TH(CM)}/\Delta V_{IN}$. Simulation parameters: I_0 = 2.5µA (NMOS and PMOS), W/L_N = 10µm/2µm, W/L_P = 200µm/1µm.

A. Improved temperature compensated current injection.

In the description provided in *section IV.B*, a low value of R_{OS} was required to maintain desired temperature characteristic of $I_{OS}(T)$. This, in turn, leads to a high range of the trimming current values $I_{DAC(L,R)}$.

Fig. 18. shows a Miller OTA that is configured for trimming through the temperature-compensated current injection method. In order to minimize the trimming current from $I_{DAC(L,R)}$, a source resistance R_{OS} = 5kΩ of $M_{R,A,B}$, was utilized (*Fig. 7*). However, as mentioned earlier, this value alters the temperature characteristic of $I_{OS}(T)$.

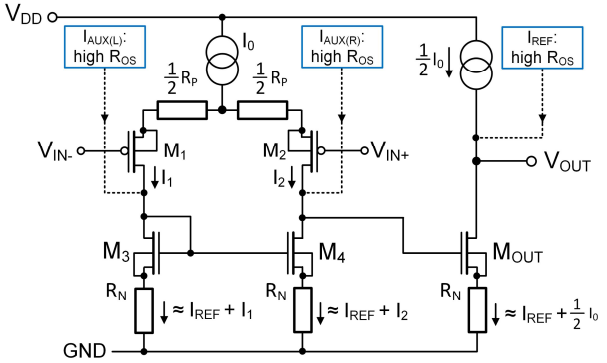

Fig. 18. PMOS Miller OTA allowing temperature transconductance damping of both differential pair and active load. Temperature characteristics of $g_{m(IN)}$ and $g_{m(CM)}$ are modified by R_P, R_N, respectively, allowing to align with dumped temperature characteristic of $I_{OS}(T)$ current source.

In order to align the modified characteristic of I_{OS}(T) with the temperature characteristic of the differential pair and active load, resistances R_P = 2kΩ and R_N = 2kΩ were employed in the OTA from *Fig. 18*. It is worth noting that reducing the transconductance of the differential pair increases the range of V_{OS} (10). However, this degradation is compensated through the trimming process. *Fig. 19* shows an example of simulated performances based on the temperature transconductance damping with similar results as shown in the original characteristic from *Fig. 8*. However, the maximal magnitude of $I_{DAC(L,R)}$ was reduced from 17µA to 2µA.

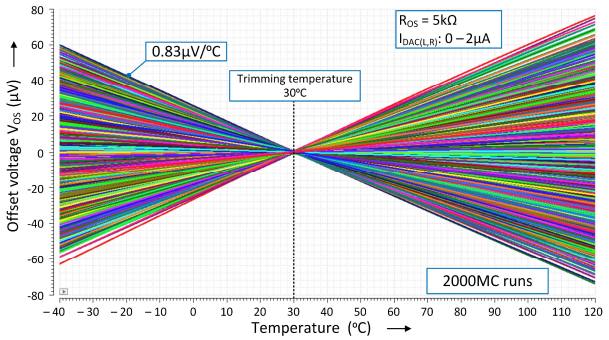

Fig.19. Example of the performances obtained with *Fig. 18* OTA and temperature compensated current injection from *Fig. 7* with increased R_{OS}. OTA was implemented with W/$L_{1,2}$ = 160µm/1µm, W/$L_{3,4,OUT}$ = 20µm/2µm, I_0 = 30µA, and I_{REF} = 5µA.

B. Improving temperature drift of the untrimmed OTA.

In the case where the offset trimming is conducted at the system level, *i.e.* outside the OTA, the primary focus may be to reduce the temperature drift of the uncompensated V_{OS}. Similarly as in the latter case, this can be achieved by adjusting the temperature characteristics of $g_{m(CM)}/g_{m(IN)}$. This becomes particularly relevant *e.g.* when the differential pair operates in the subthreshold region, where the temperature behavior of $g_{m(IN)}$ differs from $g_{m(CM)}$ given by (3).

The improvement of the temperature drift is demonstrated for this particular case by using the Miller OTA from *Fig. 18,* implemented without trimming circuit and with identical transistor sizes and bias current as the example from *Fig. 17.* In *Fig. 17*, temperature stability is achieved for single transistors with R_P = 4kΩ and R_N = 0. By incorporating these values into the OTA from *Fig. 18*, the temperature drift of V_{OS} can be reduced by more than 50%. This improvement is demonstrated in *Fig. 20*, comparing the statistical distribution of the temperature drift averaged over –40°C to +120°C temperature range.

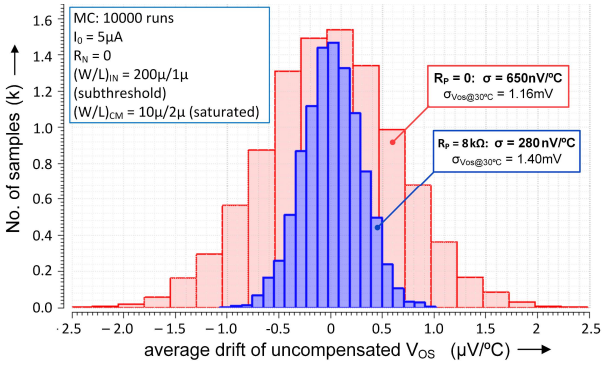

Fig. 20. Comparison of the temperature drift of the uncompensated OTA from *Fig. 18*. Improvement is achieved by adding 2 × ½R_P = 4kΩ, corresponding to the results presented in *Fig. 17* inset.

Tab. 1. Comparison of the methods presented in this paper. * - require either accurate R_{OS} or R_{OS} identical to the resistance used in bandgap to generate I_{AUX} or I_{DAC}. This allows to ensure temperature stability of V_{AUX}.

chapter	complexity	dV_{OS}/dT	Notes:
IV. A	very low	high	High resolution if I_{AUX}
IV. B	low	low	*
V.A	moderate	high	Complex layout
V.B	very low	low	*
VI.A	high	high	Complex layout
VII. A	moderate	low	*
VII.B	very low	very low	*
VIII.A	very low	low	*
IX.	low	very low	Require high model accuracy

X. CONCLUSION

This paper presents methods of the OTA input offset voltage trimming, that can be used in a large majority of CMOS operational amplifiers and comparators. It focuses on the optimization of the temperature drift of the compensated and uncompensated input-referred offset voltage. A brief overview of the parameters related to the methods presented in this paper is summarized in *Tab. 1*. New methods presented in *sections IV. B, V.B VIII. B, VIII and IX* allow parameter improvement and simplification of the trimming process and offer state-of-the-art performances of the single temperature offset trimming. The main target of this study is to facilitate the trimming implementation, allowing efficient offset compensation during the electrical wafer test or during the circuit operation.

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