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***Abstract*—This paper presents an analytical analysis to estimate the optimal slew rate (SR) and gain bandwidth (GBW) requirements of operational transconductance amplifiers (OTA) in discrete-time sigma-delta modulators (DT-$\Sigma\Delta$M). The proposed g_m/I_d approach takes into account the bias condition of the transistor allowing the designer to easily obtain transistor-level design specifications from system-level requirements. The accuracy of the presented study is verified by post-layout simulations of a DT-$\Sigma\Delta$M. The post-layout simulation results are in agreement with system-level predictions even considering process, voltage, and temperature variations.**

***Index Terms*—Settling error, switched-capacitor integrators, modeling, slew rate, gain-bandwidth product, $\Sigma\Delta$-ADC, g_m/I_d.**

I. Introduction

Sigma delta modulators ($\Sigma\Delta$Ms) are the primary solution when targeting a good trade-off between accuracy, speed, and power consumption in analog-to-digital converters. Compared to continuous-time modulators, discrete time (DT) modulators are less sensitive to jitter noise, scales automatically with the sampling frequency, and enable high coefficient stability [1]. However, integrator defective settling is one of the main limiting factors in DT implementations. This error is mainly due to the amplifier's finite DC gain (A), finite gain-bandwidth product (GBW), and limited slew rate (SR).

The finite DC gain is modeled as a magnitude and a phase error on the integrator's ideal transfer function, whereas the finite GBW and limited SR may be interpreted as a non-linear gain error depending on the integrator's input voltage. For this reason, both conditions are much more complex to model as reported in [2]. Solutions such as [3] and [4] require transistor-level parameters, assuming an already existing OTA design. An alternative method is presented in [2] and [5], where a simple model of the settling behavior is achieved, but it does not consider the charge redistribution effect. A design-oriented model including the charge redistribution effect is proposed in [6], but the time constant was expressed as $\tau_{int} = 1/GBW$(rad/s). However, most published models lack an analytical approach to estimate the optimal SR and GBW for a required modulator resolution [2], [5], [6].

This work presents a g_m over I_d based methodology providing a close relationship between the modulator resolution and amplifier speed constraints as GBW and SR. Proposal keeps the high-level advantage of the model developed in [2], [6] while considering power consumption [7], gain [8], speed, and noise [9] of the amplifier. Section II develops a system-level analysis and modeling of $\Sigma\Delta$Ms. Section III proposes a g_m/I_d based methodology for optimum amplifier specifications. Post-layout results are depicted in Sec. IV.

II. $\Sigma\Delta$Ms' Integrator Analysis and Modeling

A. Settling behavior phases of the output voltage

Figure 1(a) illustrates a single-ended parasitic-insensitive integrator with a capacitance ratio $a = C_s/C_i$. During the integrating phase ($\Phi_2 \equiv T_s/2 < t < T_s$), charge is transferred from C_s to C_i. Thus, the temporal evolution of the output voltage can be divided as follows: at the starting time, a potential drop (V_{drop}) occurs due to the charge redistribution effect, increasing the integration step voltage as represented by the blue line in Fig. 1(b). Then, the OTA starts charging C_i considering the equivalent output voltage ($V_{tot} = V_{out} + V_{drop}$), the equivalent settling time τ_{int}, and the SR. When $V_{tot} \leq SR \cdot \tau_{int}$, the amplifier works in its linear region, and it is not limited in current. The evolution of output voltage assuming a single-pole OTA and no charge stored in C_i is defined by [2],

$$v_{out}(t) = V_{out} - V_{tot} \cdot e^{-\frac{t-T_s}{\tau_{int}}}. \tag{1}$$

When $V_{tot} > SR \cdot \tau_{int}$, the OTA is firstly in slewing and the temporal evolution of the output voltage $(v_{out}\,(t \leq t_{slew})$ is linear with a slop of SR as illustrated by the red line in Fig. 1(b). After the slewing phase $(t_{slew} \leq t)$, the output voltage follows an exponential evolution with a settling time constant $\tau_{int} \propto 1/GBW$ as illustrated by the green line in Fig.1(b). Under this condition, the following equations hold [2]:

$$v_{out}(t) = -V_{drop} + SR \cdot \left(t - \frac{T_s}{2}\right), \tag{2}$$

for $\frac{T_s}{2} < t \leq t_{slew}$, and

$$v_{out}(t) = V_{out} - \left(V_{tot} - SR \cdot \left(t_{slew} - \frac{T_s}{2}\right)\right) \cdot e^{-\frac{t-t_{slew}}{\tau_{int}}}, \tag{3}$$

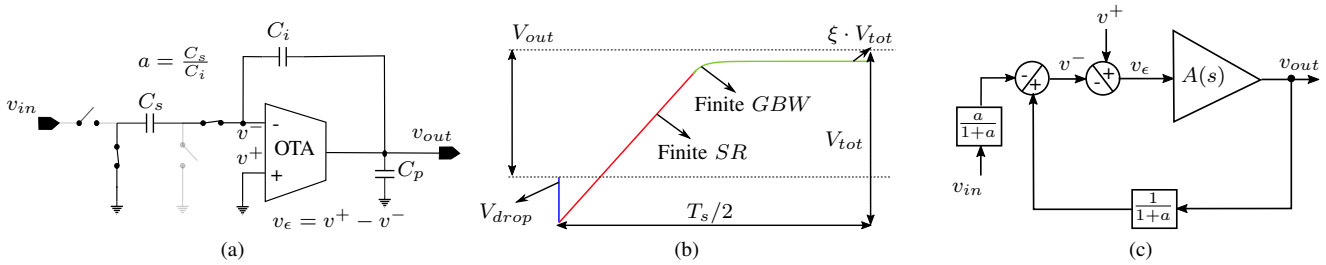


Figure 1. Illustration of (a) the parasitic-insensitive-integrator during the integrating phase Φ_2, (b) its output response, and (c) its equivalent closed loop.

for $t_{slew} < t \leq T_s$. Here, $V_{drop} \approx \frac{V_{out}}{a+r(1+a)}$, $r = C_p/C_i < 1$; α is a relationship between sampling period (T_s) and slewing duration (t_{slew}) as $t_{slew} = \frac{(1+\alpha)}{2}T_s$. Depending on α and the input voltage, the integrator response is completely linear as (1), completely slewing as (2), or partially linear as (3) and partially slewing as (2). Thus, a trade-off between power consumption and accuracy can be investigated. In fact, case (1) with exponential attenuation leads the output settling error to be very low. Then, $\alpha = 0$ and the SR requirement with respect to the GBW could be very high according to [6]. Although this is a common design solution, it leads to a high power consumption. Under a low SR operation, $\alpha > 1$ and the output is completely slewing in (2), leading to a very large settling error. Therefore, working in the partial slewing operation ($0 < \alpha < 1$) can provide a good trade-off between accuracy and power consumption. It is worth noting that if the settling error during the integration phase does not affect the modulator's performance, the same applies to the settling error of the sampling phase [6]. The following section will conduct a detailed analysis to find the optimal value for α. However, the expression of τ_{int} should be first established.

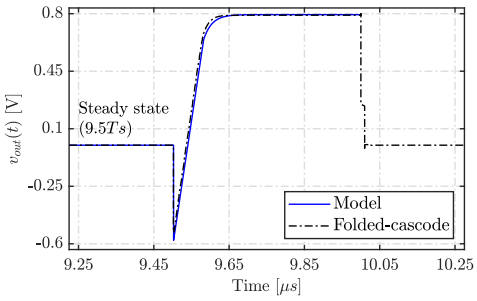


Figure 2. Integrator response using typical folded-cascode OTA (black), and model (blue), considering $GBW \approx 13$ MHz, $SR \approx 11$ MV/s, $T_s = 1\mu s$, $a = 0.8$, $r = 0.3$, $V_{in} = 1$ V, and $A = 60$ dB.

B. Integrator equivalent closed loop gain and time constant

The expressions of the integrator gain (A_{int}) and time constant (τ_{int}) can be determined from the integrator closed-loop transfer function $H_{int}(s)$ illustrated in Fig. 1(c). Assuming a single-pole amplifier, i.e. $A(s) = \frac{A}{1+s\cdot\tau}$, $H_{int}(s)$ can be written as,

$$H_{int}(s) = \frac{A_{int}}{1 + s \cdot \tau_{int}}, \begin{cases} A_{int} = \frac{a \cdot A}{1+a+A}, \\ \tau_{int} = \frac{1/GBW}{1+\frac{1}{1+a}A}. \end{cases} \quad (4)$$

Clearly, τ_{int} is not a simple function with GBW as in [2], [6], but it also exhibits a dependency on a. Figure 2 compares the time response of the integrator shown in Fig. 1(a) using the model proposed in Fig. 1 in blue continuous line and a transistor-level folded-cascode OTA in black dot-dashed line. It can be indicated that the settling behavior of the presented model follows precisely the electrical simulations. The only difference is the smoothed charge redistribution (lower V_{drop}) in the real case, due to the switches finite on resistance. Thus, the model accurate estimates the amplifier specifications.

III. Proposed g_m/I_d Based Methodology for Optimum Specifications

This paper proposes a method to estimate the optimal OTA speed specifications (SR and GBW) to fulfill a $\Sigma\Delta$Ms requirement. Proposal considers a g_m/I_d based methodology in extension of power consumption [7], noise [9], and non-linearity [10]. System-level considerations are as follows. **i.** Both 2^{nd} and 3^{rd} order single-bit feedforward $\Sigma\Delta$Ms are used to validate the analytical analysis. **ii.** Only the imperfections of the first integrator are considered since distortions, and noises of the remaining blocks are attenuated by the feedback-loop and noise-shaping capabilities of the modulator. **iii.** The output saturation level of the OTA is not taken into account in the model. **iv.** The DC gain of the OTA is assumed to be sufficiently high ($A \gg 1$) and its effect is neglected. Therefore, the normalized error at the end of the integrating phase denoted ξ in Fig. 1(b) is solely due to the limited SR and finite GBW, i.e. $\xi = \xi_{GBW,SR}$. Under this condition, A_{int} is equal to a, and τ_{int} is approximately $(1+a)/GBW$. **v.** The proposed method aims to analyze how the maximum settling error ($\xi^{max}_{GBW,SR}$ at V^{max}_{tot}) affects the modulator resolution, rather than studying its time-depended value. These assumptions simplify the analysis, while preserving accuracy.

A. Trade-offs Between α, g_m/I_d, and $\xi_{GBW,SR}$

To find the best combination of GBW and SR (or α) of the OTA for a required $\Sigma\Delta$M resolution, one should determine analytical equations relating them to g_m/I_d . A first relationship between GBW, SR, and α can be obtained by

imposing a maximum output error of ξ (i.e. $\xi^{max}_{GBW,SR}$) at the end of the integrating phase. From (3) at $t = T_s$, one may find

$$GBW \cdot T_s = 2\frac{1+a}{1-\alpha} \cdot ln\left(\frac{1/DR}{\xi^{max}_{GBW,SR}} \frac{1+a}{V_{ref} \cdot GBW/SR}\right), \quad (5)$$

where DR is the OTA dynamic range; V_{ref} is the modulator reference voltage. A second relationship between these parameters can be found by imposing the condition for the continuity of the derivatives of (2) and (3) in α,

$$\frac{SR \cdot T_s}{V_{ref}} = \frac{2}{\alpha} \cdot \left(\frac{V^{max}_{tot}}{V_{ref}} - \frac{1+a}{V_{ref} \cdot GBW/SR}\right). \quad (6)$$

Depending on the chosen OTA topology, relations between GBW, SR, and g_m/I_d can be established. In practice, the input differential pair's bias current (I_d) affects the GBW, while the output stage's driving current (I_s) determines the SR requirement. For example, a continuous-time design using folded cascode OTA it is recommended to maintain a current ratio $(\beta = I_d/I_s)$ between 2 and 3, which leads to the best speed and power consumption trade-off. While using switched capacitor circuits, a β between 1.1 and 1.2 is considered optimal, as higher values of β may cause significant asymmetrical slewing according to [11]. If the $GBW = g_m/C_{load}$ and the $SR = I_s/C_{load}$, then one may write

$$\frac{GBW}{SR/V_{ref}} = \frac{V_{ref}}{\beta} \cdot \frac{g_m}{I_d}. \quad (7)$$

In two stages OTA (Miller), the optimal operation occurs when $\beta \approx C_c/(C_c + C_{load}) < 1$ [12]. By dividing (5) and (6), and replacing (7) and $V^{max}_{tot} = \xi \cdot V_{tot}$, one may find an optimal function

$$f(\alpha) = \frac{\alpha}{1-\alpha} \cdot \frac{ln\left(\frac{\beta/DR}{V_{ref} \cdot g_m/I_d} \cdot \frac{1+a}{\xi^{max}_{GBW,SR}}\right)}{\frac{aV_{ref} \cdot g_m/I_d}{\beta}\left(\frac{1+r}{a+r(1+a)}\right) \cdot V^{max}_{in}/V_{ref} - 1}. \quad (8)$$

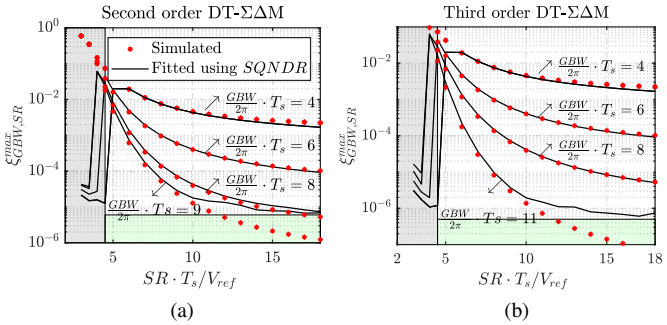


Figure 3. The $\xi^{max}_{GBW,SR}$ as a function of GBW and SR, of (a) the 2^{nd} order, and (b) the 3^{rd} order ΣΔM, considering $DR = 0.5$, $r = 0.3$ and $OSR = 256$.

The optimal value of α is thus obtained by solving $f(\alpha) = 1$ for fixed design specifications: a, V^{max}_{in}, r, g_m/I_d and $\xi^{max}_{GBW,SR}$. These specifications are defined as follows. **i.** The a is defined during system-level simulation for a given ΣΔM resolution and maximum DR. **ii.** The V^{max}_{in} is determined from the modulator reference voltage and DR according to the relationship $V^{max}_{in} = V_{ref}(1+DR)$ [13]. **iii.** C_s is defined for a given thermal noise level (negligible flicker noise), allowing estimation for $r = a \cdot C_p/C_s$. **iv.** $\xi^{max}_{GBW,SR}$ is defined for a required modulator resolution and will be discussed in Subsec. III-B. **iv.** The biasing condition of the input differential pair transistors g_m/I_d is given by a power consumption and reliability trade-off detailed in Subsec. III-C.

B. System-level Trade-Off: Settling Error and Modulator Resolution

The $\xi^{max}_{GBW,SR}$ can be determined directly from (1), (2), and (3). However, the effect of this error cannot be easily extended to the case of ΣΔMs. Thus, the optimal combination of GBW and SR is typically defined from system-level simulation [6]. Here, the proposal highlights a close relationship between the modulator-distorted resolution (signal-to-quantization noise and distortion ratio $SQNDR$) and $\xi_{GBW,SR}$, providing a direct estimation of GBW and SR from (8). For this purpose, a system-level model consisting of (1), (2), and (3), is implemented using MatLab/Simulink. A set of simulations are then run with various GBW and SR values. Figure 3 illustrates the simulated and the estimated values of $\xi^{max}_{GBW,SR}$ considering 2^{nd} and the 3^{rd} order ΣΔM. The simulated error, represented by the red points, is directly captured from the MatLab function during transient simulations.

The curve fit expression is derived from simulated $SQNDR$, with given specs of DR, GBW, and SR. This trade-off is estimated by

$$\xi^{max}_{GBW,SR} \approx \frac{\frac{GBW}{SR/V_{ref}} \cdot DR}{2^{\left\lfloor \frac{SQNDR - 1.7 + (0.5 - DR^2) \cdot V_{ref} \cdot GBW/SR}{6.02} \right\rfloor}}. \quad (9)$$

Figure 3 depicts in green and gray, both the regions where (9) are not valid. Invalid regions can be explained as follows. Considering a high-speed design, a higher enough GBW and SR lead to a negligible the settling error $\xi^{max}_{GBW,SR}$ (green region), and the modulator resolution is only limited by the quantification error $(SQNDR \approx SQNR)$. When the SR becomes very low $(\alpha > 1)$, the integrator is completely slewing, thereby (9) is no longer valid (gray region). Thus, the estimated error given by (9) can be inserted into (8) to determine α. Figure 4(a) shows analytical solutions obtained by solving (8) for a 2^{nd} order modulator targeting $SQNDR$ of 65, 75, 85, 95, and 105 dB. Each curve represents the best trade-off between speed (GBW and SR) and g_m/I_d from (7) in a range from 2 to 20. Reducing SR, the required GBW increases in a non-linear manner, resulting in an interesting design solution with both relatively low GBW and SR when

$$\frac{g_m}{I_d} \approx 2\pi \cdot \frac{\beta}{V_{ref}}. \quad (10)$$

This design solution in moderate inversion was also identified in [6], but only through system-level simulations. Finally,

the equivalent g_m/I_d solutions are used in the system-level simulation and the optimal $SQNDR$ is illustrated in Fig. 4(b).

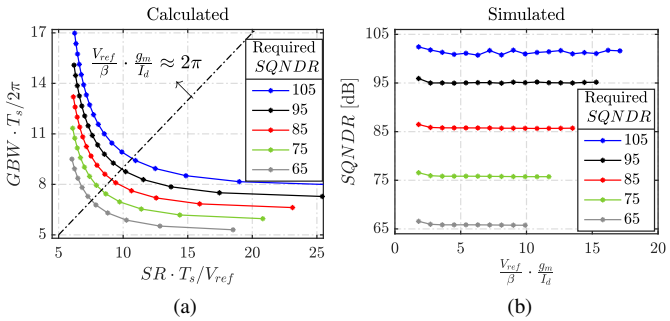


Figure 4. Calculated GBW and SR in 2^{nd} order modulator for (a) required $SQNDR$, and (b) the simulated $SQNDR$ as a function of g_m/I_d.

C. Transistor-Level Trade Off: g_m/I_d and Reliability

In the context of DT-ΣΔM, the integrator is increasingly seeking a trade-off between low power consumption, low noise, tiny footprint, and good reliability. While low power consumption is achieved under moderate inversion, one could choose o operate in such region for a good compromise between high g_m, high-voltage swing, low area, and low power consumption. However, such g_m/I_d solution could be very limiting in speed since $GBW \ll f_T$ and high enough transition frequency (f_T) is only found in strong inversion.

Noise considerations in OTA design have been drawn in [9]. In this case, the designer should choose the noise corner frequency (f_{CO}) of the differential pair small enough, so flicker noise is negligible and only thermal noise is considered. Negligible flicker noise ($f_{CO} \propto g_m/I_d$) is the hypothesis behind the design choice of C_s using the thermal noise approximation ($K \cdot T/C_s$). Reduced flicker noise often leads to a higher area trade-off. By preferring a strong inversion operation, the designer could expect a better circuit performance in terms of parameters variability, and to achieve higher current using small transistor size. However, this design choice comes at the cost of higher saturation voltage and reduced voltage swing. Strong inversion is also known to favor reliability degradation. In [8], the designer may choose a temperature-aware design limiting the transistor operation to trade reliability and power consumption. In [14], the designer may choose to limit transistor width to a W_{min} trade reliability and area under small geometry effects. Once the value of g_m/I_d is selected, the optimum GBW and SR is obtained for a desired $SQNDR$.

IV. Post-Layout Simulation Results

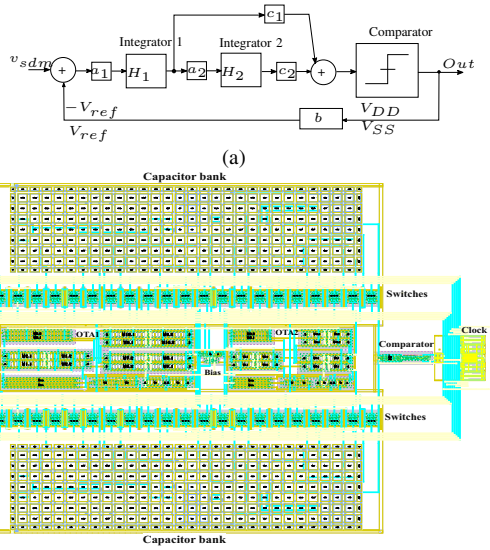
To illustrate the proposal, this paper implemented a 2^{nd} order ΣΔM depicted in Fig. 5(a). Transistor-level design is carried out using mixed signal 180 nm technology from XFAB. The modulator coefficients are $c_1 = c_2 = b = 1$, $a_1 = 0.8$, and $a_2 = 0.5$. Modulator uses a one-bit quantizer implemented with a dynamic comparator as [15], and integrator OTAs with folded cascode topology. The folded cascode OTA is temperature aware designed using the g_m/I_d approach of [8]. Thermal stability of SR is insured using a stable current reference in the input and output stages with $\beta \approx 1.1$. $GBW \propto g_m$ drift is minimized by biasing the differential pair in moderate inversion with $g_m/I_d \approx 9$ [8]. For $V_{ref} = V_{DD}/2 = 0.9$ V and 1 MHz sampling frequency the optimum GBW and SR combination for 100 dB $SQNDR$ target are 11 MHz and 7.7 MV/s respectively (see Fig. 4). The output stage transistors are sized so that the output impedance has a complementary temperature coefficient with g_m, and to obtain a minimum DC-gain $A > 3 \cdot OSR \approx 58$ dB so that its effect can be neglected for a 2^{nd} order modulator [6]. Figure 5(b) illustrates the ΣΔM layout having an area of 530 x 450 μm^2. Post-layout simulations (PLS) presented a total power consumption of 0.8 mW.

The noiseless power spectral density (PSD) of the modulator bit stream for 1 kHz input frequency and 1 MHz sampling frequency is shown in Fig. 6(a). Simulation results consider a Hann-windowed NFFT of $2 \cdot 10^5$ points. Ideal-OTA modeling is depicted in black line achieving an $SNR \approx 103$ dB. In blue line, PLS OTA simulation presented an $SNR \approx 99$ dB, which is in good agreement with the proposal predictions. Figure 6(b) illustrates the modulator output versus input response considering a sine wave of 1 Hz and a transient PLS. One can observe a negligible non-linearity below $0.5 \cdot LSB$ on the modulator typical response (black circles). Worst-case conditions are depicted in blue squares (1.98 V, -40 °C) and in red stars (1.62 V, 125 °). Typical and worst-case conditions are in agreement with system-level model in black line.

The first integrator OTA is post-layout simulated considering process-voltage-temperature (PVT) variations. Figure 7 illustrates a reliable gain and speed performance. Typical performance is given in black (μ, 1.8 V), and worst-case conditions are in blue (μ – 3σ, 1.62 V), and in red (μ + 3σ, 1.98 V). In Fig. 7(a), the amplifiers DC-gain exhibits high thermal stability with only 1 dB variation, for a temperature coefficient (TC) of 659 ppm/°C. In Fig. 7(b), the temperature-induced GBW variation from 27 to 125 °C is only 1.6 MHz, which represents a $TC = 646$ ppm/°C. The OTA used in the second integrator shows similar performance, and for lack of space is omitted.

V. Conclusions

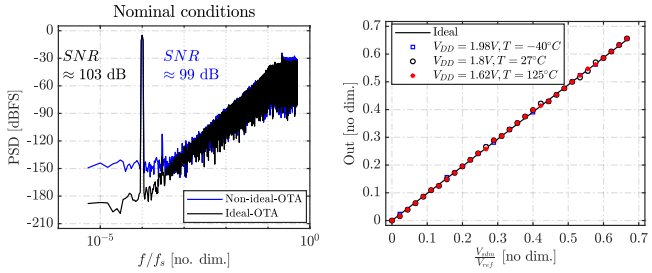
Integrator defective settling is one of the main limiting factors in ΣΔMs implementations. This paper presented a g_m/I_d based methodology to bridge the gap between the modulator resolution and amplifier speed constraints. The proposal demonstrated the existence of a sweet spot in moderate inversion, where $g_m/I_d \approx 9$. Thus, a reliable ΣΔM is optimal designed for an $SNR \approx 99$ dB and non-linearity below $0.5 \cdot LSB$ under PVT variations. PLS results of the folded-cascode OTA are in agreement with system-level modeling for $A \geq 58$ dB, $GBW \geq 13$ MHz, and a $TC \approx 650$ ppm/°C. Typical and worst-case PLS results are in agreement



(a)

(b)

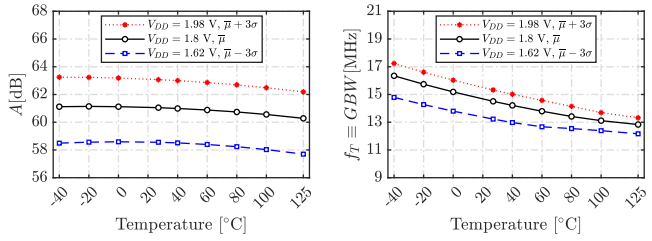
Figure 5. Illustration of Modulator (a) system-level architecture, and (b) layout using 180 nm XFAB technology for an area of 530 x 450 μm^2.



(a) (b)

Figure 6. Simulation results of the modulator in terms of (a) the PSD, and (b) output versus input transfer function.

with system-level modeling, which validates the proposed methodology.



(a) (b)

Figure 7. Simulation results of the OTA (a) DC-gain and (b) GBW, considering a temperature range from -40 °C to 125 °C, ±10% V_{DD}, and 51-points process and mismatch.

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