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Kai Ping Chang,[1] Haneen Abushammala,[2] Mamina Sahoo,[1] Alexandre Jaffre,[3,4] David Alamarguy,[3,4] Yu Jiang,[5] Mohamed Boutchich,[3,4,5,a)] and Chao-Sung Lai[1,6,7,a)]

AFFILIATIONS

[1]Department of Electronic Engineering, Chang Gung University, Guishan Dist., Taoyuan 33302, Taiwan
[2]IMPMC, Sorbonne Université, CNRS, MNHN, 4, place Jussieu, 75005 Paris, France
[3]Université Paris-Saclay, CentraleSupélec, CNRS, Laboratoire de Génie Electrique et Electronique de Paris, 91192 Gif-sur-Yvette, France
[4]Sorbonne Université, CNRS, Laboratoire de Génie Electrique et Electronique de Paris, 75252 Paris, France
[5]CINTRA UMI CNRS/NTU/THALES 3288, Research Techno Plaza, 50 Nanyang Drive, Border X Block, Level 6, Singapore 637553
[6]Department of Nephrology, Chang Gung Memorial Hospital, Linkou, Taoyuan 33305, Taiwan
[7]Department of Materials Engineering, Ming Chi University of Technology, New Taipei City 24301, Taiwan

[a)]**Authors to whom correspondence should be addressed:** mohamed.boutchich@sorbonne-universite.fr and cslai@mail.cgu.edu.tw

ABSTRACT

Graphene and 2D analogs such as transition metal dichalcogenides (TMDCs) have been widely investigated for their tuneable electronic properties. There is a large spectrum of applications of such 2D analogs; for example, non-volatile memory, which is a key building block for future low-power consumer electronics. In this work, we have investigated a vertical heterostructure composed of a chemical vapour-deposited molybdenum disulphide transistor channel coupled with silicon tunnel oxide (SiO_2) and hafnium oxide as a blocking barrier, with fluorographene (FGr) being used as the charge trapping medium. Owing to the larger trap density of FGr, the memory window is three times larger, and the data retention measurements at room temperature yield a 50% charge loss extrapolated to 10 years. The low barrier at the FGr/SiO_2 interface induces a steeper charge loss for holes. Nevertheless, the stack can sustain at least to 550 cycles without showing any sign of degradation. Although bandgap engineering is required to improve the data retention, particularly for the holes, the combination studied here is an encouraging route for 2D-based non-volatile memories.

I. INTRODUCTION

As the electronics industry has shifted from scaling to material-driven integration, devices have suffered from a wide range of instabilities, such as current leakage, power dissipation, and yield /reliability issues. Memory has also not been spared, and the flash memory concept has been challenged despite various concepts being under investigation.[1] Data storage devices are a cornerstone of current and future digital technologies; both academic and industrial researchers are working on a wide range of emerging concepts, but none has so far outperformed the data retention and endurance performance of flash memories,[2] particularly NAND flash memory, where the requirement for high-density traditional planar NAND is hindered by tunnel barrier reliability, cell-to-cell interference, and manufacturing cost.[3] 3D NAND flash is replacing the planar configuration below the 15 nm node, an architecture that not only reduces the scaling issues but also enhances the operation speed and reduces power consumption.[4] Triple-level cells (TLCs) are in production and are used in solid-state drives (SSDs) in place of single-level cells (SLCs) to minimize cost and increase the number of dies per wafer.[5] However, to fabricate 3D TLC NAND flash memory, the technology must minimize interference between neighboring cells, implying an increase in memory cell size.[6,7]

Proof of concepts of atomically thin two-dimensional (2D) memories such as graphene and transition metal dichalcogenides (TMDCs) has already been demonstrated.[8,9] Although there remain

questions regarding the reliability of the materials, researchers have judiciously exploited TMDC`s unique electronic, mechanical, and optical properties.[10–12] The ultrathin nature of the structure reduces the sidewall capacitance seen by the neighboring cell and, therefore, limits the crosstalk interference. Moreover, a better capacitive coupling through the stack could reduce the P/E voltage and improve the P/E operation speed. These materials can be integrated in a traditional planar architecture as well as in 3D, although technologically, this would be more challenging.[13]

Despite its lack of bandgap, graphene has been implemented as a transistor channel in a nanoribbon configuration, passivation layer, or even an electron storage medium for memories.[14–16] However, the low program/erase current ratio[17] hampers its integration in nonvolatile memory devices. In contrast to graphene, molybdenum disulphide (MoS_2), a TMDC, possesses a direct bandgap (1.8 eV) for monolayer and an indirect bandgap (~1.3 eV) for bulk materials[18] with high optical sensitivity and mechanical flexibility of up to 11% strain.[19] These properties have opened alternative routes for transistor channel and memory devices with mobilities as high as ~200 $cm^2/V\,s$ and an on/off ($> \sim 10^4$) for exfoliated MoS_2-based field-effect transistors (FETs)[20] having been observed. Moreover, there are several reports on ferroelectric memory or charge-trapping memory devices based on MoS_2.[21,22] However, most of the research has relied on an exfoliated material that does not completely translate the impact of processing onto the electronic properties of the end device. Interestingly, TMDC-based devices often exhibit hysteresis during DC sweep inherent to traps located or induced at the interfaces between a substrate and a channel and/or channel and tunnel dielectric.[23] This side effect, which is detrimental to most electronic devices, has been exploited for memory[24] by judiciously coupling a TMDC channel transistor with high-κ dielectric such as hafnium oxide (HfO_2) and HfAlO acting as the trapping medium (TM) for charges. These TMs were thought to enhance the data retention and program/erase speed of flash memory devices due to their relatively low leakage, reduced coupling crosstalk, and good scalability in addition to their larger conduction band offset relative to SiO_2.[25] However, their low charge trapping efficiency and poor data retention has hindered their development in robust charge-trapping memory devices. One study utilized graphene oxide (GO) as the TM,[26] but its lower thermal stability during device fabrication yielded poor performance.[27]

Fluorinated graphene (FGr) is one of the most stable graphene derivatives and could be a good candidate as a TM for memory devices. The conductivity of FGr is modulated by tuning the carbon-to-fluorine ratio (C/F), while maintaining good chemical and thermal stability.[28] Furthermore, the high electronegativity of FGr acts as an excellent passivation to a substrate and enables decoupling of the carrier transport at the interfaces.[29] Whereas most of the studies have been focused on fluorine-doped metal oxide for TM,[30,31] there have been a few reports showing the potential of FGr as a TM for charge storage applications.[32] FGr as a trapping medium offers several advantages over mainstream TM materials. The higher work function of FGr ~5.1 eV[33] permits to trap charges more deeply, improving data retention by reducing thermo-ionic emission over the tunnel barrier. This property can be tailored either by functionalization or by increasing the number of layers,[34] which will in addition, increase the density of states available for trapping. With respect to processing, multilayer graphene can be directly produced by CVD[35] and completely fluorinated by CF_4 plasma,[36] which is easy to process and compatible with semiconductor manufacturing processes. Finally, the ultrathin nature of the FGr translates into a better capacitive coupling and reduction in P/E voltages. Moreover, it could also reduce the sidewall capacitance, limiting the crosstalk to neighboring cells.

In this work, we synthesized MoS_2 on a SiO_2 substrate by CVD inside a quartz tube furnace using MoO_3 (molybdenum trioxide) and sulfur (S) powder. The growth conditions were optimized to form a continuous monolayer film of MoS_2 on the SiO_2 substrate, and the crystalline structure was characterized by Raman, photoluminescence (PL), and x-ray photoelectron (XPS) spectroscopies. We also studied the charge storage capabilities of $MoS_2/SiO_2/FGr/HfO_2$ heterostructures, including data retention and endurance. We show, despite charge loss mechanisms, that the devices with FGr exhibit a large symmetrical memory window within typical programming (P) and erase (E) voltages of flash memories, demonstrating the added value of such heterostructures.

II. EXPERIMENTAL SECTION

The $MoS_2/SiO_2/FGr/HfO_2$ devices, with FGr as the charge storage medium, were fabricated on 4-in. p^+-type (100) silicon wafers.

A. Materials growth and characterization

First, Si was cleaned using the standard Radio Corporation of America (RCA) cleaning procedures. Then, 300 nm silicon oxide (SiO_2) was grown by thermal oxidation to ensure a uniform thickness, which is critical for the P/E speed of the device. Subsequently, a monolayer (1 ML) of MoS_2 was grown over SiO_2 by CVD in a quartz tube furnace [Fig. 1(a)]. High-purity MoO_3 and S powder precursors were placed in two separate crucibles along the tube. The substrate of SiO_2/Si was faced up and placed closer to the MoO_3 crucible and then heated to 630 °C. The solid sulfur was placed at the upstream end until its temperature reached 210 °C. The entire process was conducted under Ar flow as the carrier gas to bring the sulfur vapor into the furnace for 30 min. This method allowed the growth of 1 ML MoS_2 films onto the 300 nm SiO_2. The film was characterized by both Raman and PL spectroscopy. The mappings, Fig. S1, were acquired over the same $20 \times 20\,\mu m^2$ monolayer MoS_2 sample by using an Alpha300 Witec system with a 532 nm laser, an integration time of 3 s and grating of 1800 g/mm area for both the Raman and PL (E^1_{2g} and A_{1g} modes) at 300 K and 84 K [Figs. 1(b) and 1(c)].

Figure 1(b) represents the Raman spectra for several random locations on the CVD MoS_2 sample. Spectra in black are the measurements at room temperature, whereas the ones in orange are for 84 K. It is clear that the spectra have a similar Raman separation of 18.5 cm^{-1} at room temperature and 19.7 cm^{-1} at 84 K. These separations indicate the presence of a monolayer over the sample.[37] Moreover, by decreasing the temperature to 84 K, both E^1_{2g} and A_{1g} follow a blue shift. Here, the frequency shift differs for the two modes; the A_{1g} mode exhibits a larger shift (2.5 cm^{-1}) than the E^1_{2g} mode (1.2 cm^{-1}) inherent to strain.[38]

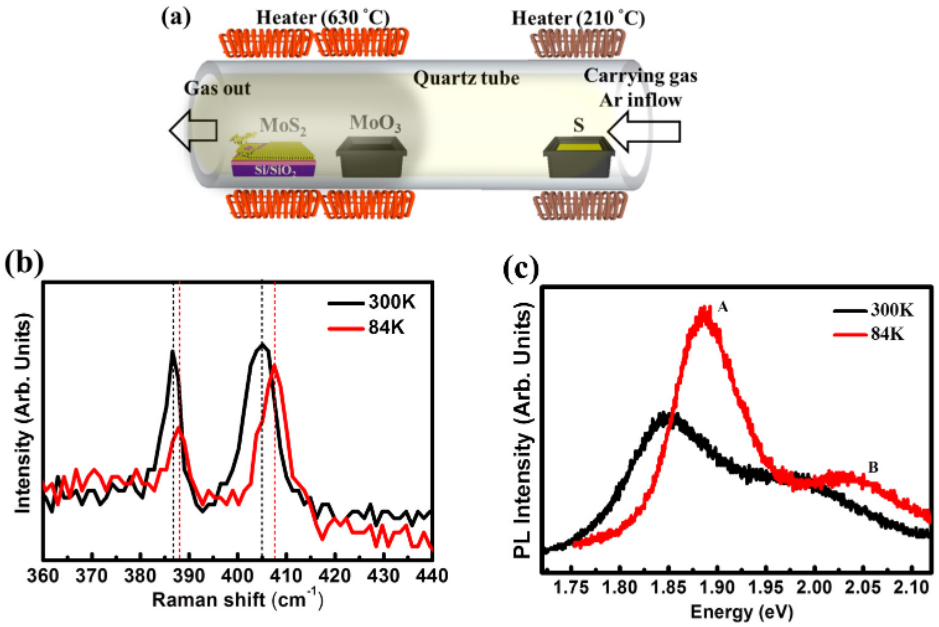

FIG. 1. (a) Schematic diagram of the MoS_2 furnace with MoO_3 and S precursor. (b) Raman spectra at 84 K (red) and 300 K (black) for the monolayer MoS_2 sample; (c) PL spectra at 84 K (red) and 300 K (black) indicating PL of a monolayer sample with a bandgap of 1.88 eV.

To verify the homogeneity of our large-scale monolayer, PL measurements were carried out over the same area. Figure 1(c) displays a typical PL spectrum extracted from the mapping (the mappings are provided in Figure S1 in the supplementary material). A homogeneous energy gap is observed at 84 K at the energy of 1.89 eV (peak A); at 300 K, the energy gap is 1.84 eV. The values of the position and the FWHM of the peaks A and B at 300 and 84 K are listed in the supplementary material Table S1. A characteristic spin–orbit splitting of 0.11 eV is also calculated at 300 K; this energy increases to 0.13 eV at 84 K, as listed in Table S2. Following Raman and PL experiments, we carried out x-ray photoelectron spectroscopy (XPS) to determine the stoichiometry of MoS_2 as well as the degree of oxidation. Figure 2 displays the high-resolution spectra of Mo and S elements deconvoluted. Figure 2(a) represents the deconvoluted Mo 3d spectrum. We observed the +4 oxidation state where the two peaks at 229.7 eV and 232.8 eV are assigned to $3d_{5/2}$ and $3d_{3/2}$ binding energies, respectively. Similarly, the +6 oxidation state comprises the 233 eV and 236.1 eV assigned to the $3d_{5/2}$ and $3d_{3/2}$, respectively. The Mo^{5+} state is also visible with a smaller contribution at energies of 232 eV and 235.1 eV. Regarding the S element, a −2 oxidation was observed, as shown in Fig. 2(b). These chemical states confirm the presence of MoS_2. The various energies observed are in good agreement with the previous values reported for MoS_2.[39,40]

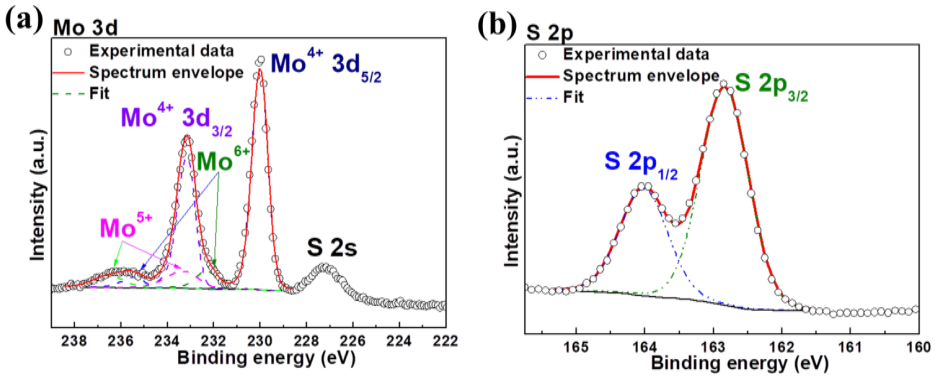

FIG. 2. High-resolution XPS spectra of (a) Mo 3d and (b) S 2p orbitals of a monolayer MoS_2 film.

The higher oxidation states of Mo show that 21% of the Mo element was bound to the O element and as a result, 21% of the film was oxidized. The resulting stoichiometry was closer to $MoS_{1.8}$. Table S3 summarizes the binding energies of the three oxidation states of Mo and S components as well as the composition.[41]

To fabricate the FGr trapping medium, we first grew a CVD monolayer of graphene on a copper substrate. The copper was rolled and loaded into a 1-in. furnace. After the temperature was increased to 1000 °C, the methane and hydrogen (CH_4/H_2 = 20 sccm/20 sccm) were introduced for 20 min. After the furnace cooled to room temperature, the graphene sample on Cu was loaded into the PECVD chamber and subjected to CF_4 plasma for 40 min at 200 °C, transforming the pristine graphene into FGr. Finally, the FGr was transferred onto the tunnel oxide previously deposited onto the MoS_2 channel. Raman spectra were acquired to determine the quality of pristine graphene (PG) and FGr, as shown in Fig. S2. The PG showed two main peaks G (~1590 cm^{-1}) and 2D peaks (~2700 cm^{-1}) that indicated the in-plane vibrational mode and two phonon mode, with a negligible D band indicating the high crystalline phase with low defects. Moreover, the I_{2D}/I_G ratio was 2.3, indicating the presence of monolayer graphene. After the CF_4 plasma treatment with increasing exposure time, the D peak suddenly intensified, whereas the 2D peak intensity gradually decreased. This observation indicated the introduction of lattice disorder due to CF_4 plasma treatment. Moreover, the G peaks become broader, and a new D' at ~1623 cm^{-1} peaks originated from the intravalley resonance. As the exposure time increased up to 40 min, all the peaks disappeared, indicating that the FGr was highly insulated.[42]

B. Fabrication of nonvolatile memory (NVM) device

After patterning the MoS_2 channel via optical lithography and reactive ion etching (RIE), 50-nm Ni source/drain contacts were deposited by a thermal evaporation and lift-off process. 5 nm SiO_2 tunnel oxide was deposited onto the MoS_2 channel by plasma-enhanced chemical vapor deposition (PECVD) at 300 °C. FGr grown by CVD was then transferred onto the tunneling oxide followed by a 50-nm-thick HfO_2 film deposited by atomic layer deposition (ALD) at 250 °C acting as the blocking oxide (BO). Finally, a 50-nm-thick Ni gate was patterned by photolithography and lift-off processes. The schematic structure and optical image of the MoS_2 memory device are shown in Figs. 3(a) and 3(b). The electrical measurements, I–V curves, and P/E characteristics were determined using a Keithley 4200A-SCS semiconductor parameter analyzer.

III. RESULTS AND DISCUSSION

Figure 3(c) shows the transfer characteristics of the MoS_2 NVM device with V_{DS} ranging from 0 V to 1 V. The linear I–V characteristics in Figure S3 under a drain bias ranging from −1 V to 1 V shows ohmic contacts between Ni and MoS_2. At V_{DS} = 0 V, the current is approximately 50 pA for all ranges of V_G, indicating that I_{DS} is effectively the drain current and not due to gate leakage current. The I_{DS}–V_{GS}, Fig. 3(c), shows n-type transistor characteristics with an on/off ratio of ~10^4. The carrier mobility was determined using

$$\mu = (L/WC_{OX}V_{DS})(dI/dV), \quad (1)$$

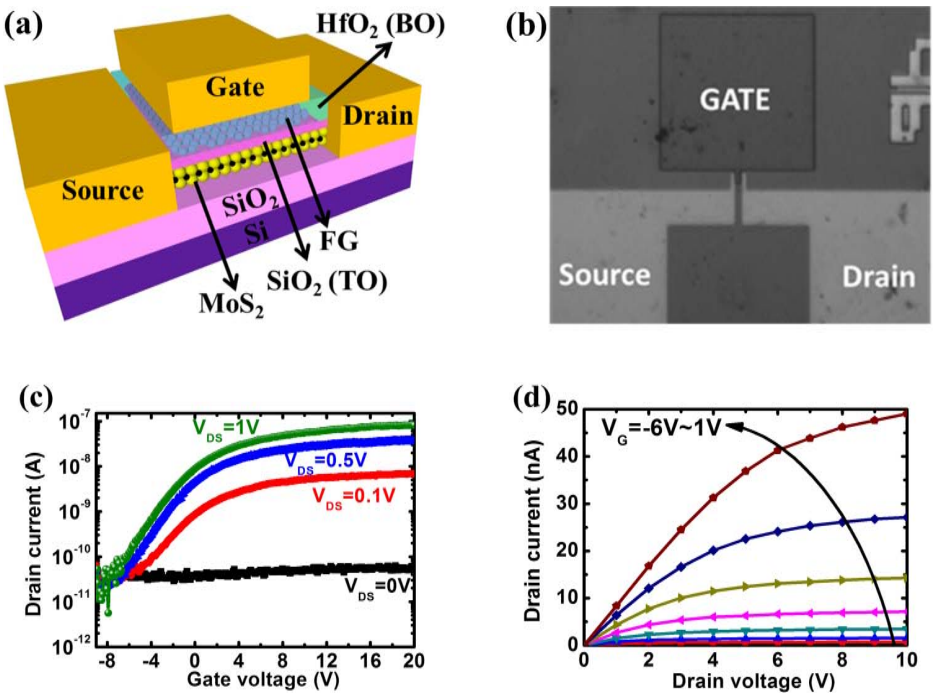

FIG. 3. (a) Three-dimensional schematic structure of MoS_2-FGr NVM. (b) Optical top-view image of MoS_2-FGr NVM. (c) I_{DS}-V_{GS} characteristics of the MoS_2 device with the FGr trapping medium; the drain current is observed at different V_{DS} from 0 V to 1 V. (d) I_{DS}–V_{DS} characteristics of the MoS_2 device under an extended drain bias from 0 V to 10 V.

where L is the channel length, and W is the channel width, $V_{DS=} = 1$ V, $C_{OX} = 270$ nF cm^{-2} and dI/dV is the slope of the linear regions of the I_{DS}–V_{GS} characteristics. The threshold voltage (V_{th}) measured is −1.8 V and the field-effect electron mobility (μ_e) in the linear region at $V_{DS} = 1$ V is 0.1 cm^2 V^{-1} s^{-1}.

Figure 3(d) illustrates the output characteristics of the MoS_2 device with FGr for V_{GS} from −6 V to 1 V. The device exhibits a maximum drain current of 50 nA at $V_{GS} = 1$ V and $V_{DS} = 10$ V. The partial oxidation of the MoS_2 channel may explain the limited mobility and current output. These properties could be improved by tuning the growth parameters and taking special care in handling the MoS_2 during processing. Note that the low mobility does not prevent the memory operation since in this configuration, the electron transfer in vertical from the channel to the TM. The I_{DS}–V_{GS} and I_{DS}–V_{GS} characteristics of the MoS_2 FET without FGr are shown in Fig. S4. This device exhibits a similar on/off ratio as compared to MoS_2 FET with FGr. Therefore, the gate control is not affected by FGr in the memory device owing to the ultrathin thickness of FGr. Figure 4 shows the I_{DS}–V_{GS} hysteresis of the MoS_2 devices with and without the FGr storage layer. The trapping effect is determined by a circulatory gate voltage sweep under a fixed source and/or drain voltage ($V_{DS} = 0.1$ V). We observed a noticeable I_{DS}–V_{GS} hysteresis for both devices; however, the device with FGr exhibits a threefold (25 V) memory window compared to the FGr-less devices (9 V) for the same sweep voltages. A large memory window is an advantage to delay the data retention loss.

The shallow traps at the substrate/MoS_2 interface or the MoS_2/SiO_2 as well as the water and/or oxygen absorbed on the MoS_2[43] are often responsible for V_{th} hysteresis in 2D FET devices.[23] Such an effect, Fig. 4(a), has been exploited for memory devices.[44,45] this memory window typically disappear within minutes as the shallow traps are not located deep enough to withstand thermo-ionic emission. We have shown in a previous study that it is possible to improve the channel performance using a C_1F_1 FGr layer as a passivation, substantially increasing the mobility and current.[42] Such an interface screens the Coulomb charge effect and improves the mobility as well as the current output. The mechanism is different when FGr is implemented as the trapping medium [Fig. 4(b)]. Here, when V_G is swept from the negative to positive voltages (−20 V to 30 V), electrons tunnel through the SiO_2 barrier into the FGr where they are trapped.[8] These electrons screen part of the gate electric field yielding to saturation, which sets the programming state and leads to a positive shift of the V_{th}. On the other hand, the shift is negative when V_G is swept from positive to negative values. Here, electrons are removed (holes injected) from the FGr to the MoS_2 channel down to a V_G equal to −20 V, setting the erase state. Having demonstrated the trapping efficiency of the FGr layer, we measured the P/E characteristics of the MoS_2-FGr device with pulse widths of 1 μs up to 1 s and voltages of ±12, ±14 and ±16 V applied on the top gate, Fig. 5(a). Operating the device under a pulse of ±16 V for up to 1 s yielded a maximum memory window of 4.7 V. Note that the erase saturation of the NVM is faster than the program saturation due to the tunnel oxide CB and VB band offsets with respect to FGr. The energy diagram of the MoS_2 device with FGr in a flatband state is illustrated in Fig. S5. The electron affinity (χ) and bandgap (E_g) are, respectively, 3.4 eV and 2 eV for monolayer MoS_2,[46] 2.4 eV and 5.7 eV for HfO_2,[41] 5.1 eV and 3 eV for FGr,[33,47] 0.9 eV and 8.9 eV for SiO_2. The work function (ϕ_m) of the nickel gate is 5.1 eV.[48] Using Ni/MoS_2/HfO_2/Ni and Ni/MoS_2/SiO_2/Ni test structures, we have determined comparable barrier height for the MoS_2/SiO_2 interface, Fig. S6. Because the electron barrier is high, larger voltages are required to tunnel electrons through. We have carried out simulations for different energy barrier heights (Figs. S7 and S8) demonstrating that direct and Fowler–Nordheim tunneling are the dominant charge transfer mechanisms. Similarly, due to the hole barrier being smaller, the erase saturation is reached more rapidly. An alternative tunnel oxide could be utilized to improve the P/E mechanism. Note that the memory window and P/E voltages achieved are comparable to flash memory and charge trapping devices.[49]

To determine the room temperature data retention of the NVM device, Fig. 5(b), we applied a + 16 V/1 s pulse on the gate inducing a V_{th} shift of 3.3 V. We then acquired an I_{ds}–V_{gs} characteristic at $V_{DS} = 0.1$ V by sweeping the gate voltage from −8 V to 4 V. V_{th} is determined by fitting the plot. This fitting operation is reproduced for different time intervals. The I_{ds}–V_{gs} characteristic exhibits a time-dependent decay (Fig. S9). The measurements were continuously acquired at regular time intervals until 10^4 s. The extrapolation to 10 years shows a 50% charge loss, which is essentially due to the poor retention of the holes, primarily associated with the small barrier seen by the holes at the blocking oxide (HfO_2) interface, Fig. S9. Here, we erased the memory close to the erase saturation observed in the P/E curves of Fig. 5(a). Our devices exhibit a neutral V_{th} of −2.3 V close to this erase saturation level; it is therefore unlikely that the leakage current observed is subsequent

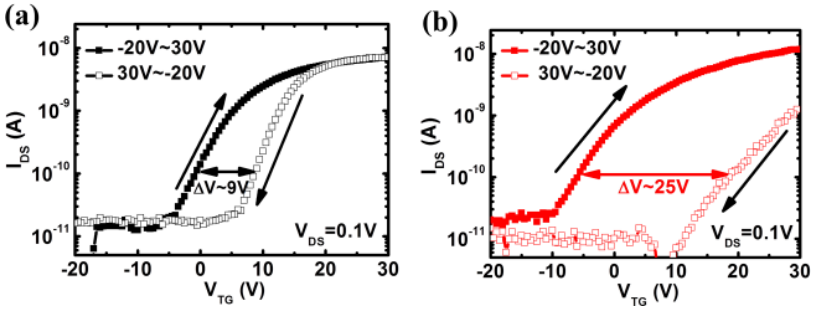

FIG. 4. I_{DS}–V_{GS} hysteresis characteristics of (a) MoS_2 device without FGr and (b) MoS_2 device with FGr. The devices with FGr present a memory window nearly three times larger than devices without FGr.

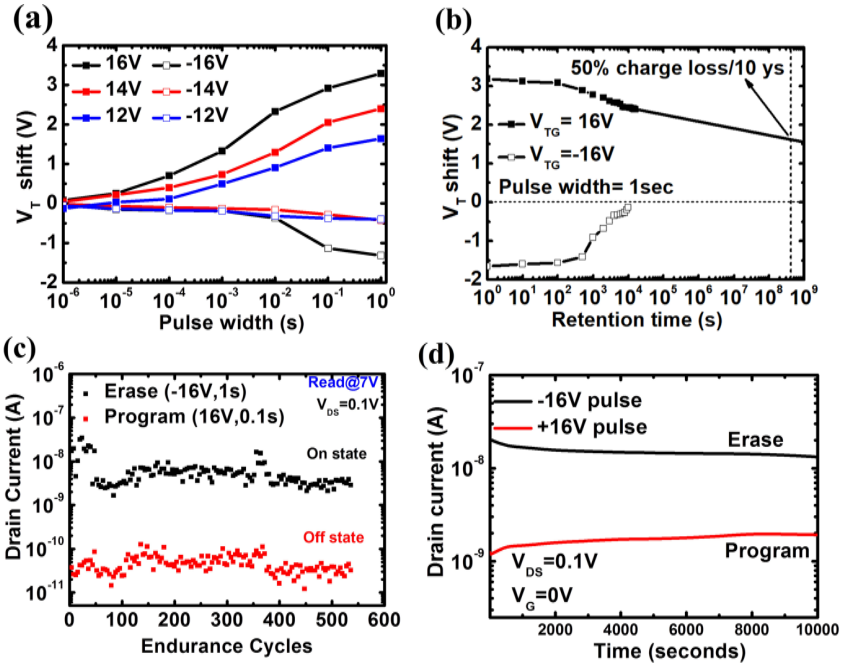

FIG. 5. Programming and erase curves, endurance, and data retention of the memory device. (a) Vth shift with different P/E pulse widths and voltage. The memory window reaches 4.7 V for at ± 16 V for 1 s. (b) Room temperature data retention characteristics. Measurements have been performed for a minimum of 10^4 s. (c) Endurance characteristics for device cycled up to 550 cycles. (d) P/E currents up to 10^4 s with 0 V reading voltage.

to an over erase of the memory device. We believe that the limited barrier at the HfO_2/FGr interface cannot efficiently block the holes, and the thermo-ionic process even at room temperature causes a large leakage current that translates into a steep loss in the erase V_{th} starting at 10^3 s. An alternative blocking oxide such as hexagonal boron nitride (h-BN) is under investigation.[50] Comparing with HfO_2, h-BN is an isomorph of graphene and a dielectric with a wide bandgap (5.9 eV) and lower electron affinity (2.0 eV).[51] Figure 5(c) shows the endurance characteristics of the MoS_2-FGr devices acquired upon cycling. The acquisition was carried out with pulses of ±16 V for 1 s and 0.1 s applied to the gate while the drain current was at $V_{ds} = 0.1$ V and the source was grounded. No obvious degradation was observed up to 550 cycles, indicating the good quality of the stack. Finally, to verify whether the memory was non-volatile, the current changes over 10^4 s while maintaining a constant read voltage are shown in Fig. 5(d). The P/E currents of MoS_2-FGr devices are stable and exhibit a factor 10 difference that clearly discriminates the P and E states.

IV. CONCLUSIONS

In this work, we developed the growth of a uniform monolayer CVD MoS_2 on a SiO_2 substrate. The material was integrated as a channel for nonvolatile memory devices using fluorographene as the charge storage medium and HfO_2 as a blocking oxide. The on/off ratio was observed to reach 10^4 with particularly low leakage current. The memory window achieved with FGr was three times larger (~25 V) than without for pulses lower than ±16 V, demonstrating the added value of FGr as a charge storage medium. The programming efficiency is limited because the V_T/V_G ratio is low, but the devices still exhibited a 4.7 V window at ±16 V for 1 s with an endurance of at least to 550 cycles. The extrapolation to 10 years shows a 50% charge loss for the room temperature data originating from the small barrier to holes at the FGr/HfO_2 interface. These results suggest that the FGr-based MoS_2 heterostructure could be optimized by adequate bandgap engineering for nonvolatile memory applications.

SUPPLEMENTARY MATERIAL

See the supplementary material for Raman spectra of graphene and fluorographene with various CF_4 plasma exposure times (10, 20, 30, and 40 min). The Raman and PL mapping of MoS_2 at 84 K and 300 K, along with the tables of E^1_{2g} and A_{1g} modes' positions and shifts with temperature, are also provided. The binding energies of chemical orbitals and the FWHM of the XPS peaks for both Mo and S elements are also presented, as well as the FN tunneling calculations. The time-dependent I_{ds}–V_{gs} characteristics are also presented to determine the V_{th} shift for data retention.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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