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Design and Simulation of an Associative Memory Circuit with a Nanoscale Ionic Li_xTiO_2 -based Synaptic Transistor

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SNNs (Spiking Neural Networks) demonstrate important biorealistic learning mechanisms, like associative memory, verified by Pavlov's dog experiment.¹ The experiment involves four steps: (1 and 2) The dog's mouth salivates upon seeing food (unconditioned stimulus - US) but not upon hearing a bell (neutral stimulus - NS). (3) During the conditioning period, the dog learns to associate the bell sound with food. (4) After conditioning, the bell sound alone triggers salivation (conditioned stimulus - CS) without the need for visual input.

Pavlov's dog experiment can be modeled by a neural network circuit, comprising two synapses and a neuron. The stimulations are represented by electrical pulses sent to synapses 1 and 2, respectively. Eventually, the output neuron starts to respond to CS alone (Figure 1, top panel).

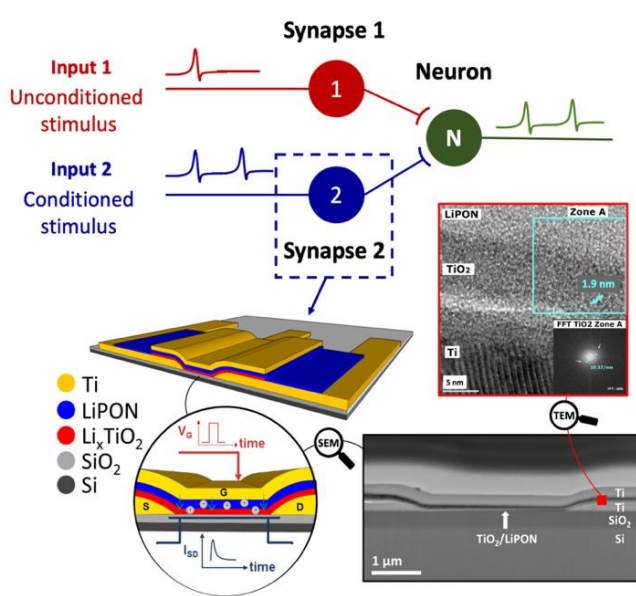


Figure 1. Simple neural network model for Pavlov's dog experiment, in which the "Synapse 2" is modeled by a Li_xTiO_2 -based electrochemical synaptic transistor. The insets display the cross-sectional views of the elaborated device, as seen through TEM and SEM imaging.

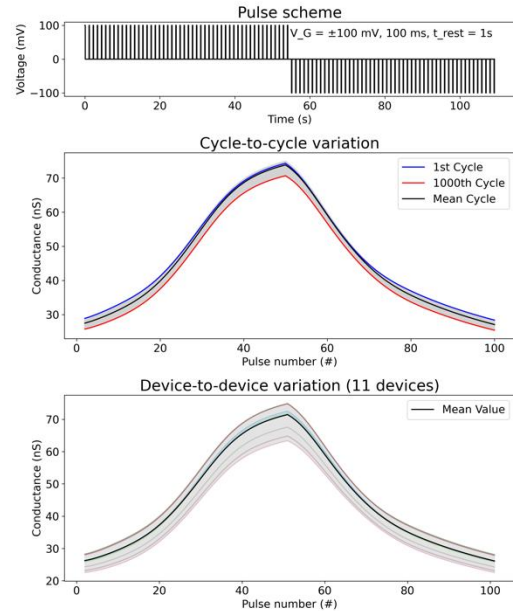


Figure 2. Characterization scheme of the SynTs (top panel) with cycle-to-cycle variation (middle panel) and device-to-device variation across the wafer (bottom panel).

Prior works have demonstrated Pavlov's Dog behavior using two-terminal memristors.² Three-terminal synaptic transistors have also shown promises, offering advantages over two-terminal devices.^{3, 4} However, existing circuits add complexity with computer interfaces or op-amps, and the materials used in some three-terminal synaptic transistors present wafer-scale integration challenges.^{5, 6}

Our main objective is to emulate associative memory behavior using a recently reported three-terminal all-solid-state (Li_xTiO_2 -based) device called SynT, benefiting from its outstanding properties such as high wafer scale integration possibilities and ultralow energy consumption.⁷ The transistor stack consists of an 10nm Li_xTiO_2 channel, a solid-state electrolyte made of 200nm LiPON, and a Ti top gate as illustrated by SEM and TEM observations (Figure 1, bottom panel). The observed nano-inclusions of TiO_2 embedded in the channel

amorphous matrix might play a pivotal role in the linear conductance switching, stability, and resilience of the tested SynTs. The device high stability feature is illustrated by cycle-to-cycle and device-to-device variation tests (Figure 2).

We model the SynT behavior with a combination of a small capacitor ($C_{\text{SynT}} = 1 \text{ nF}$) to simulate the behavior of SynT gate stack, a resistor ($R_{\text{SynT}} = 10 \text{ G}\Omega$) used to mimic the high leakage resistance of the gate stack, and a transistor U in which the current I_{DS} can be controlled by the gate voltage V_G to model the conductance evolution (Figure 3a). From the experimental measurement of the channel conductance G_{DS} can be modeled as a linear function of gate voltage V_G (Figure 3b). The model response to a current pulses train is simulated in Figure 3c.

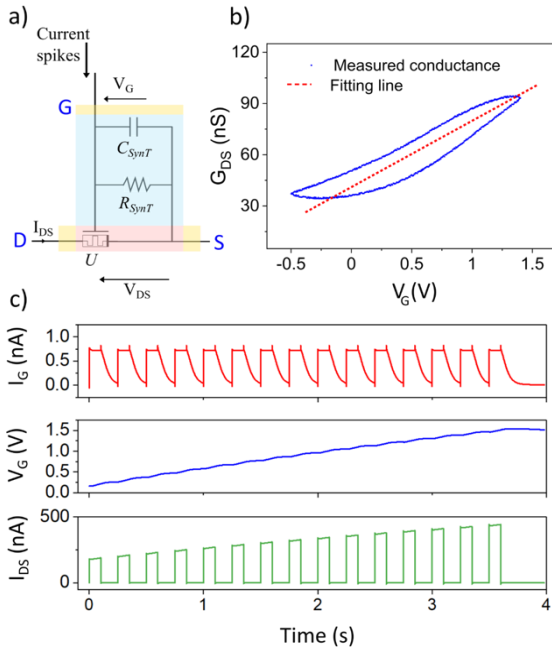


Figure 3. a) Synaptic transistor compact model proposed. b) Implementing the measured conductance as a function of the gate voltage. c) Simulation of the SynT response (Top) The writing current pulses. (Middle) The increase of gate potential (simulated by the potential across C_{SynT}). (Bottom) The channel current I_{DS} of SynT.

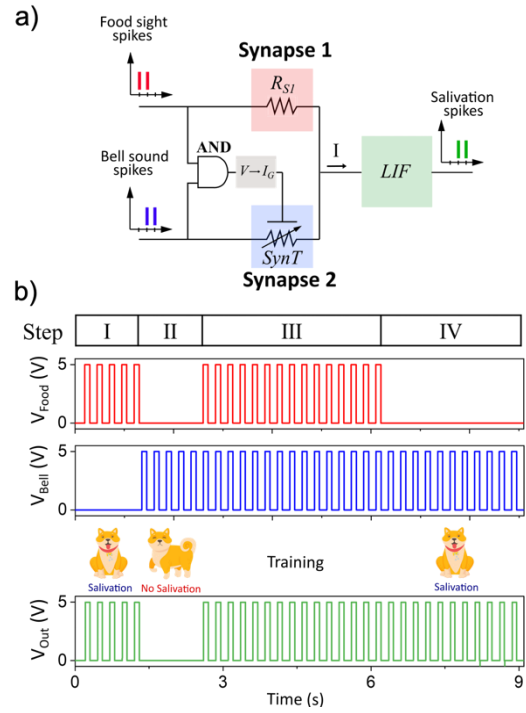


Figure 4. a) Schematic of the circuit used for the simulation of the associative memory development. b) Simulation of the development of the associative memory, with the neural network circuit using our device model.

Figure 4a illustrates the circuit design that we propose for the demonstration of the associative memory. We set the weight value of Synapse 1 by using a $10 \text{ M}\Omega$ resistor, while the adaptive SynT serves as Synapse 2 with synaptic plasticity. V_{FOOD} and V_{BELL} inputs are connected to an AND logic component. Simultaneous arrival of both inputs triggers the AND component, producing a 5V output voltage, which is converted to a current through an interface circuit (not shown). The current is then injected into the gate of SynT (Synapse 2), causing its conductance to gradually increase during the conditioning period. By employing these components, we successfully reproduced Pavlov's dog experiment in 4 successive steps with our neural network circuit, as shown in Figure 4b.

In conclusion, we showed the emulation of an associative memory, with the design and simulation of a simple neuromimetic circuit composed of an electrochemical all solid-state synaptic transistor component. The interesting features from the study may give insights towards future bio-inspired embedded networks.

¹ Clark, R.E. 2004. Integrative Physiological & Behavioral Science, ² Pershin, Y.V. and Di Ventra, M. 2010. Neural Networks, ³ Bichler, O. et al. 2013. Neural Computation, ⁴ Ha, S.D. et al. 2014. Physical Review Applied, ⁵ Yang,

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