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Bidimensional materials for low power and energy harvesting devices: Modulation of the electronic properties of graphene

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**ACCREDITATION TO SUPERVISE RESEARCH
(HABILITATION À DIRIGER DES RECHERCHES)**

**OF
THE UNIVERSITY PIERRE AND MARIE CURIE (UPMC)**

By

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Bidimensional materials for low power and energy harvesting devices: Modulation of the electronic properties of graphene

Presented at Paris, June 1st 2016 :

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Abstract

Since my appointment at the University Pierre and Marie Curie (UPMC) in the Group of Electrical Engineering of Paris (GeePs) PHEMADIC division, my research interests focused on heterojunctions for nanoelectronics and photo detection devices. Notably, I was interested in the integration of 2D materials that present a great potential for these topics. However, my first studies considered epitaxial diamond based power and UV detector heterojunctions. This work was a collaboration with (LPICM-Ecole Polytechnique) and the National Institute for Material Science (National Institute for Material Science-Japan) that yielded a high on/off ratio device. Nevertheless, the difficulty to achieve pn junction on diamond hindered further development and I shifted my interest towards the modulation of the electronic properties of graphene keeping in mind the aforementioned applications. This new direction was possible thanks to strong national (Dr P. Roca i Cabarrocas du Laboratoire de Physique des Interfaces, Dr A. Ouerghi and Dr A. Madouri from Laboratoire de Photonique et Nanostructures - CNRS) and international partnerships (Pr S. Oda - Tokyo Institute of Technology, Pr Y Hee Lee - Sungkyunkwan University, Pr C.S Lai - Chang Gung University and Dr S. Kanjanachuchai - Chulalongkorn University) within the framework of the Labex NanoSaclay (post doc: F.Gunes (2012-2014) and Phd student H.Arezki (2012-2016)) and the ICT-ASIA programme (PhD K-I Ho (2013-2016)). In that context, we studied several heterostructures such as *e.g.* silicon nanocrystals/graphene, fluorographene/graphene and memories, h-BN/graphene for field effect devices and transparent electrodes. Moreover, in collaboration with Dr K.Fukumoto and Pr S.Koshihara at Tokyo Institute technology, we have investigated the ultra fast carrier dynamics in CVD graphene superlattices by fs-PEEM (femtosecond-Photomission Electron Microscopy). We have been able to map the carrier lifetime across a sample and we are trying to correlate the observation to the twist angle of the superlattices. In addition, I extended this collaboration to synchrotron Soleil in an attempt to observe the band structure of these superlattices. Another field of research concerned the study of photovoltaic heterojunctions by modulated photo-luminescence technique (PhD student Ming Xu 2013-2016). Within the framework of ANR (SMASH IBC^2) and European project (HERCULES) we have investigated and benchmarked various passivation by measuring the carrier lifetime (*ms* for crystalline silicon as opposed to *ps* for graphene). In addition, we have extended the range of data available to the community for the radiative recombination coefficient B down to 20 K. This manuscript is structured around three different sections. The first section presents a detailed resume including my bibliography. In the second section, I will present a summary of my research activity. For the sake of clarity, I will only present my work since my appointment at the University Pierre and Marie Curie (UPMC)

as an Associate Professor in Electrical Engineering. Nevertheless, links to my previous research notably my work as a Senior Scientist at NXP-TSMC research centre (formely Philips Research Europe) will appear in the various sections. This second section throughtout the thesis I directed or co-directed will include my activity on (i)diamond and silicon based heterojunctions as well as (ii) bidimensional (2D) materials such as graphene. This latest was my main research topic for the last five years. The last section, will consider my prospective research for the coming 5 years dedicated to the low power applications of advanced materials. In this part, I will consider the exploitation of 2D layered materials for two domains : nanoelectronic memory devices based on a patent i recently filed and the integration of topological insulators (TI) in thermoelectric generators (TEG). I was acquainted to both domains since my PhD and I believe the remarkable properties of 2D materials may be of interest for the data retention and power consumption in non volatile memories on one hand but also improve the figure of merit in order to demonstrate thermoelectric generators using topological insulators.

Résumé en français

Depuis mon intégration à l'Université Pierre et Marie Curie (UPMC) au Laboratoire de Génie Electronique et Electrique de Paris (GeePs) pole PHEMADIC, je me suis intéressé aux hétérojonctions à base de semi-conducteurs pour les applications nanoélectroniques et de photo détection notamment l'intégration des cristaux bidimensionnels, qui présentent depuis l'avènement du graphène un fort potentiel applicatif. Mes premiers travaux au sein du pôle PHEMADIC ont porté sur le diamant épitaxié, matériau grand gap qui présente des propriétés remarquables pour la photo détection UV et l'électronique de puissance. Dans ce contexte, en collaboration avec le Laboratoire de Physique des Interfaces et Couches Minces (LPICM-Ecole Polytechnique) et le National Institute for Material Science (NIMS-Japon) nous avons développé une hétérojonction diamant (type p 500 nm)/a-Si:H (10 nm) à fort facteur de redressement. Néanmoins, la difficulté à produire du diamant de type N a ralenti le développement d'autres hétérojonctions. Dès lors, j'ai décidé de concentrer mes efforts sur le graphène cru sur des surfaces technologiquement viables. Mon axe de recherche s'articule autour de la caractérisation et la modulation des propriétés électroniques de ces matériaux 2D, j'ai étudié essentiellement deux types de graphène produit par mes partenaires nationaux et internationaux. Dans ce cadre, et avec le soutien du labex NanoSaclay, j'ai pu mettre en place une plateforme GraPhIC (Graphene Growth Interface and Characterization) nous avons développé des instrumentations et des structures de test que nous avons caractérisé au sein du consortium (post doc: F.Gunes (2012-2014) et doctorant H.Arezki (2012-2016)). Ces travaux ont permis d'acquérir une expertise dans des techniques spectroscopiques photo électroniques et Raman d'une part mais aussi de développer des composants nanoélectroniques tels que des transistors tout graphène, des hétérostructures pour des applications photovoltaïques et mémoires. Ces travaux sont le fruit de collaborations fortes nationales (Dr P. Roca i Cabarrocas du Laboratoire de Physique des Interfaces, Dr A. Ouerghi et Dr A. Madouri du Laboratoire de Photonique et Nanostructures - CNRS) et internationales (Pr S. Oda de Tokyo Institute of Technology, Pr Y Hee Lee de Sungkyunkwan University, Pr C.S Lai de Chang Gung University et Dr S. Kanjanachuchai de Chulalongkorn University) que j'ai pu établir via des invitations (Japon/Taiwan) et le projet 2D Nanotech (STIC-ASIE 2013-2015). Dans le cadre de ce projet, nous avons étudié différentes interfaces *e.g.* graphène/nanocristaux (Pr S. Oda), graphène/fluorographène (Pr C.S Lai - doctorant Kuan-I Ho 2013-2016). Mes travaux avec le Japon (Dr K.Fukumoto et Pr S.Koshihara) ont notamment porté sur la mesure de la dynamique ultra rapide des électrons dans des superstructures en graphène par fs-PEEM (femtosecond-Photomission Electron Microscopy) développé au Tokyo Institute of Technology que je visite chaque année depuis 2012. Nous avons ainsi pu établir

une distribution spatiale de la dynamique des porteurs avec une technique originale et tentons de corrélérer les différentes dynamiques à l'angle de rotation entre chaque couche de graphène. Par ailleurs, mes travaux se sont étendus dans le cadre d'une collaboration avec le synchrotron Soleil pour la mesure des structures de bandes sur les superstructures en graphène CVD. Un second axe de recherche concerne l'étude des hétérojonctions photovoltaïques par des techniques de photoluminescence notamment la photoluminescence modulée. Nous avons développé des techniques de luminescence pour la mesure des propriétés à l'échelle micro/nanométrique et en fonction de la température (doctorant Ming Xu 2013-2016). Nous avons étudié différents type de passivations dans le cadre de projet ANR (SMASH IBC^2) et européen (HERCULES) pour déterminer le temps de vie des porteurs majoritaires (ms pour le silicium à opposer au ps pour le graphène) pour différents types d'hétérojonctions.

Ce manuscrit est constitué de trois parties : la première partie présente mon curriculum vitæ détaillé dans lequel j'y ai inclus ma bibliographie. Dans la seconde partie, je présente un résumé de mes travaux de recherche. Dans un soucis de cohérence et clarté, je n'ai inclus que mes travaux depuis ma prise de fonction en tant que maître de conférences à l'UPMC (2009). Néanmoins, des références à mes travaux antérieurs notamment en tant que scientifique au sein de la division recherche de NXP-TSMC Research Centre (IMEC - Leuven *ex* Philips Research Europe) apparaîtront dans les différentes parties. Cette section au travers de mes encadrements et co-encadrements de thèse effectués durant la période 2009-2016 porte sur les travaux suivants : (i) hétérojonctions à base de diamant et de silicium (ii) ingénierie des propriétés électroniques du graphène. Ce dernier point a constitué mon activité principale ces cinq dernières années. Enfin, dans la dernière partie, je propose deux axes de recherches pour les cinq prochaines années qui s'articulent sur l'étude des matériaux 2D (isolants topologiques inclus) et leur potentiel pour les applications électroniques basses puissances notamment les mémoires non volatiles et la conversion thermoélectrique. J'ai été amené à travailler sur ces deux sujets depuis mon doctorat et il m'apparaît pertinent d'investiguer l'apport de la nanostructuration des matériaux 2D et de leurs propriétés électroniques remarquables sur la performance des mémoires à piégeage de charge en terme de réduction des puissance d'injection et de rétention des électrons d'une part et d'autre part démontrer une augmentation du facteur de mérite thermoélectrique en intégrant des isolants topologiques sur un concept de thermogénérateur que j'avais déjà démontré en technologie microsysteme.

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Chapter 1

Research activity 2009-2016

1.1 Foreword

My research started in 1999 during my PhD at the Institut d'Electronique de Microélectronique & de Nanotechnologies (IEMN-Lille, France) from 1999 to 2002¹. I designed, fabricated and characterized infrared sensors based on thermoelectric micro radiometer in MEMS technology. particularly, I developed a highly sensitive thermopile based on the doping of polysilicon thermoelements². This research led to the development of a new planar device using a suspended thermopile designed to prevent the encapsulation under atmosphere³.

Following my PhD, I joined The University of Cambridge Engineering Department (CUED) and the Centre for Advanced Photonics and Electronics (CAPE) as a research associate (06/2003-07/2006) in the Electronic Devices & Materials Group head by Pr W.I.Milne and under the supervision of Dr D.F Moore within the framework of an EPSRC funded project entitled APOEM (250k£) : Active Packaging for Optoelectronic and Electronic Microsystems. In this context, I utilized the experience acquired during my PhD to developed micromechanical structures for the alignment of photonics devices as well as characterization set up. Notably, I implemented a force measurement set up to measure mN forces delivered by thermomechanical microactuators⁴. In this framework, I've been involved in national and international collaborations with Tokyo University, Imperial College London, EPFL Lausanne as well as the company Micro Circuit Engineering that was interested in such MEMS devices for its products⁵⁻⁷. Moreover, I participated to the launch of Owlstonenanotech Ltd a spin off of CUED for which I prototyped as a consultant (06/2004-07/2006) a field asymmetric microspectrometer*.

In 2006, I joined Philips Research (acquired by NXP and TSMC in 2008) Europe and became a senior scientist at NXP-TSMC Research Centre located at IMEC (Leuven, Belgium) & The High Tech Campus (Eindhoven, The Netherlands). I participated in different work packages in the NEMeSyS European Project (4M€)⁸ developing future non-volatile memories for 45nm and beyond integrating advanced tunnel barriers such as charge trapping devices⁹. I was in charge of the technology and the characterization of advanced memory devices using high-k materials and metal gate. This work led to the demonstration of advanced charge trapping concepts based on the

* www.owlstonenanotech.com

integration of high- k and metal gate for 45 nm and beyond. This work was partly within the Industrial affiliated program within IMEC with various semiconductor research groups. I authored several technical notes on the topic^{10, 11-13}. I participated to the demonstration of a new programming mechanism entitled PAHHI (Punch Through Assisted Hot Holes Injection) to programme and erase thick tunnel oxide flash devices¹⁴. I filed four patents including a thermoelectric sensor using the CMOS integration technology to create a temperature gradient between two thermoelements¹⁵.

In September 2009, I was appointed as an Associate Professor in Electrical Engineering at Pierre and Marie Curie University (UPMC), Paris. I started my research on diamond based devices and progressively shifted to graphene and photovoltaic heterostructures. I coordinated the project GraPhIC (Graphene growth Interfaces and Characterization) funded by Labex NanoSaclay in which we developed a characterization platform for graphene based devices as well as synthesis using CVD (post doctoral research associate Dr F. Gunes). From September to December 2012, I was an invited Associate Professor at the Quantum Nanoelectronic Research Centre (QNERC) at Tokyo Institute of Technology/Japan in Professor S.Oda's lab. I closely work with Pr S. Koshihara and Dr K.Fukumoto whom I visit every year to investigate the lifetime in CVD graphene superlattices using their fs-PEEM technique. Since March 2013, I head the ICT-ASIA funded (2D Nanotech) research exchange programme in collaboration with Tokyo Institute of Technology (Japan), SDRL (Chulalongkorn University-Thailand) and Semiconductors lab (Chang Gung University-Taiwan). I am also the French coordinator for an International nanoscience master degree (XNEM 2014-2017) funded by the EU-TEMPUS programme for the Middle East and North Africa region*. I coordinate the semiconductors physics course and we will welcome 3 students at UPMC to carry out their master's thesis.

1.2 Diamond based heterojunctions

My integration at GeePs lab (formerly LGEP lab) started with the study of diamond based heterostructures. This work was a collaborative research between GeePs, the Physics of Interfaces and Thin film lab LPICM and the National Institute for Materials Science (NIMS - Japan). Despite the tremendous challenges to overcome for its synthesis and doping, diamond remains an attractive wide band gap semiconductor (5.5 eV) for a range of electronic devices especially those requiring high power and operating in harsh environment (temperature, radiations)¹⁶. Amongst the concepts that raised a lot of interest are Schottky-barrier diodes (SBD), Schottky-barrier Photodiode (SPD) as well as pn and p-i-n junction (PND) with (N)-doped diamond¹⁷⁻¹⁹. The development of reliable bipolar devices is a key technological building block for the design and fabrication of electronic devices. For that purpose, it is necessary to obtain device-grade quality for the n as well as the p -type diamond. Although various groups have devoted a lot of efforts to incorporate donor atoms such as (P)-Phosphorus or (As)-Arsenic into semiconductor diamond, the resistivity as well as junction characteristics such as built-in voltage and rectification ratio remain too

* <http://www.arabnano.eu/>

poor to envision competitive device. In addition, increasing the donor concentration beyond a certain level has proven to be detrimental to the diamond integrity. The aforementioned technological issues to fabricate bipolar devices on diamond homojunctions have raised interest into the study of heterojunction with semiconductor materials such as aluminum nitride (AlN) or zinc oxide (ZnO)^{20,21}. Such a structure combines the properties of both semiconductors and may lead to outstanding performance in terms of rectification ratio. Note that if these heterostructures are fabricated with transparent electrodes, *pn* and/or *p-i-n* diamond based heterojunctions find applications in photo detection as well as light emitting diodes²². In our work we have integrated amorphous silicon (a-Si:H). 500 nm thick diamond epilayers were grown by the dissociation of CH_4 and H_2 gas precursors. The B species inside the microwave plasma chemical vapor deposition (MPCVD) chamber were incorporated into the diamond epilayer with a concentration ranging from 10^{15} to $10^{16} cm^{-3}$. Following the diamond growth, the samples were oxidized to remove the surface conductive hydrogenated layer and introduced in a standard RF glow discharge reactor for the amorphous and microcrystalline silicon deposition. Hydrogenated amorphous silicon layers were deposited at 175 °C on these substrates by plasma enhanced chemical vapour deposition. A 30 s hydrogen plasma treatment of the p-type diamond epi layer was performed just before the deposition of a 50 nm intrinsic a-Si:H from the dissociation of pure silane at 7 Pa under an RF power of $5 mW/cm^2$. After the intrinsic a-Si:H we deposited 50 nm thick n-type amorphous films by adding phosphine to silane in the case of n+a-Si:H layers. Fig.1.1 illustrates the energy band diagram of the studied device.

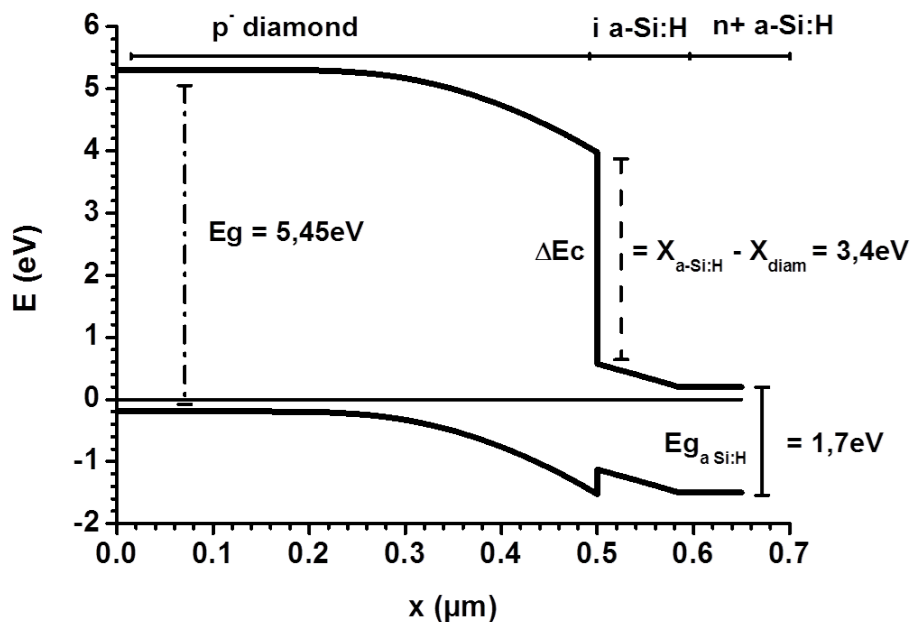


Fig. 1.1 Schematic of the energy band diagram for diamond/a-Si:H/n +a-Si:H at equilibrium

The whole diamond layer is fully depleted at -2.5 V reverse bias. The experimental space charge region is estimated around 570 nm which corresponds approximately to the thicknesses of the epi-diamond and the intrinsic a-Si:H. Fig.1.2 shows the current–voltage characteristics (J–V)

of the heterojunction diodes in semi-logarithmic scale. The reverse current is below the detection limit up to 440 K. The heterojunction diodes exhibit a pronounced rectifying behaviour (up to 10^9 or more) for a current density of 10 mA/cm^2 at +2 V bias. The magnitude of the ideality factor n and the variation of $J_0(T)$ as a function of temperature provide information on the carrier transport mechanism. We could distinguish 2 regimes of operation indicating the presence of different transport mechanisms. For very low bias *i.e.* $0 < V < 1$ V, the characteristic of the heterojunction with temperature follows the SBD's model and therefore presents a similar ideality factor n 1.1. However, for the second regime of operation *i.e.* $1 < V < 2.5$ V, n is much larger than the value of 2 expected from the Sah–Noyce–Shockley theory.

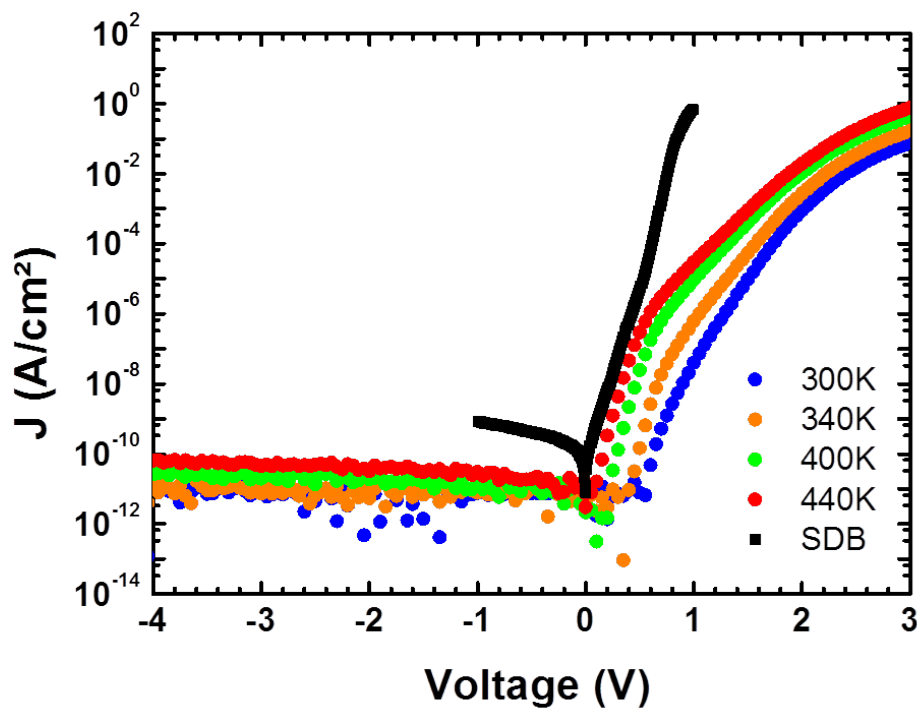


Fig. 1.2 Current–voltage characteristic of a diamond/a-Si:H/n+ a-Si:H heterojunction versus temperature. The SBD characteristic, measured at room temperature, is shown for comparison. The inset shows the reverse current versus voltage until breakdown at -160 V at 300 K

In this regime, n reaches 3.6 and remains approximately constant with temperature. This observation is in contradiction with the trend observed in other heterojunctions where n decreases with increasing temperature²³. Such an anomalous n value indicates that the current is not limited by drift nor by diffusion, but gives evidence of the presence of alternative transport mechanisms such as space charge limited current (SCLC). Indeed for the second bias region, we showed that the dominant transport mechanism was SCLC controlled by deep energy states. The breakdown voltage reached -160 V *i.e.* 1.6 MV/cm in the 50 nm intrinsic amorphous silicon layer. Such a thin amorphous silicon layer could be implemented in power switches in order to reduce the thick diamond layers usually implemented in Schottky diodes. The cycling of the devices with temperature showed a robust operation with no variation of the C–V as well as the J–V charac-

teristics demonstrating the potential of such structures in harsh environments. These results have been presented at the ICANS 24 in Nara - Japan August 2011 and subsequently published in the Journal of Non Crystalline Solids²⁴.

We kept collaborating with NIMS developing diamond based ultraviolet photodetectors²⁵. In addition, using the characterization platforms developed at GeePs, we were able to observe the leakage current in epitaxial diamond Schottky barrier devices by the correlation of conductive-probe atomic force microscopy and Raman imaging²⁶.

Since 2012, I progressively reduced my involvement in diamond research and joined a photovoltaic topic on the characterization of passivation for solar cells and transparent electrode. At the same time, I was granted by the Labex NanoSaclay funding to focus on the modulation of the electronic properties of graphene to devise heterojunctions. Through this grant I could set the GraPhIC platform (Graphene growth Interface and Characterization)* that aimed at sharing material, technology and characterization techniques to develop various research topics around graphene applications. This collaboration led by myself (GeePs) includes LPICM lab, LPN lab and the Atomic Energy Commission (CEA). In the following, I will describe these activities centered on the research projects I supervised and carried out by the PhD students I co-directed with Dr J-P Kleider (CNRS-GeePs) and Pr C-S Lai from Chang Gung University - Taiwan.

1.3 Silicon based heterojunctions and interfaces

PhD student : Ming Xu, thesis defended on April 8th 2016. Funding Chinese Scholarship Council.
Subject : "Photoluminescence techniques for the characterization of photovoltaic interfaces".

1.3.1 Modulated photoluminescence and carrier lifetime measurement

Ming Xu has utilized and developed modulated photoluminescence (MPL) techniques and extended its capabilities with the temperature control from 20 to 300 K. This system was applied to study photovoltaic heterostructures. The driving force to improve the efficiency of silicon heterojunction solar cells (SHJ) consists of adapting the cell structure to further reduce the interface recombination at the back surface. In that regard, we studied various combinations of passivation as well as doping within the framework of the European project HERCULES (High Efficiency Rear Contact solar cells and Ultra powerful moduLES) †. Few research on the temperature dependence of the electronic properties of a-Si:H/c-Si junction have been reported, Fig.1.3. In this range of temperature, we observed that the carrier lifetime of heterostructures passivated with doped interfaces exhibit peculiar temperature and injection level dependence. These experiments were supported by TCAD simulation in order to determine the dominant recombination mechanisms and the influence of shallow and/or deep defects²⁷. Particularly we discussed the lifetime extraction from simulations and introduced the concept of differential and steady state lifetime.

* Labex NanoSaclay † www.helmholtz-berlin.de/projects/hercules

The system developed is benchmarked to the quasi-steady-state photoconductance (QSSPC) and photoconductance decay that are widely accepted as the industrial standard.

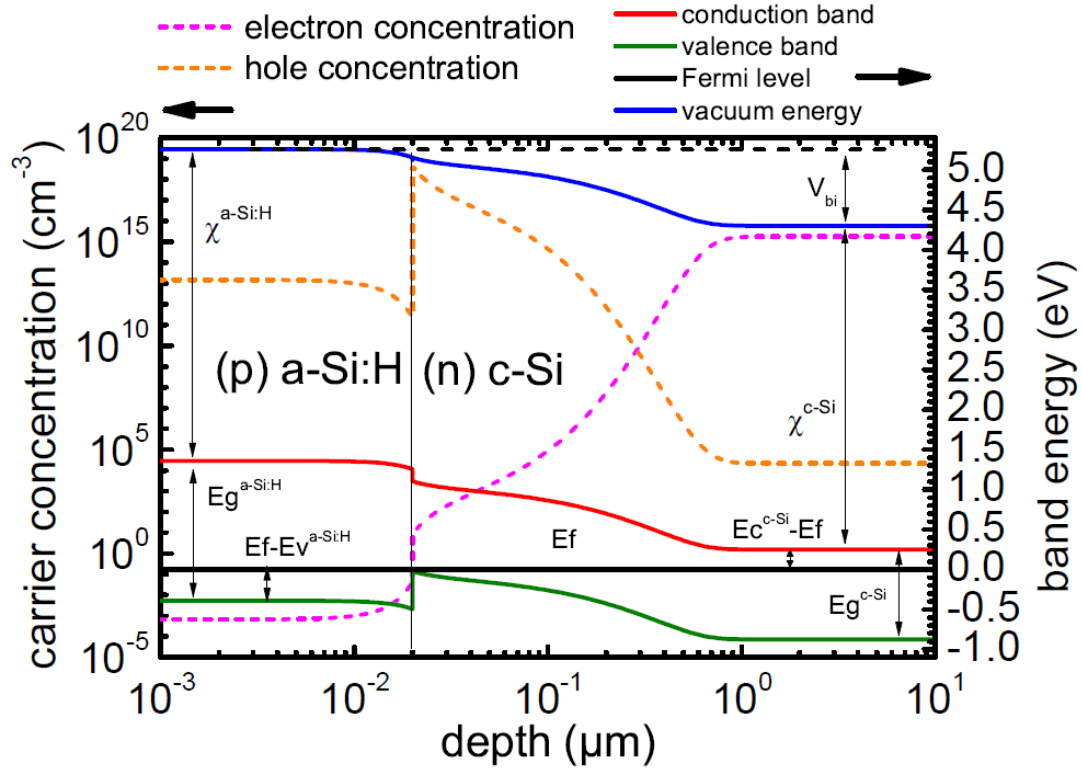


Fig. 1.3 Band diagram and carrier concentration of the simulated SHJ stack structure in thermal equilibrium

Amongst all the results achieved during his thesis the most striking one is the experimental determination of the temperature dependence of the band-to-band radiative coefficient $B(T)$, the data range (*to be published*) was extended from 77 K to 20 K. Radiative recombination is the origin of luminescence. Its rate is described as:

$$R_{rad} = Bnp \quad (1.1)$$

that yields the steady state radiative recombination lifetime defined as:

$$\tau_{ss,rad} = \frac{\Delta n}{R_{rad}} = \frac{\Delta n}{Bnp} \quad (1.2)$$

n and p are respectively the carrier concentrations for electrons and holes whereas Δn and Δp represent the excess carrier concentrations in c-Si. Assuming that $\Delta n = \Delta p$: The radiative recombination coefficient B is characterized as a function of temperature and data are available down to 90 K to date²⁸⁻³⁰. Coupling PL and MPL measurements, Ming Xu was able to extend the range of B as a function of T down to 20 K. First one needs to acquire the DC PL signal $V(T)$ over the whole spectrum. This signal is proportional to the integrated PL intensity $j(T)$ through

a calibration constant c_1 Eq.(1.3):

$$V(T) = c_1 j(T) \quad (1.3)$$

where $j(T)$ is proportional to the radiative recombination R_{rad} that is proportional to $B(T)$ through a constant c_2 Eq.(1.4). Therefore

$$j(T) = c_2 B(T) n(T) p(T) \quad (1.4)$$

Where $n(T)$ and $p(T)$ are determined from the measurement of the lifetime by MPL Eq.(1.2). whereas $n_0(T)$ is obtained considering the concentration of ionized dopants. As a result :

$$B(T) = \frac{V(T)}{n(T)p(T)c_1 c_2} \quad (1.5)$$

The constant c_1 and c_2 are evaluated using the temperature dependent B values given by Nguyen *et al.*³⁰ for $T > 90$ K. . Fig.1.4 displays the benchmark of our work with the data reported in the literature notably Nguyen's, Trupke's and Brüggemann's results, Eq.1.5. The $B(T)$ curves are in good agreement above 77 K. Note that there were no data available below 77 K in the literature

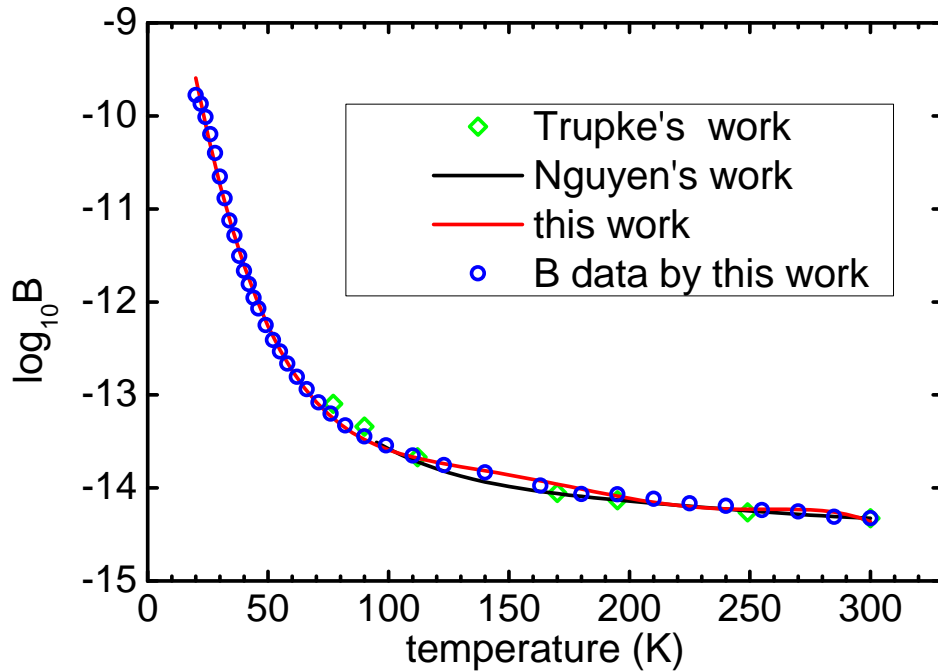


Fig. 1.4 Radiative recombination coefficient $\log_{10} B$ supercited from³⁰, Trupke's work²⁸, Brüggemann's work²⁹ and fitting from the experimental data in this work. The integrated PL is directly deduced from the experiments.

and our work contributed to extended the range of B available for the community down to 20 K.

1.3.2 Observation of the Excitation transfer in stacked quantum dot chains by micro PL - Collaboration with Chulalongkorn University - Thailand

In addition to silicon based heterojunctions, we have investigated the opportunity of using III-V quantum dots sequences for solar cell applications grown by molecular beam epitaxy. This work is a collaborative research between Pr S.Kanjanachuchai SDRL (Semiconductor Device Research Laboratory) of Chulalongkorn University (Thailand) and myself in the framework of ICT-ASIA programme. Here, We introduced the application of micro-PL mapping as a function of temperature under high injection in order to investigate the coupling between 1, 3, 5 layers of III-V InAs quantum dot separated by 10 nm GaAs. This structure is particularly interesting as it finds potential application in multijunction solar cells^{31,32}. Fig.1.5(a) comprises multiple stacks of InAs

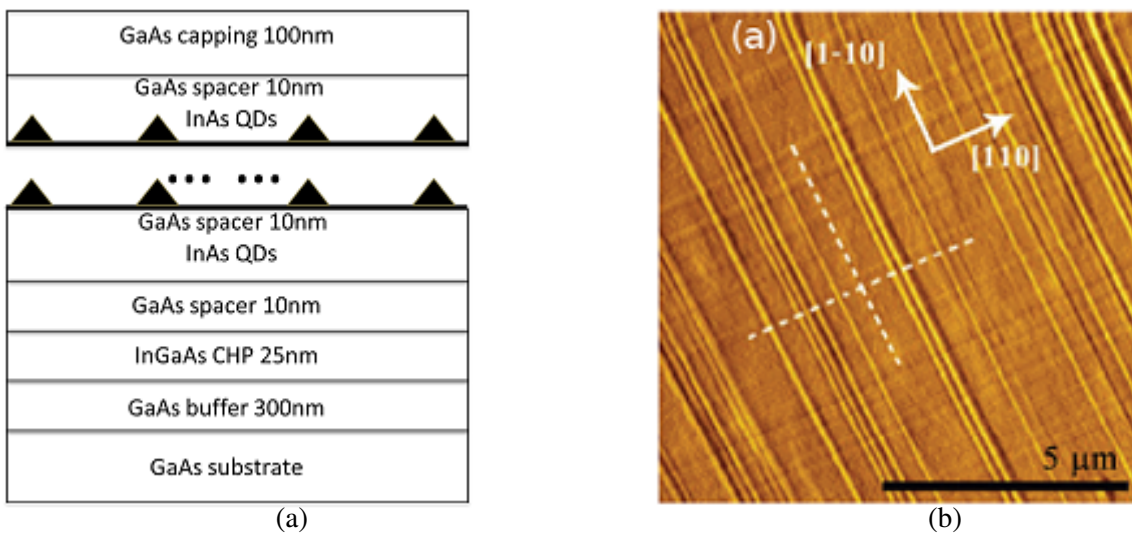


Fig. 1.5 (a) Schematic of investigated QDCs stacks structure (b) AFM image of $In_{0.2}Ga_{0.8}As$ on GaAs cross-hatch pattern (CHP) reproduced from^{31,32}

QDCs grown on partially-relaxed InGaAs film on GaAs by solid-source MBE Using Riber's 32P MBE system, and after in situ thermal cleaning of GaAs (001) surface, growth starts from 300 nm GaAs buffer layer, followed by 25 nm $In_{0.2}Ga_{0.8}As$, 10 nm GaAs spacer, and 1, 3, or 5 stacks of InAs QDC/10 nm GaAs spacer pairs. The cross-hatch pattern surface of the InGaAs layer serves as a template on which chains of QDs form along the orthogonal [110] and [1-10] directions,³³. Fig.1.5(b) displays $10 \times 10 \mu m^2$ AFM image showing the QDs geometry and distribution on the topmost layer. For 1-stack the QDs are aligned along [110] and [1-10] dislocation lines of the underlying CHP layer and some of them distribute randomly. Stacked InAs quantum dot chains (QDCs) on InGaAs/GaAs cross-hatch pattern (CHP) templates yield a rich emission spectrum with an unusual carrier transfer characteristic compared to conventional quantum dot (QD) stacks. The photoluminescent spectra of the controlled, single QDC layer comprise multiple peaks from the orthogonal QDCs, the free-standing QDs, the CHP, the wetting layers and the GaAs substrate.

When the QDC layers are stacked, employing a 10 nm GaAs spacer between adjacent QDC layers, the PL spectra are dominated by the top-most stack, indicating that the QDC layers are nominally uncoupled. Under high excitation power densities when the high-energy peaks of the top stack are saturated, however, low-energy PL peaks from the bottom stacks emerge as a result of carrier transfers across the GaAs spacers. These unique PL signatures contrast with the state-filling effects in conventional, coupled QD stacks and serve as a means to quickly assess the presence of electronic coupling in stacks of dissimilar-sized nanostructures,^{34–36} Fig. 1.6.

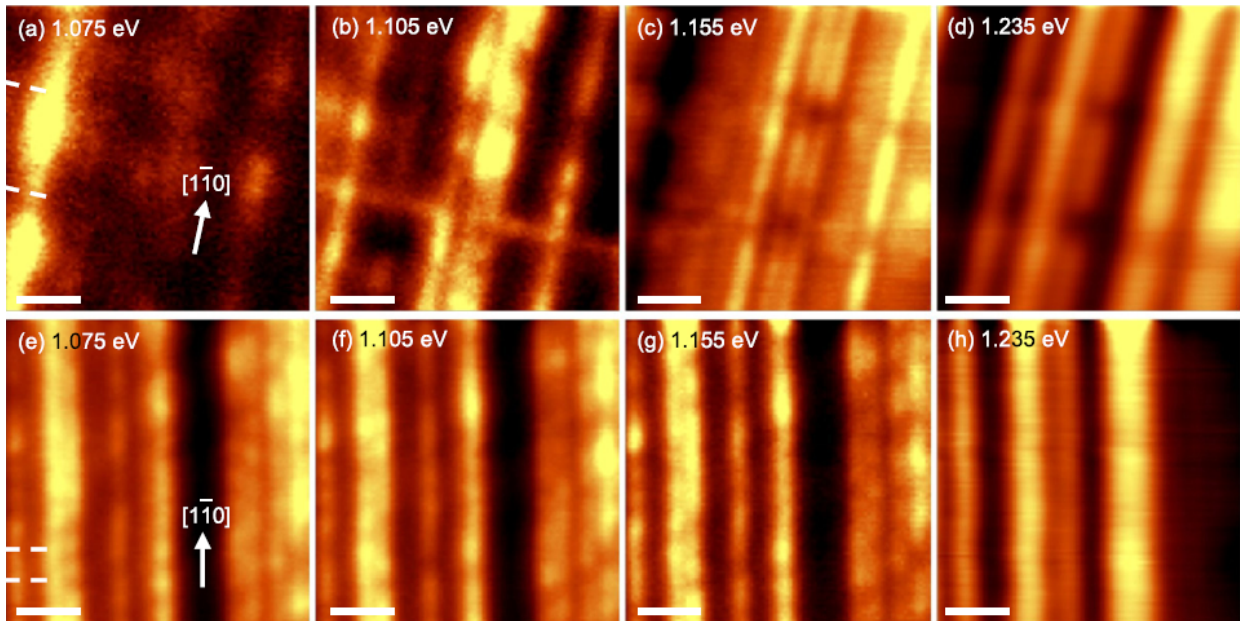


Fig. 1.6 Room-temperature, $10 \times 10 \mu\text{m}^2$ micro-PL mapping at 532 nm of (upper panels) the 3-stack QD chain sample at increasing integrated intensity from (a) 1.075 to (b) 1.105, (c) 1.155 and (d) 1.235 eV, and (lower panels) the 5-stack QD chain sample from (e) 1.075 to (f) 1.105, (g) 1.155 and (h) 1.235 eV. The scale bars are 2 μm . The broken lines are guide to the eye and indicate some of the buried [110] dislocation lines³⁶.

We are currently investigating the opportunity to use p-type graphene electrode on a sequence of QDs grown on n-type GaAs for the fabrication of III-V multijunction solar cell. In the following we demonstrate how to tailor the work function of graphene.

1.4 Modulation of the electronic properties of graphene

PhD student : Hakim Arezki, thesis defended on May 13th 2016. Funding University Paris Saclay. Subject : "Ingenierie des propriétés électroniques du graphene".

Hakim Arezki studied and characterized various samples of CVD and SiC graphene grown by our partners Pr Y.H Lee from Sungkyunkwan University (South Korea) and Dr A. Ouerghi from LPN-CNRS, respectively. His work was initially related to the project GraPhIC funded by the Labex NanoSaclay and Hakim Arezki collaborated with Fethullah Gunes post doctoral research associate recruited for this project. In this work, we were mainly interested in the modulation of the work function (WF) and the mobility through doping for transparent electrode and gate application

as well as FET channel. For that purpose we resorted to various experimental techniques such as Raman spectroscopy, photoemission X and UV as well as clean room lab for the nanofabrication of the test structures and devices. We have investigated different doping methods *in situ* and *ex situ*.

1.4.1 *In situ* nitrogen doping

In collaboration with Dr A. Ouerghi from Laboratory of Photonics and Nanostructures (LPN-CNRS), we first looked at the nitrogen incorporation in trilayer graphene. Here the nitrogen was incorporated during the cooling process after the growth of the SiC sample, Fig.1.7.

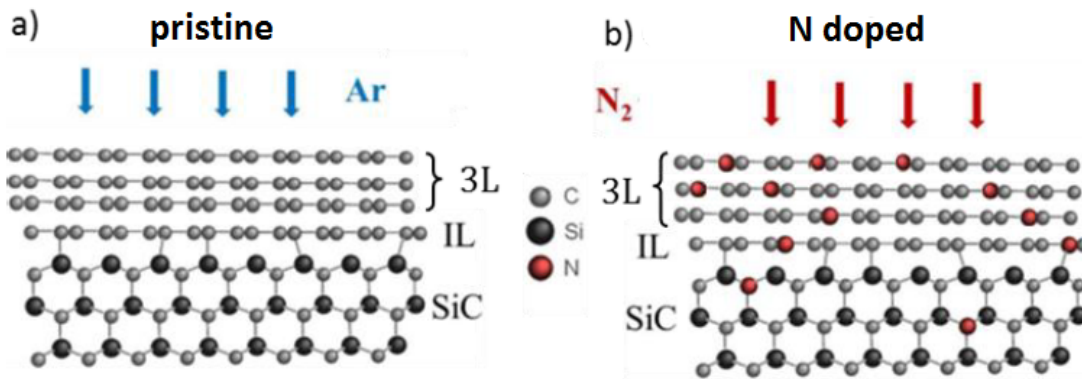


Fig. 1.7 Schematic of trilayer graphene grown on SiC (a) grown under argon flux and (b) cooled under nitrogen flux³⁷

Fig.1.8 presents AFM, TEM images, and micro-Raman spectroscopy, obtained on the N-doped trilayer graphene sample. Fig.1.8 (a) and (b) present the AFM images of the graphene grown on a SiC (0001) substrate. The AFM image shows a highly homogenous topography with a step density of 10–15 nm height and atomically flat terraces of about $7 \mu\text{m}$ wide on average³⁸ (Fig.1.8 (a)). In AFM phase images (Fig.1.8 (b)), at the step edges we observed the appearance of different regions, which corresponded to multilayer ribbons located at the very edge of the terrace^{39–41}. As observed from the STEM images (Fig.1.8 (c)), the N-doped graphene produced here, is predominantly composed by trilayer graphene. In the STEM image, the 3C-SiC lattice planes are straight, sharp, parallel to the surface, and equidistant. The interlayer separation is about $0.34 \pm 0.01 \text{ nm}$, and the graphitic layers are atomically flat and show a continuous film. In addition to acquiring AFM and STEM images, we characterized the graphene layer using Raman spectroscopy. In Fig.1.8 (d), typical spectra of pristine graphene and N doped graphene are shown, which correspond to measurements made on two locations of a terrace. The signatures of graphene are also observed as expected in the pristine and N-doped trilayer. They are identified by three main structures: (i) the D band, (ii) the G band, and (iii) the 2D band. For pristine graphene, the D peak is weak, indicating a low density of defects. In the case of N doped graphene, we note an increase of the D band and one more contribution due to the (D') bands at 1620 cm^{-1} , corresponding to the disorder-induced feature, which is known to occur in sp² carbon with defects. The high intensity of D band, as well as the presence of the D band, suggests that nitrogen breaks the local symmetry

of the graphene lattice. In addition, we note that the 2D peak reduces in intensity and the FWHM increases from 40 cm^{-1} to 70 cm^{-1} as typically observed in N-doped graphene⁴².

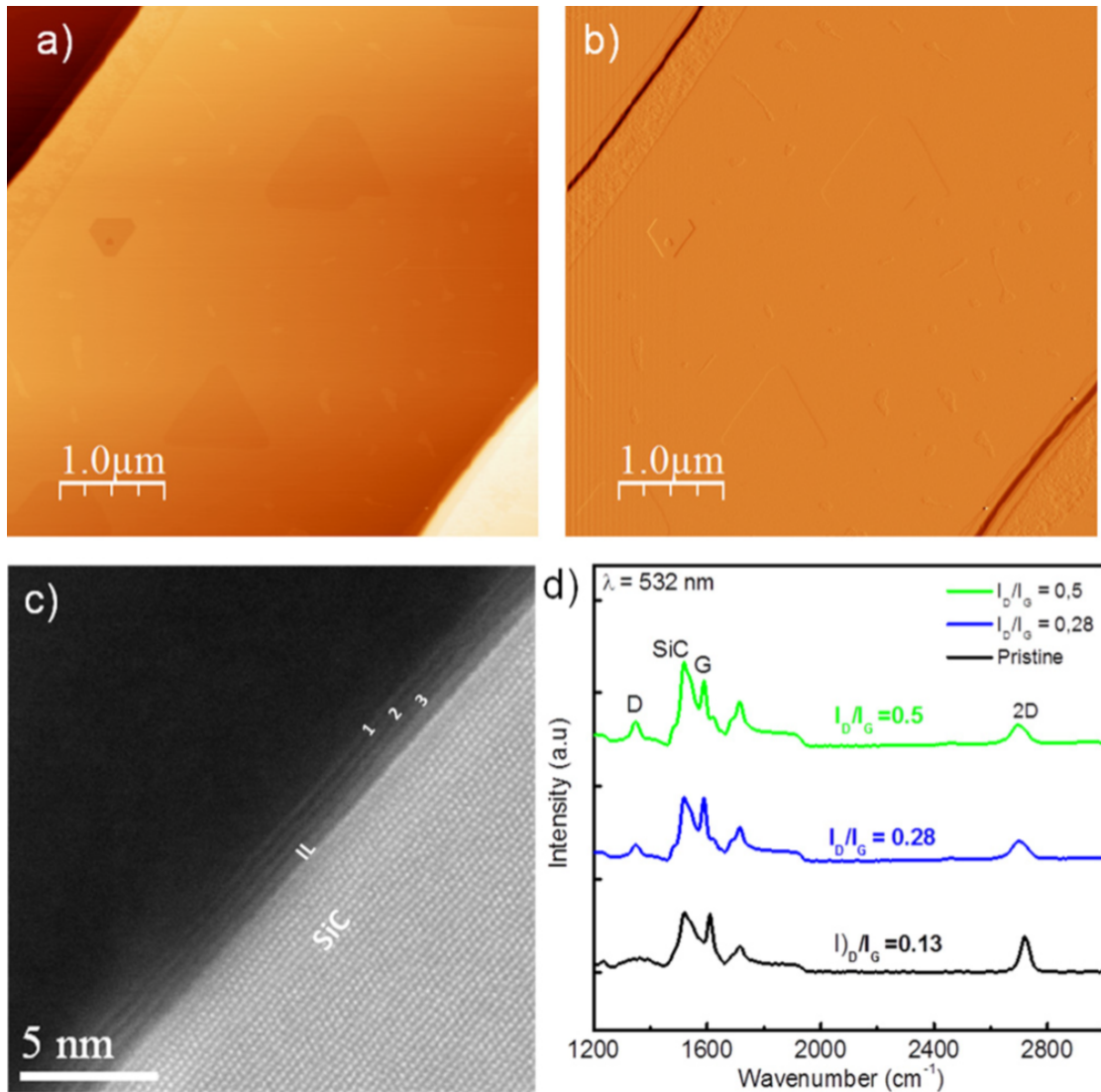


Fig. 1.8 (a) AFM topography of N-doped graphene sample. (b) AFM phase image of N-doped graphene. Graphene layer covers the entire substrate. (c) Cross-sectional High-resolution STEM image of N-doped graphene. (d) Comparison of Raman spectra taken for different I_D/I_G ratios on N-doped graphene and comparison to pristine sample.⁴³

In order to locate the nitrogen into the trilayer and measure the WF shift induced, we carried out XPS and UPS experiments. We probed the electronic properties of the samples using X-ray photoelectron spectroscopy (XPS) of nitrogen doped graphene layer (Fig. 1.9). Fig. 1.9 (a) displays the deconvoluted C 1s core level XPS spectrum of N doped graphene. The C 1s spectrum showed four components at 283.7, 284.6, 285.4, and 286.5 eV in binding energy. These components correspond to the SiC bulk (noted SiC), the graphene layer (noted G), the interface layer (noted IL), and the C-N bounds (C-N), respectively. The small new peaks at 286.5 eV suggest the bonding formation of doped nitrogen atoms to be sp²-C or sp³-C atoms. Fig. 1.9 (b) shows the Si 2p spectrum for an N-doped graphene sample. It is dominated by a peak at 101.1 eV corresponding

to the bulk silicon and presents a shoulder at higher energies. The shoulder is composed of a peak at 102.0 eV assigned to the IL between the graphene and the SiC (0001) substrate. Another peak at 100.7 eV is attributed to Si clusters of broken Si-C bonds formed during the graphitization process. Fig.1.9 (c) shows the deconvoluted N 1s of the N-doped graphene sample. This peak is decomposed in three components centered at 398.2 eV, 399.6 eV, and 401.4 eV assigned, respectively, to pyridinic, pyrrolic, and graphitic configurations, respectively, as shown in Fig.1.9 (d). It is admitted that graphitic-N is the most efficient doping configuration^{37,44}. In our context, pyrrolic and pyridinic-N appear to be the dominant bonding configurations. Interestingly, no Si-N-C bonds are visible³⁷. This observation indicates that the nitrogen is predominantly bonded in the graphene plane and edges and did not diffuse to the interface. This diffusion may have been prevented by the trilayer nature of the graphene in our sample.

We performed UPS analysis to determine the shift in work function induced by N atoms and verify the nature of the doping of graphene layers. As a reference, we utilized a sample of pristine monolayer graphene but without N-doping, the WF measured is 4.3 eV, similar values have been reported previously and trilayer undoped graphene is estimated to be 4.4 eV⁴⁵. We therefore conclude that the N doping process implemented in this work on trilayer epitaxial graphene has demonstrated its effectiveness to shift to a minimum of 0.3 eV, the WF from 4.4 eV to 4.1 eV confirming the n-type nature of the graphene layer. The mobility for holes and electrons is about $1300 \text{ cm}^2/Vs$ and $850 \text{ cm}^2/Vs$, respectively measured on a top gate device with Al_2O_3 gate oxide. The striking feature of this device is its carrier mobility that is nearly as high as pristine graphene obtained on Hall bars by Pallecchi *et al.*⁴⁶ in prior work but at 4 K and without any gate oxide. We conclude therefore that although oxygen may have hindered the nitrogen doping to an extent, limited scattering or traps centers have diffused at the interface and the carriers mobility estimated could have been even larger before the gate completion. In addition, no hysteresis was observed while sweeping V_g back and forth indicating that no trapping occurred at the Al_2O_3 /graphene interface. Note that current silicon high speed devices exhibit few $100 \text{ cm}^2/Vs$ and suffer from short channel effects. Yet, considering the low on/off ratios logic devices are unrealistic however there is potential for radiofrequency FETs as the cut off frequency FT increases with mobility, but one should consider parasitic resistances to properly assess the potential for such applications. On the other hand, nanoribbons patterned on N doped graphene with optimized gate dielectric could open the band gap required for logic applications⁴⁷. Such a scheme coupled to this atmospheric growth and doping method is a simple and cost effective approach to produce graphene based nanoelectronic devices.

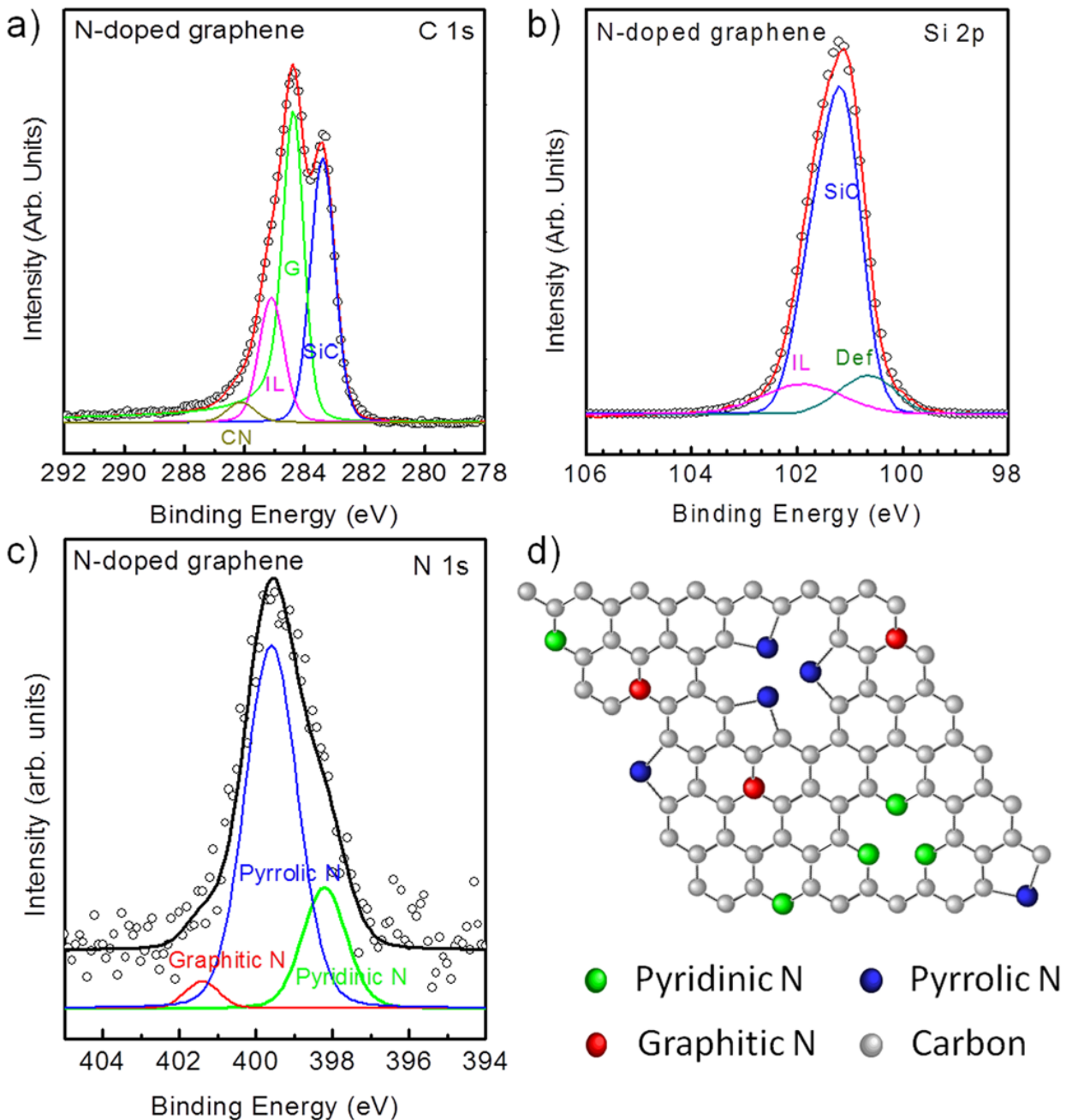


Fig. 1.9 (a) C 1s spectrum for N-doped graphene. The deconvolution using Doniach-Sunjjic line shape analysis shows the SiC, G, IL, and carbon nitrogen (CN) bonding configurations. (b) Si 2p XPS spectrum for N-doped graphene. (c) N 1s XPS spectrum for N-doped graphene showing 3 different nitrogen configurations. (d) The atomic configuration showing pyridinic-N, pyrrolic-N, and graphitic-N as well as graphene lattice and vacancies. XPS measurements were carried out at an angle of 45° with respect to the sample normal.

1.4.2 *Ex situ* doping by nitric acid

We have shown using in situ nitrogen doping that the WF could be modulated up to 0.3 eV. Here we have monitored the structural and electronic modifications of epitaxial graphene for different concentrations of diluted nitric acid (NA) 15 vol % (NA15), 30 vol % (NA30), 70 vol % (NA70) and 100 % (NA100) of nitric acid (NA) solutions in deionized water (DI water) for 2 min. The electro-

nic properties of the doped graphene samples were characterized by Raman spectroscopy and the work function shift after NA doping were measured using ultraviolet photoemission spectroscopy (UPS). To highlight the effect of nitric acid doping, these measurements were compared with the obtained values for pristine graphene. We demonstrated that the NA doping permits the WF modulation with respect to the dilution^{48,49}. Indeed, the WF first increases the electronic doping between 15 and 30 vol % (NA15, NA30) and then decreases the electronic doping between 70 and 100 vol % (NA70, NA100). This study on epitaxial graphene presents striking differences compared to the work of Das et al on CVD graphene where only p-type work function shifts are observed. We clearly demonstrate that both systems react differently to an identical chemical functionalization. Moreover, these observations are supported by density functional theory calculations (DFT)^{49,50}, Fig.1.10. We believe that the first HNO_3 molecules dissociate and saturate

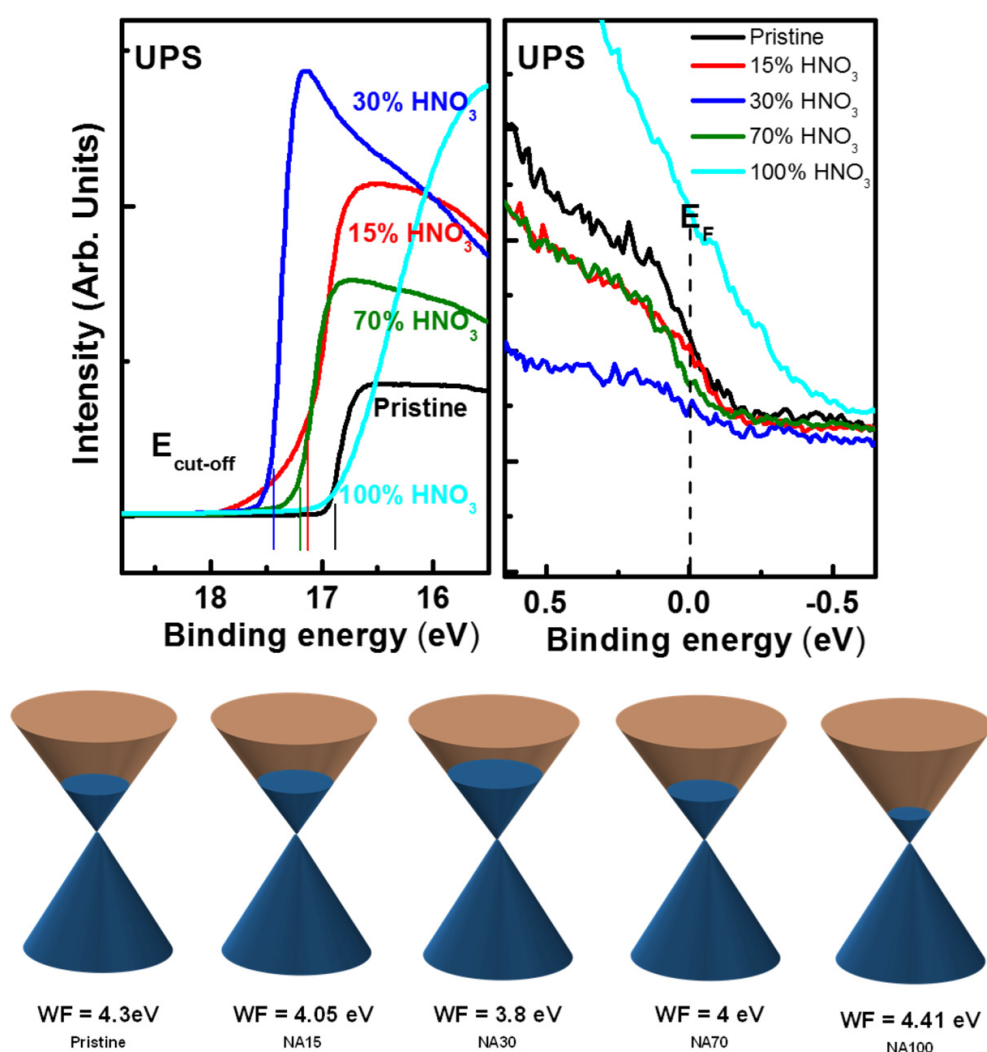


Fig. 1.10 (a) UPS data for pristine, NA30, NA70 and NA100 samples indicating the WF shift as a function of nitric acid concentration. (b) Illustration of the Fermi level shift in the graphene Dirac cones.

all available defect sites or step edges. This induces a nitrogen-doped graphene layer (NA15% and NA30%) and therefore decreases the WF. On the other hand, beyond NA30%, the HNO_3 molecules can physisorb on the surface inducing a p-type doping, lowering the Fermi level and as

a result increasing the WF.

To evaluate the electronic quality of our graphene layers, we determined the carrier mobility of the pristine and NA100% doped graphene using van der Pauw measurements at room temperature. Table 1 shows the electrical data measured for the pristine sample and NA100 extracted from Hall measurements. We have measured in previous works the electronic properties on such a monolayer graphene using the same growth mechanism. The lowest mobility achieved was $1400 \text{ cm}^2/\text{Vs}$ at 300 K. Note that Günes *et al.*⁵¹ achieved a sheet resistance of $100 \text{ } \Omega/\text{sq}$, using HNO_3 doping on CVD graphene. These data clearly indicate that although doping alters the lattice of graphene to some extent, it does not render the material electronically poor. The orders of magnitude are sufficient for many mainstream applications where contacts are required^{52–54}, Fig.1.11*.

	Sheet resistance (Ω/cm^2)	Carrier density (cm^{-2})	Mobility (cm^2/Vs)
Pristine	800	9×10^{12}	2500
NA100	500	6×10^{12}	1700

Fig. 1.11 Electrical data extracted from Hall effect measurements on pristine and NA100% sample at 300 K, majority carriers are holes.⁴⁹

1.4.3 CVD graphene/a-Si:H heterostructure

As we targeted to implement CVD graphene as a transparent electrode or a Schottky contact with crystalline silicon for solar cell applications⁵⁶, we studied the impact of amorphous silicon (a-Si:H) onto monolayer graphene. a-Si:H is utilized as a passivation layer in silicon heterojunctions solar cells⁵⁷. It prevents the surface recombination that is detrimental for the power conversion efficiency. To study the influence of a capping layer on the charge carrier transport in embedded graphene, 10nm of doped a-Si:H (n-type and p-type) were deposited onto the graphene by PECVD at $100 \text{ }^\circ\text{C}$. Raman spectroscopy measurements have shown a difference between n-type and p-type a-Si:H doped silicon capped graphene. As deposited a-Si:H onto CVD graphene present a high compressive strain as observed in Fig.1.12. Interestingly, the Raman features of the embedded graphene are preserved and this clearly demonstrates that little or no structural damages occurred during the deposition process. Indeed the G peak downshifted for both n-type and p-type a-Si:H compared to pristine that is a signature of strain⁵⁸. This red shift of both the G and 2D band is inherent to the elongation of the carbon-carbon bonds lowering their vibrational frequency. When n-type a-Si:H is capping the graphene, the shifts become -6 cm^{-1} and -1 cm^{-1} for both the G and 2D peaks respectively whereas they increase to -8 cm^{-1} and -13 cm^{-1} when p-type a-Si:H covers the graphene inducing more compressive strain. To elucidate a possible contribution of field effect doping, Hall bars were patterned for transport measurements as a function of temperature to

* This work has been highlighted in Nanotechnology perspective written by Dr Filippo Giannazzo⁵⁵

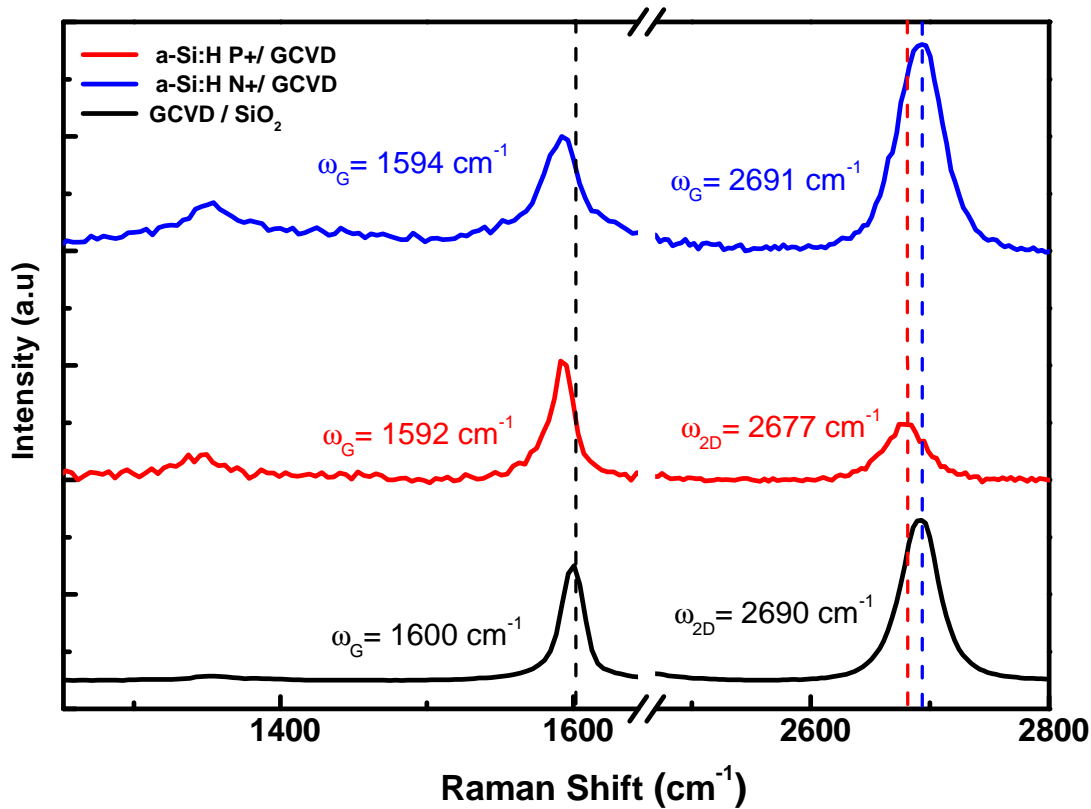


Fig. 1.12 Raman spectra of CVD graphene capped with 10 nm a-Si:H p and n doped.

evaluate the sheet resistance, charge carrier density and Hall mobility of the encapsulated film⁵⁹, Fig.1.13. We observe that whatever the capping type the electrical measurement are temperature independent, this is in sharp contrast with the observation of Gluba *et al.*⁶⁰ that observed the influence of scattering mechanisms for undoped capped graphene. In addition, we show that graphene capped with p-type a-Si:H undergoes a limited holes transfer increasing its charge carrier density without affecting its mobility ($\approx 1400 \text{ cm}^2/\text{Vs}$) compared to pristine on SiO_2 . Whereas the for n-type capping, the carrier density decreases and the mobility is reduced by more than a factor of 2 approximately with respect to graphene on SiO_2 ($\approx 600 \text{ cm}^2/\text{Vs}$ and Rs increased to 1300 ohm/sq). As the strain is more important for p-type capping than for n-type and the defect peak does not substantially increase, the strain is not responsible for this change in transport properties. As a result, we conclude that there must be a field effect doping due to impurities at the interface. At last, we demonstrated that a phase change of the as deposited a-Si:H under high laser power induces a Raman shift^{61–64}. The a-Si:H transforms into $\mu - c\text{Si}$ for both type of capping as it is visible by the appearance of a peak at 520 cm^{-1} , Fig.1.14. Both cappings exhibit up shifts for the G and 2D peaks upon crystallization inherent to the relaxation of the mechanical strain as well as a possible field effect doping as the intensity of the 2D peak diminishes as opposed to the G peak. We have demonstrated that the transport properties of capped graphene with a-Si:H remain interesting and the graphene is not damaged neither by the deposition process nor by the mechanical strain. This route may find application in embedded GFET channel to reduce the high

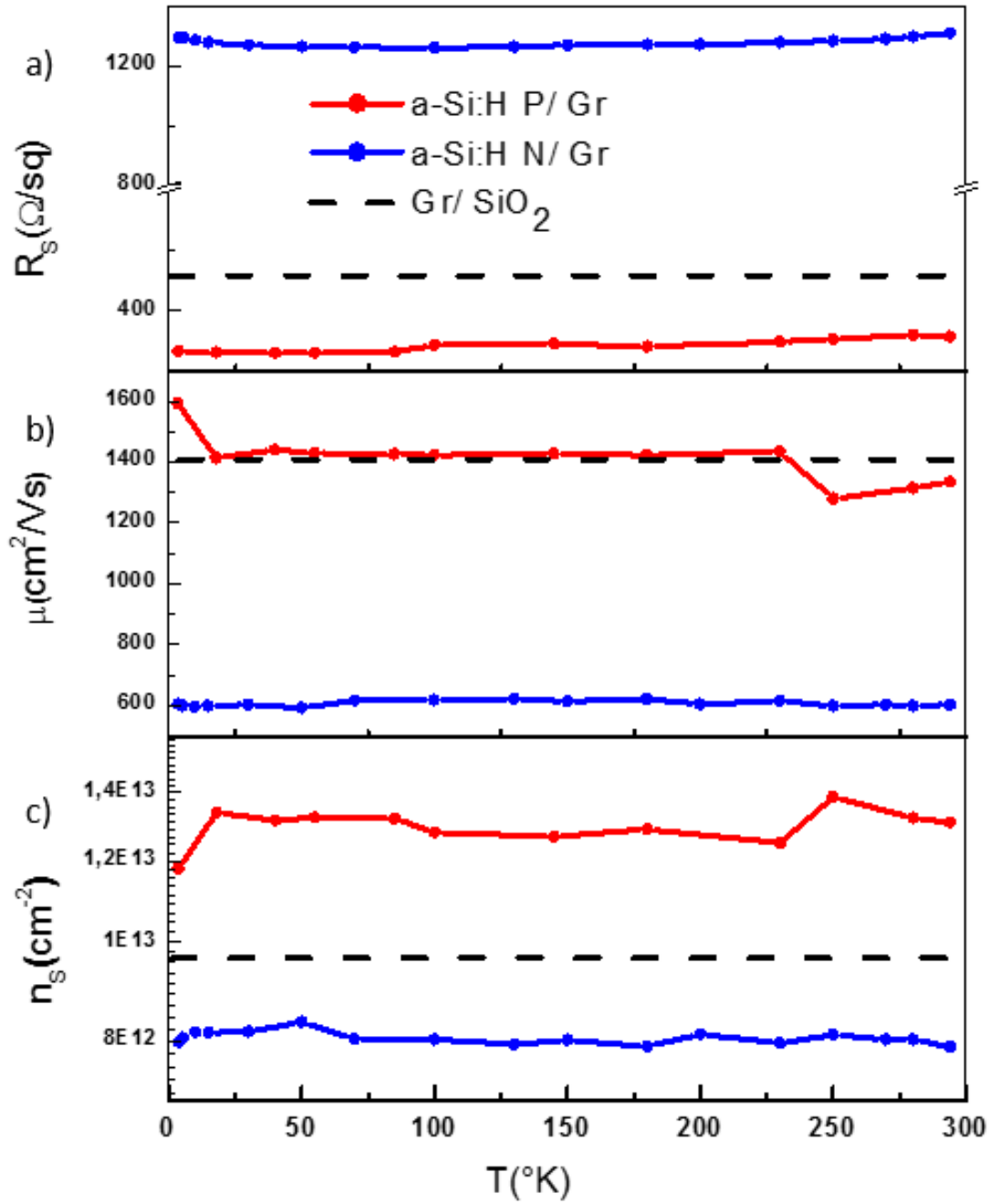
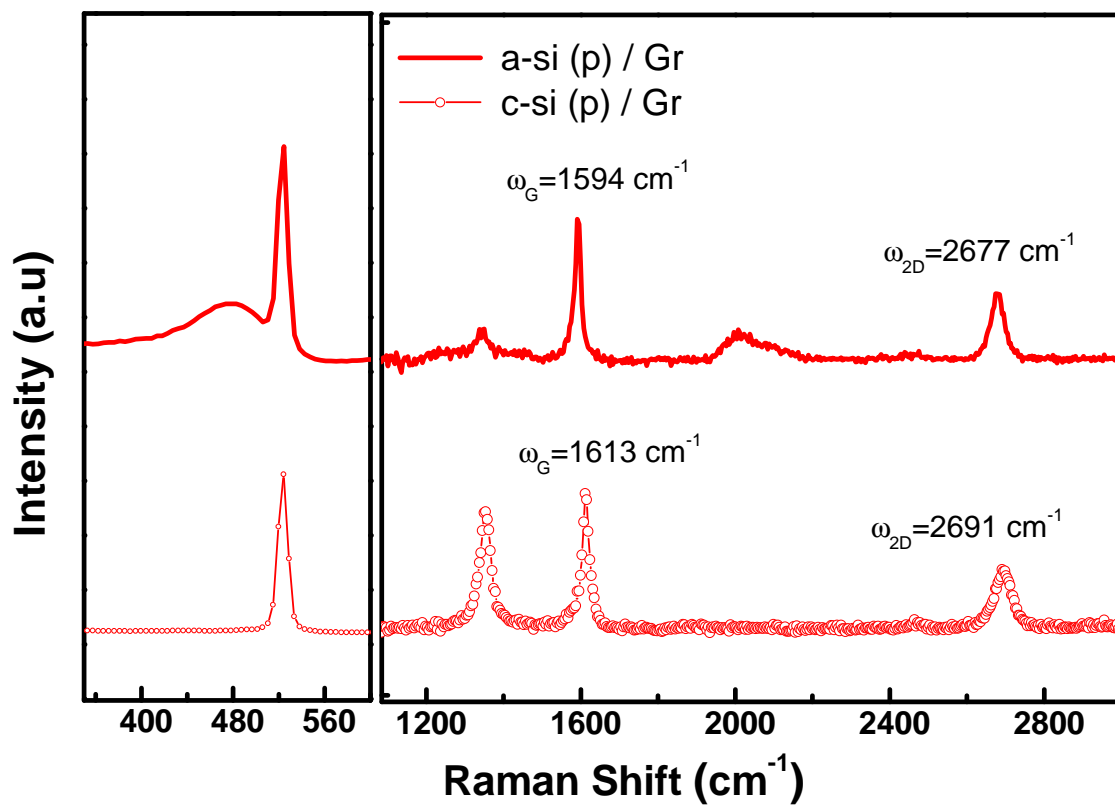


Fig. 1.13 Transport measurement versus temperature on CVD graphene capped with 10 nm a-Si:H : (a) sheet resistance, (b) mobility, (c) carrier density.

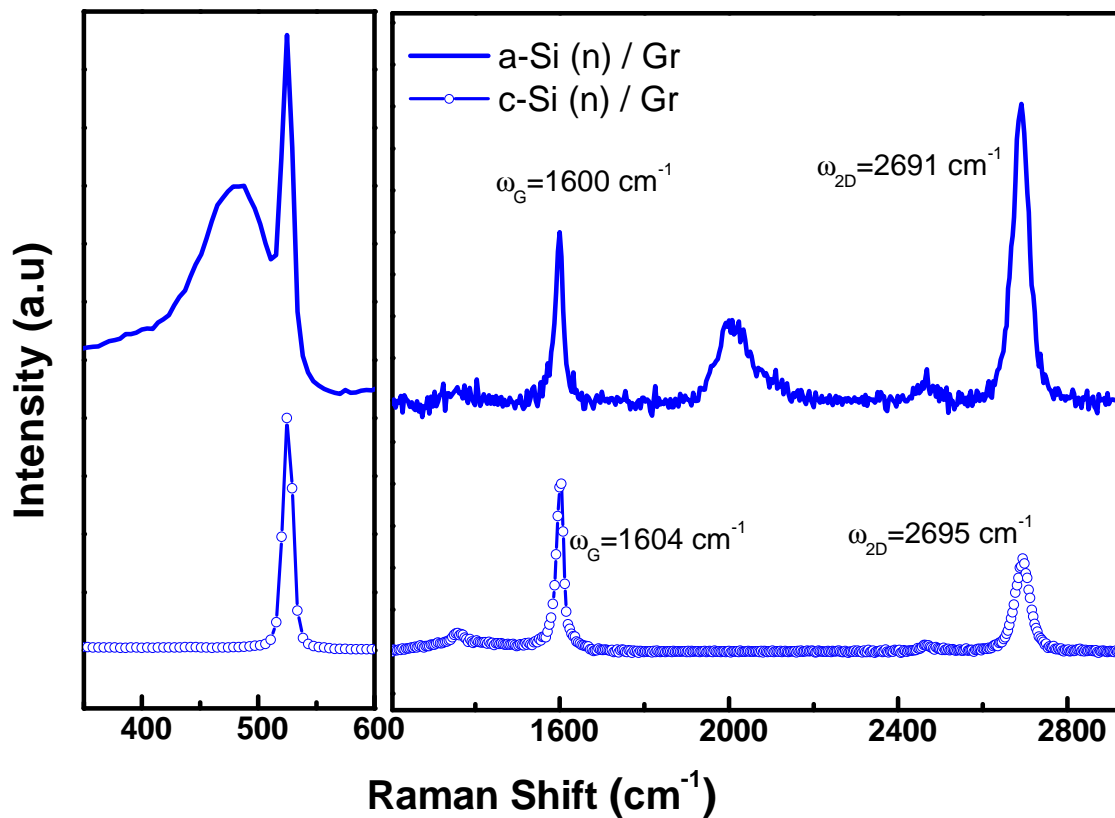
threshold voltage observed due to charge accumulation often due to contamination. The capping will prevent unintentional doping and tailor the Fermi level towards the charge neutrality point.

The ΔE_F can be evaluated with Eq.1.6⁶⁵.

$$E_F - E_{Dirac} = \frac{\hbar v_F}{e} \sqrt{\pi n_{Hall}} \quad (1.6)$$



(a)



(b)

Fig. 1.14 Raman spectra of CVD graphene capped with 10 nm a-Si:H before and after recrystallization of the a-Si:H. a) p-doped, b) n-doped

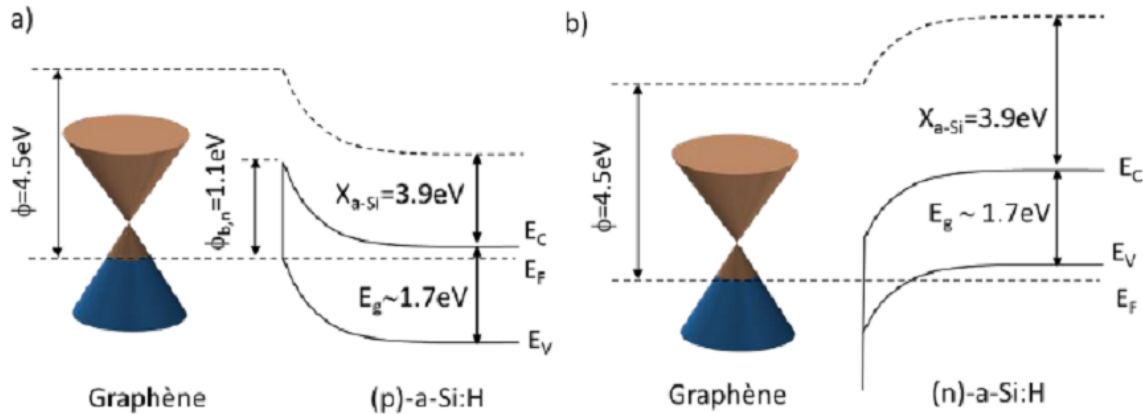


Fig. 1.15 Energy band diagrams of heterostructures graphene/a-Si:H n and p doped.

We estimate before crystallization a ΔE_F of 0.3 eV between the two capping type inherent to the charge transfer from the a-Si:H. However, this energy difference could also be inherent to metallic contamination such as $FeCl_3$. It has been recently demonstrated that such heterojunction could exhibit power conversion efficiency up to 14-15 %⁶⁶, Fig.1.15.

1.5 Graphene/fluorographene heterostructures

PhD student : Kuan-I Ho, thesis defended on January 12th 2016 with Pr CS Lai at Chang Gung University (CGU). Funding Ministry of Science and Technology (MOST) - Taiwan. Subject : "Study of Fluorinated graphene and its application for dielectrics and transistors".

Since 2013, within the framework of the ICT-ASIA programme*, I collaborate with Pr CS Lai of CGU on graphene based devices. The MOST has selected K-I Ho to carry out part of his PhD in France. In that context, he joined me from February 2015 to October 2015 to work on the integration of fluorographene (FG) as a passivation layer for FET device^{67,68}. This technology has strong potential for 2D based nanoelectronic devices^{69,70}. In this work, we presented a novel, fast, and efficient method to passivate silicon dioxide substrates (SiO_2) by forming FG on the substrate surface by CF_4 plasma treatment. We studied the FG as a function of the C/F ratio and we observed that the fluorination process renders the graphene more hydrophobic and transforms the sp^2 bonding configuration into sp^3 configuration. We implemented these observations into the fabrication process of a self-aligned transistor where the gate was deposited at the last step as opposed to standard processes. Our gate-terminated self-aligned transistor further improves the overall performance by limiting the series access resistances and achieves a high carrier mobility $\approx 3000 \text{ cm}^2/V.s$, comparable to typical chemical vapor deposition graphene (CVD-graphene) on high quality self assembly monolayers (SAMs) and on boron nitride (h-BN)^{71,72}, Fig.1.16. Several devices have been tested to extract statistics. V_{Dirac} errors bars on the different substrates are shown in Fig.1.16b, left axis. The V_{Dirac} of graphene on SiO_2 , $C_{18.4}F_1$ FG, $C_{3.4}F_1$ FG, and $C_{1.1}F_1$ FG are, respectively, 1.5, 2.5, 2.5, and 1.6 V. This trend indicates a p-type doping. We

* 2D Nanotech - grant 3226/DGM/ATT/RECH

observed that the leakage current is stable whatever the passivation and fivefold lower than the drain current indicating that the FGs do not present any leakage path. This is evidence of the insulating property of the FG layer. Surprisingly, the mobility improves as the V_{Dirac} increases with the fluorination, as opposed to usual trend observed elsewhere but in this work the FG acts as a passivation and is not the channel. Therefore one should consider the total electrostatic picture of the *graphene/FG/SiO₂* system, *i.e.*, *graphene/dipole/SiO₂*. In our study, both *SiO₂* and the graphene channel are identical for all samples and therefore should present the same charge impurities in *SiO₂*, and charged or dipolar functional groups on graphene because of unintentional atmospheric contamination. These C–O based functional groups are known to be holes donors; they alter the local electric field on the graphene channel and therefore its conductivity. The graphene sheet exhibits a given electrostatic potential. This picture is the same for all our samples. However, once the FG passivation is introduced the electrostatic potential is perturbed and the presence or absence of a dipole moment at the FG/graphene interface will affect the charge transfer occurring through the FG/graphene/adsorbates system. In that regard, it has been demonstrated that the fluorination coverage translates into different F bonding configuration^{73–75} with C and therefore different dipole moment, μ . For low F content, *e.g.*, C_4F , F bonds onto C preferably on one side, whereas for CF coverage, F covers all C atoms but on both side of the graphene sheet. For the later configuration that is close to our $C_{1.1}F_1$ FG, the opposite dipole moments cancel out. note that the C/F coverage is controlled by the fluorination time. Experimentally, we observed a ≈ 1 V increase in the V_{Dirac} voltage for both $C_{18.4}F_1$ FG, $C_{3.4}F_1$ FG. These two FGs as opposed to $C_{1.1}F_1$ FG present a dipole moment that facilitates the transfer of holes from the adsorbed contamination to the graphene sheet. This translates into a drop of the Fermi level (E_F) in the graphene and as a result in an increase of V_{Dirac} as observed experimentally. Fig.1.16 c illustrates the mechanism involved for the different dipole formation. On the other hand, the $C_{1.1}F_1$ FG passivation that does not exhibit a net dipole, then the V_{Dirac} is lower. Here, we believe that the absence of net dipole reduces the charge transfer from residual adsorbates and therefore little shift in the E_F is expected as compared to *SiO₂*. Indeed, no substantial variation of the V_{Dirac} is visible. The graphene (channel) is seen as decoupled from the *SiO₂* substrate through the $C_{1.1}F_1$ FG passivation hence the better mobility. Note that the devices with FG passivation exhibit a higher slope, narrower minimum conductivity plateaus, and higher value of the minimum conductivity. This trend relates to a reduction of the scattering mechanisms and clearly indicates that the samples with FG passivation exhibit a lower charged impurity density. As shown in Fig.1.16 b, right axis, the hole mobility of devices on FG is as high as three times enhanced for the lowest C/F ratio from $300\text{ cm}^2/Vs$ on *SiO₂* to $1000\text{ cm}^2/Vs$ on $C_{1.1}F_1$ FG. The peculiarity of the $C_{1.1}F_1$ FG, *i.e.*, C/F ≈ 1 is that all the fluorine atoms covalently bond to carbon atoms. We fabricated a gate-terminated self-aligned field effect transistor in order to reduce the access series resistances, Fig.1.17 shows the electrical characteristics of the self-aligned graphene-FET with the $C_{1.1}F_1$ FG passivation. The self-aligned process enhances the carrier mobility more than six folds from $\approx 300\text{ cm}^2/Vs$ on *SiO₂* to $1800\text{ cm}^2/Vs$ on *SiO₂* with self-aligned process. The introduction of the FG passivation further improves the mobility up to $\approx 3000\text{ cm}^2/Vs$. The FG passivation layer also induces a 50

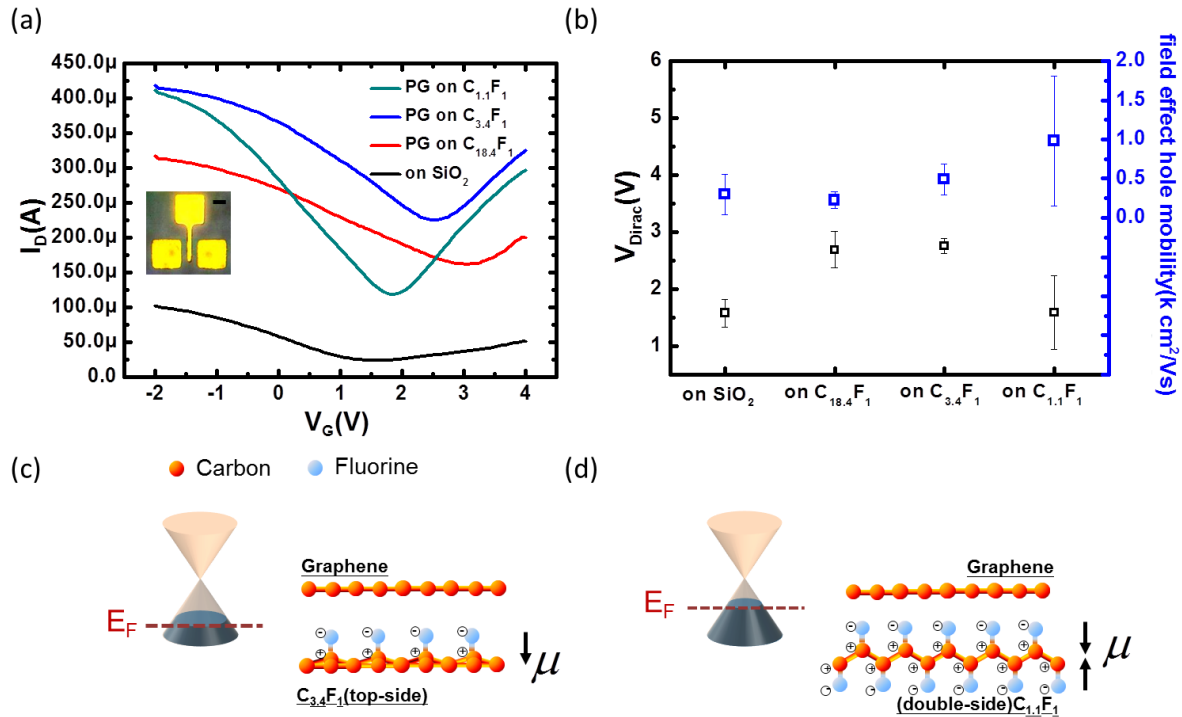


Fig. 1.16 a) $I_{DS}-V_{GS}$ characteristics of the top gate graphene-FET fabricated on FG substrate. The inset shows a photograph of the device under test. The scale bar in the inset is 50 μ m. b) Comparative plot of the V_{Dirac} voltages and hole field-effect mobility as a function of the fluorination. c) Illustration of the dipole formation for $C_{18.4}F_1$ FG and $C_{3.4}F_1$ FG. d) Dipole formation for $C_{1.1}F_1$ FG. The black arrow indicates the orientation of the dipole moment μ . The Dirac cones depicted show the variation of the Fermi level induced by the charge transfer⁷⁶.

% enhancement in the drain current and an on/off ratio increasing from ≈ 2.4 SiO_2 to 3 ($C_{1.1}F_1$ FG), Fig.1.17. We demonstrated that the FG passivation layer is a versatile and reliable option to improve the performance of graphene-based electronics*. In February 2016, in collaboration with Chang Gung University and the Laboratoire de Photonique et Nanostructures (LPN-CNRS), I filed a patent application on the integration of graphene/fluorographene nanoribbons FETs for memory applications⁷⁷.

* This work has been highlighted by the Labex NanoSaclay in July 2015

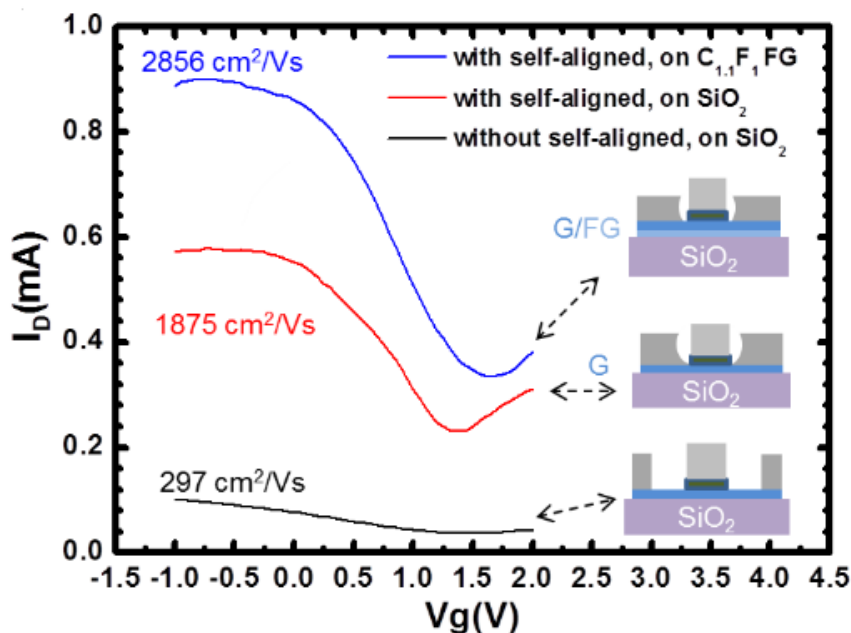


Fig. 1.17 $I_{DS} - V_{GS}$ characteristic of the devices fabricated with and/or without self-aligned design and 1 monolayer FG passivation^{ho_selfaligned_2015}.

1.6 International collaborative research

1.6.1 Toyohashi Tech - Japan - Graphene oxide

In 2012, I started a joint research on graphene oxide with Pr Adarsh Sandhu from the Electronics-Inspired Interdisciplinary Research Institute (EIIRIS) in Toyohashi University of Technology. In this work, graphene oxide was reduced into graphene through different chemical (hydrazine, ultraviolet photocatalysis) and biological (microorganisms) processes^{78,79}. We benchmarked the reduction efficiency of these methods by probing materials characteristics using X-ray photoelectron spectroscopy (XPS) analyses to observe the effectiveness of the reduction processes through the sp²/sp³ content. In addition, the homogeneity of the reduction was investigated on micrometer scale sample with micro Raman mapping as well as conductive-probe atomic force microscopy (CP-AFM) to investigate the longitudinal conductivity of the different samples. The results showed that hydrazine based reduction remains the most efficient. However, the bacterial procedure demonstrated partial reconstruction of the carbon network and reduced the amount of oxygenated functional groups⁸⁰. This work led to the signature of a Memorandum of Understanding between EIIRIS and UPMC.

1.6.2 Characterization of CVD graphene superlattices

Bilayer graphene (BG) has attracted attention thanks to its unique electronic structure, which can be modified by the stacking orders⁸¹⁻⁸⁴. A tunable bandgap can be opened by applying vertical electric fields which break the layer symmetry with potential applications in photonics and electronics⁸⁵. The CVD samples studies in this work were provided by Pr Y.Hee Lee group at

Sungkyunkwan University South Korea. These samples presented peculiar flower-shaped structures composed of bi and trilayer that exhibit random twist angles^{86,87}. These peculiar structures could be interesting for graphene dot application or as a floating gate for nonvolatile memory. During our studies on CVD graphene, we noticed the presence of multilayer defects across the

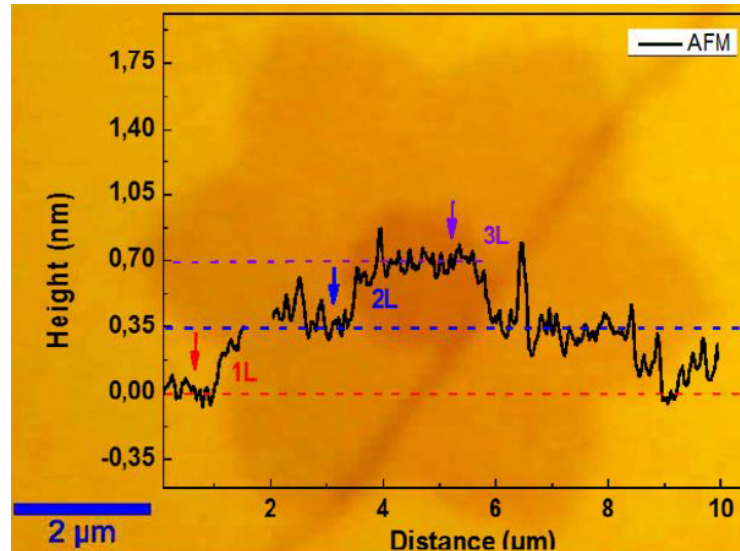


Fig. 1.18 AFM profile superposed to the optical image of 1L, 2L, 3L defect in CVD graphene.

samples, Fig.1.18. These superlattices are composed essentially of bi and trilayer, Fig.1.19. We observed by TEM analysis and Raman that the twist angle is different for various structures within the same sample, Fig.1.20. Since the electronic properties in graphene are dependent on the number of layer and stacking orientation, we decided to probe these features on our samples by Raman spectroscopy, and nano - Angle Resolved Photoemission Electron Spectroscopy (ARPES) at synchrotron Soleil.

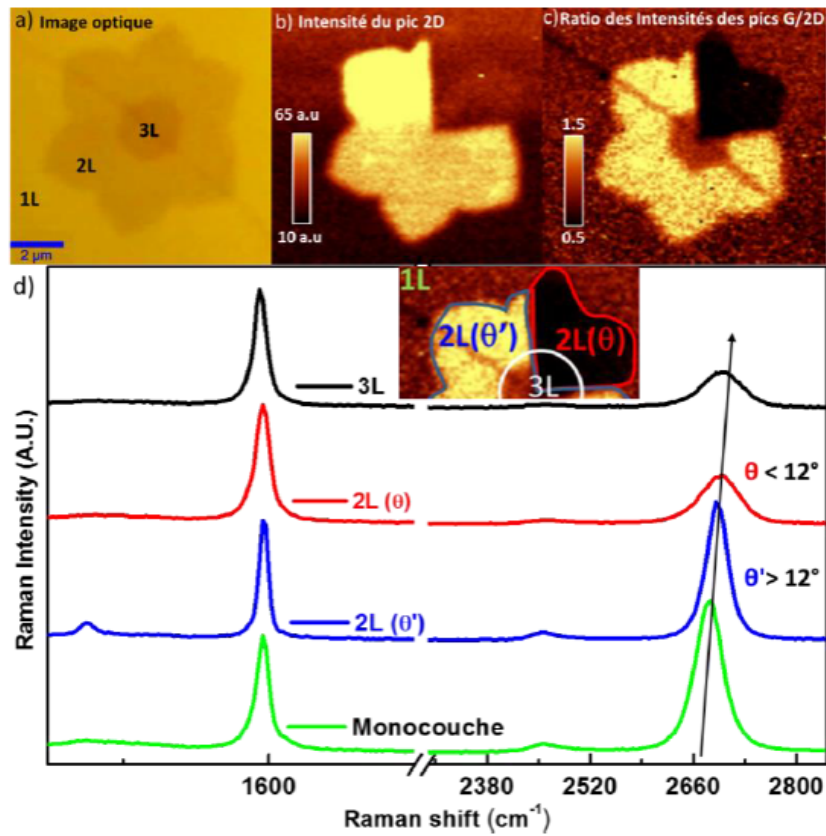


Fig. 1.19 (a) optical image of trilayer graphene superlattices, (b) Raman mapping of the 2D band, (c) Raman mapping of the G/2D ratio, (d) Raman spectra for different twist angles.

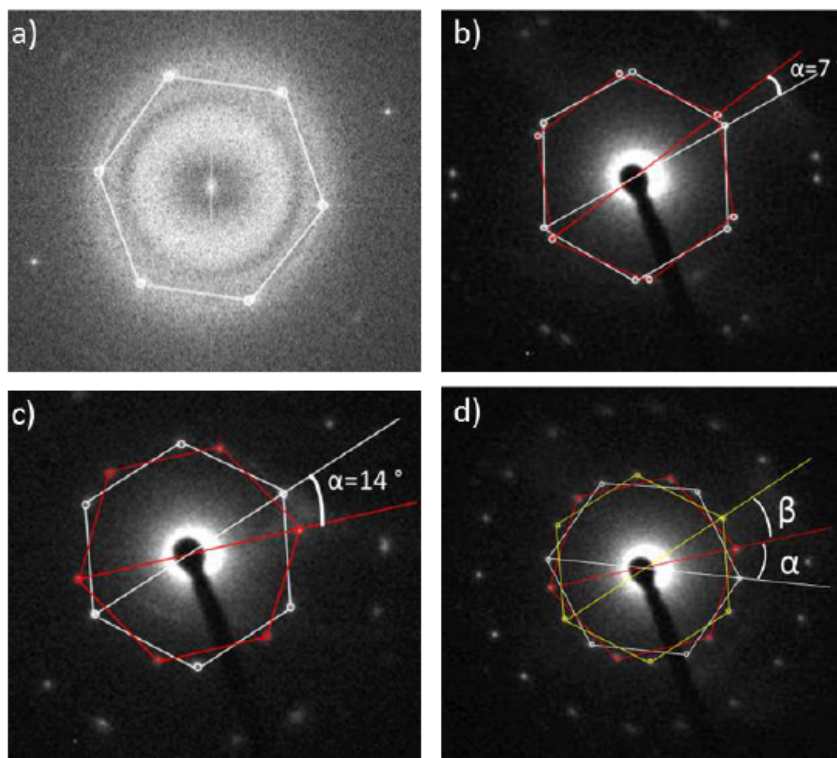


Fig. 1.20 (a) Fourier transform HR-TEM of 1ML CVD graphene.(b,c,d) diffraction of bi and tri-layer CVD graphene exhibiting various twist angles.

1.6.3 Synchrotron Soleil collaborative research - nanoARPES

In the continuity of the GraPhIC project, GeePS and ANTARES beamline have initiated a collaboration to investigate various combination of material at synchrotron Soleil under proposal 20140653 entitled Chemical nano-imaging and detection of density of states close to the Fermi level on multilayers graphene islands and heterojunction. In particular, I was interested in probing the band structure directly onto the aforementioned superlattices^{88,89}. Our collaboration is

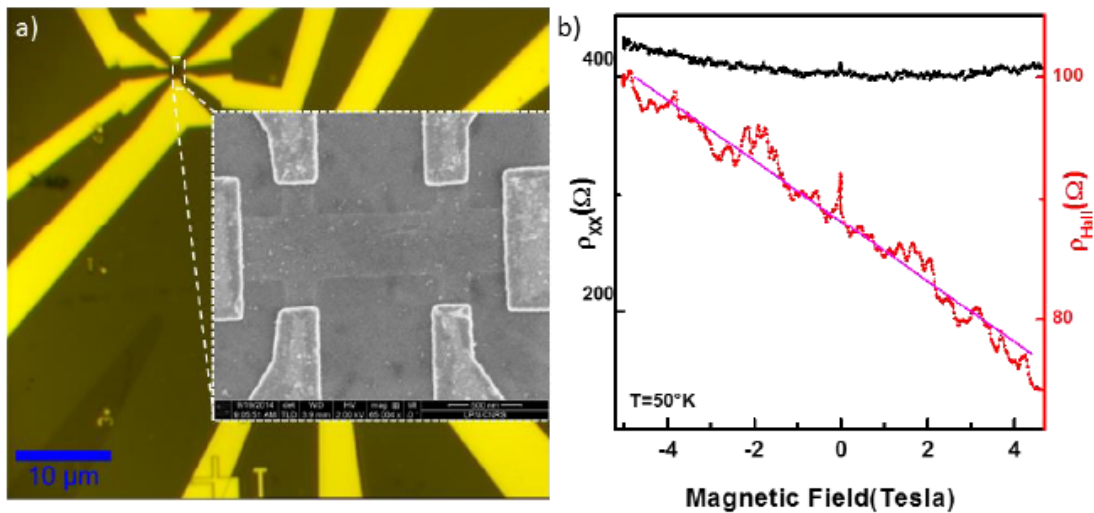


Fig. 1.21 (a) Optical and SEM picture of a Hall bar patterned onto a twisted bilayer graphene, (b) ρ_{xx} and ρ_{xy} as a function of the magnetic field.

on-going with a focus on heterojunctions. Notably, I am particularly interested in probing the charges trapped at an interface after injection through a tunnel barrier.

1.6.4 Tokyo Institute of Technology - Japan - Spatio-temporal observation of photogenerated electron dynamics in graphene superlattices

In the last decade, graphene has been one of the most studied 2D materials. Quasi-standing mono and multilayer graphene has attracted attention for a range of optoelectronic applications. The modulation of graphene's properties for devices applications relies on the understanding of the carrier interactions and recombination dynamics^{95,96}. Indeed, stacked monolayer graphene, demonstrates tunable band structures that depends on the stacking orders, *i.e.* the rotation angles between two layers. Therefore, understanding the ultrafast kinetics and their correlation with the number of layers as well as the stacking configuration is of particular interest. However, the ultrafast carrier dynamics influenced by the crystallographic structures is not well understood, because of the instrumental limitations. Here we utilize a different technique coupling an optical pump-probe technique using femtosecond laser pulses and a photoemission electron microscopy with the spatial resolution of 100 nm (time-resolved photoemission electron microscopy^{97,98}: fs-PEEM), Fig. 1.22. On one hand the *fs* timescale helps to investigate the faster relaxation mechanisms, and on the other hand the simultaneous microscopic observation probes any particular region that may exhibit a

given rotation angle. These relaxation mechanisms have been extensively studied in high quality exfoliated and SiC graphene using pump probe techniques⁹⁹. For our superlattices, we estimated the photogenerated carrier lifetimes in selected regions has been estimated by time-resolved photoemission electron microscopy with 100 nm spatial and 100 fs temporal resolutions.

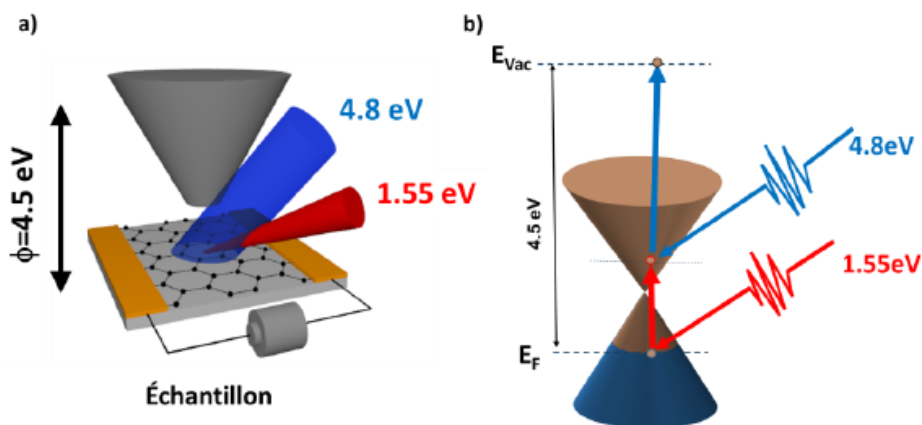


Fig. 1.22 (a) Illustration of the sample investigated in the PEEM system, (b) pump laser at 4.8 eV excites electrons from the valence band to the conduction band of the graphene the relaxation is probed at 1.55 eV.

Our spatial resolution permits to acquire in one shot the photoemission of all these superlattices. A subsequent analysis performed on the pixelized image allows the extraction of the lifetime of the carrier within a particular region. As a result, we are able to produce a map of lifetime across a large scale graphene sample and establish the superlattices which have a stronger interaction with the underlying substrate and other which seem decoupled from the substrate. Fig. 1.23 a shows a the Raman microscopy image of the 2D peak over the G peak to enhance the structural information. The bilayered regions correspond to a rotation angle of $> 12^\circ$, 12° and $< 12^\circ$, respectively. These angles have been determined from the Raman signatures.

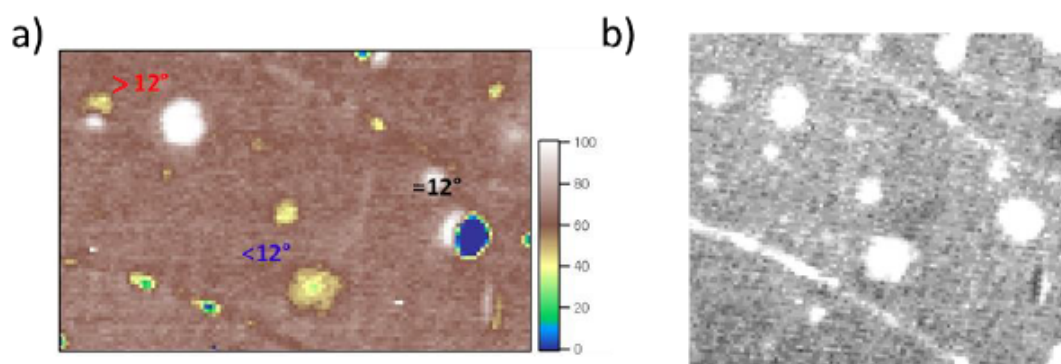


Fig. 1.23 (a) Raman mapping of G/2D bands of different superlattices with twist angle : $< 12^\circ$, $= 12^\circ$ and $> 12^\circ$, (b) PEEM intensity image corresponding to the same regions.

Fig. 1.24(a) provides a PEEM image obtained at the same region to Fig. 1.24(b) in addition to monolayer region, Fig. 1.24. Slightly darker contrasts in the three regions indicate the higher work-

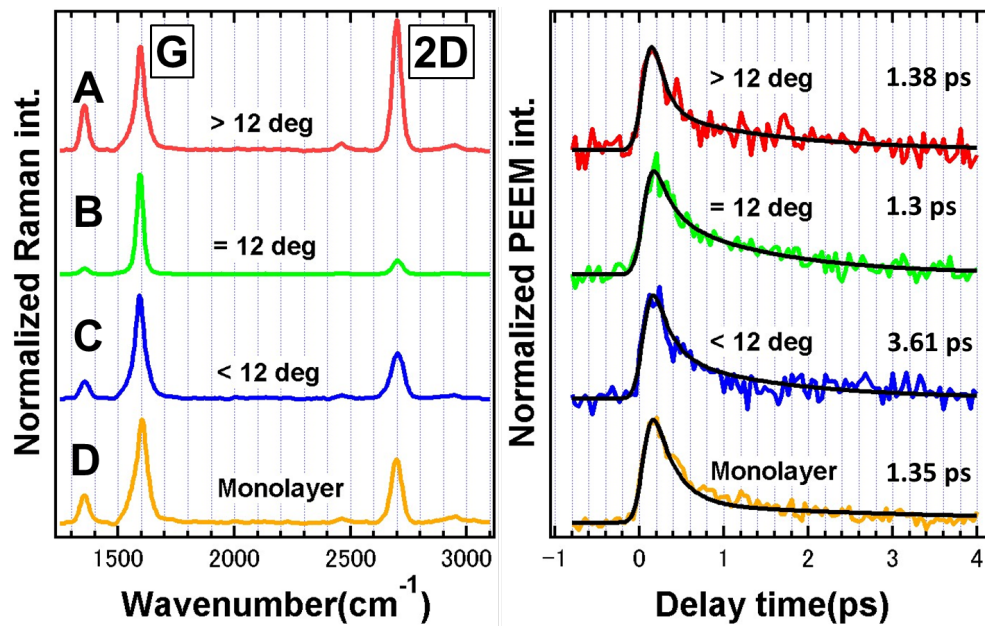


Fig. 1.24 (a) Raman spectra of different superlattices with twist angle : $< 12^\circ$, $= 12^\circ$ and $> 12^\circ$, (b) PEEM intensity profile as a function of time for the 3 superlattices.

functions inherent to the different stacking orders. From the PEEM intensity, we can determine the lifetime of the photogenerated carrier for each angle, Fig.1.24. Different stacking orientation give rise to a different band structure and therefore we expect a different recombination lifetime for each region. Clearly, we observe a difference between the monolayer that is directly onto silicon dioxide and suffers from phonon interaction as opposed to the bilayer superlattices. These latest appear to be decoupled from the substrate and longer lifetime are observed. The PEEM system presented here is able to precisely mapping in space and with *fs* time resolution the lifetime of photogenerated carrier in complex nanostructured materials. We are currently accumulating more data on these samples and extended our study to topological insulators (submitted to Carbon).

1.6.5 Chang Gung University - Taiwan

1.6.5.1 Graphene nanodiscs nonvolatile memory

Since 2013 in the framework of the ICT-ASIA project , I collaborate with Pr CS Lai in Chang Gung University (Taiwan). He has been engaged in the research of the characterization and reliability of MOSFETs, flash memory, high-k dielectrics and biosensors. In that context, we worked on SiC and CVD graphene FET device for memory applications^{43,76,77} . With regard to graphene, its large scale synthesis by chemical vapour deposition (CVD) and its transfer process onto functional substrates have opened new opportunities for device integration. However, the growth as well as the transfer of the material inherently generate structural and electrical defects. Although defects are usually detrimental for most of the devices operation, it is possible to exploit them as a trapping centres *i.e.* charge storage nodes for the fabrication of atomically thin films non-volatile memories (NVMs)^{100–103} , Fig.1.25. In this work, we have integrated graphene nano discs (GNDs ≈ 20 nm)

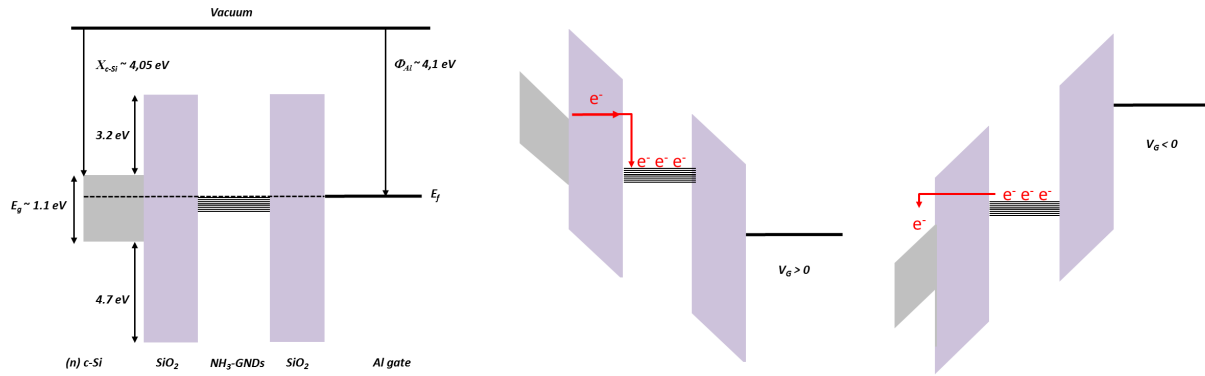


Fig. 1.25 a) illustration of the energy band diagram at the flat band. a) programme operation, the electron tunnel through the 3 nm SiO₂ barrier. This results in a Fermi level located in the conduction band. c) erase operation, the electrons tunnel back and the Fermi level move down into the valence band.

as charge trapping nodes for non-volatile memory (submitted to Carbon). The fabrication process relies on the patterning of Au nanoparticles (Au-NPs) which thicknesses are tuned to adjust the GNDs diameters upon etching. A density of GNDs as high as $8 \times 10^{11} \text{ cm}^{-2}$ is achieved. The functionalization of the GNDs by NH_3 plasma introduces defects sites and $\text{N} - \text{H}^+$ and $\text{N} - \text{H}_2^+$ functional groups as observed by Raman and FTIR spectroscopies. This inherently enhances the density of the trapping centers in and around the GNDs. As a result, the memory window reaches more than 2.4 V and remains stable after 10^4 operating cycles. The charge loss is less than 10 % 10-year data retention rendering this simple back end process suitable for low cost nonvolatile memory*, Fig.1.26.

* Integration of functionalized graphene nano-discs as trapping centers for nonvolatile memory submitted

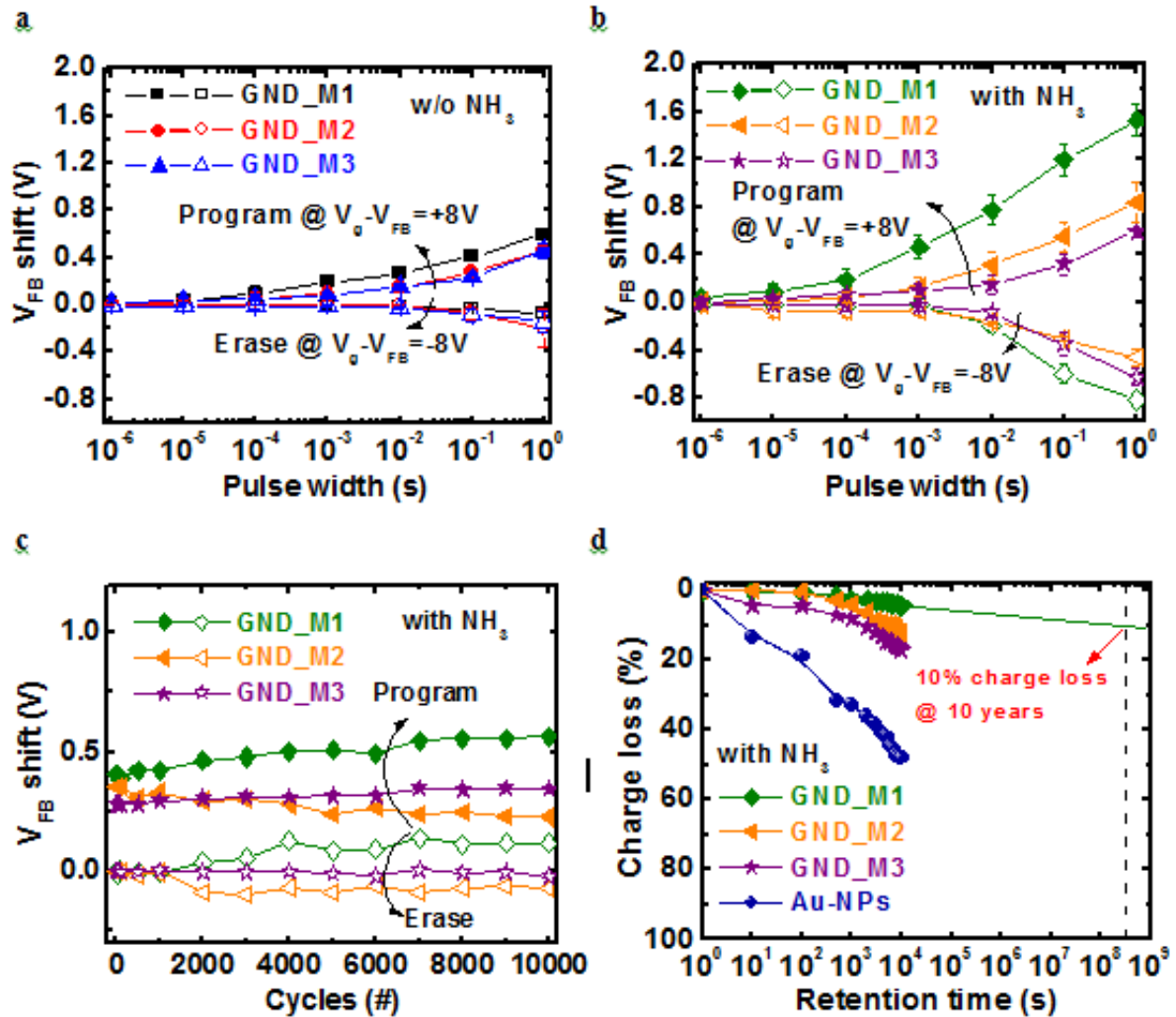


Fig. 1.26 GND nonvolatile memory characteristics. (a) P/E characteristics without NH_3 functionalization. The gate voltage (calibrated by initial V_{FB}) is 8 V for programming and -8 V for erasing, with 10^{-6} s to 1 s pulse width. (b) P/E characteristics after NH_3 functionalization. The memory window significantly enhances. (c) The endurance characteristics of the NH_3 GND-NVM. The samples can sustain more than 10^4 cycles with ± 8 V for P/E operation. (d) Extrapolated data retention characteristics of the GND-NVM. Less than 10 % charge loss after 10-year is expected.

1.6.5.2 Multilayer graphene nanoribbons

We already mentioned in section 2.5 our work on fluorographene and its potential as a passivation layer. In this collaboration, we present a novel graphene nanoribbon (GNR) transistor fabricated by the partial fluorination of the channel. This fully back end process permit the design and the fabrication of FinFet like GNR, Fig.1.27.

Our heterostructure consists of directly embedding the tunnel dielectric within the multilayer graphene *i.e.* partial transformation of the graphene by fluorinated plasma instead of growth or deposition process. Our first attempt showed that the ambipolar behaviour on GNR can be achieved with such process with a reasonably low gate nA leakage current, Fig.1.28. Interestingly, a few

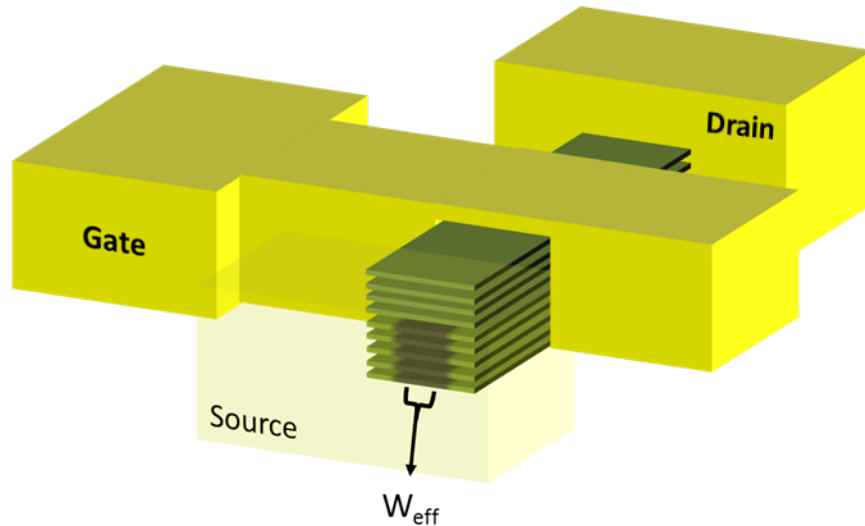


Fig. 1.27 Illustration of a FinFET like transistor fabricated using multilayer graphene grown on SiC, the fluorination process renders the channel embedded into a fluorographene dielectric.

devices showed a 10^4 *on/off* ratio at room temperature (defined as the highest on current over the charge neutrality point current). The off state current is limited by the thermionic emission that readily occurs at room temperature. Indeed, the off state current reduces with the temperature as can be seen at 200 K already. This leakage path can be limited using appropriate source and drain contact or by tuning the work function of the multilayer graphene channel in order to increase the barrier at the interface between the GNR and the metallic contact to a few kT suppressing the thermionic emission. We are working on the optimization of such device for memory application. This will be further discussed in section Perspectives.

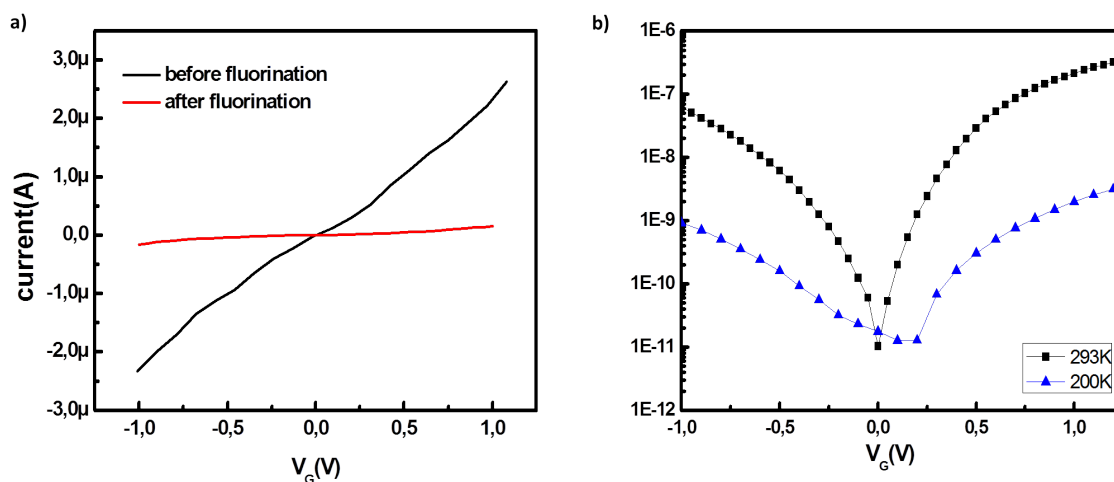


Fig. 1.28 a) current - voltage characteristics of the fluorinated multilayer graphene channel before and after fluorination showing the effective reduction of the channel width; b) I-V characteristics of Gr/GF FETs showing high on/off ratio at room temperature. The leakage current due to thermionic emission reduces with temperature.

Chapter 2

Prospective research topics

2.1 Foreword

During the last decade two dimensional (2D) crystals have emerged as a new class of materials. Graphene is probably the most famous example, but material scientists have unveiled numerous alternatives with outstanding electronic and structural properties. As the physics of these materials is being captured, researchers endeavour to integrate 2D materials and/or topological insulators (TI) to realize the strong potential these materials offer for a wide spectrum of applications *e.g.* photovoltaic (PV), nanoelectronic devices, optoelectronic devices, sensors. In that regard, based on my research background acquired on the characterization and integration of graphene into devices, I wish to pursue this activity with a focus on low power nanoelectronic devices. This section represents a tentative roadmap for my research for the next 5 years that I envision in two folds : (i) on the short term I wish to pursue the integration of ultrathin layered materials stacked into heterostructures for nonvolatile memories particularly i would like to demonstrate that our multilayer fluorinated nanoribbon can be an efficient floating gate, (ii) on a longer term, I plan to investigate the potential of 2D and TI layered material for thermoelectric power generation.

2.2 2D heterostructures for nonvolatile memory

2.2.1 Revisiting the band gap engineered charge trapping memory concept

The breakthroughs observed in the micro and nano electronic fields were always the result of the integration of new materials and the development of technological process to integrate them. Indeed, the passivation of silicon (Si) with silicon dioxide (SiO_2) has enabled years of miniaturization depicted by Moore's law and the integration of more and more complex electronic function with the advent of the digital world. To overcome the challenges dictated by Moore's law and foresee what is beyond, silicon carbide (SiC), diamond, and gallium nitride (GaN) have appeared for high voltage electronics thanks to their wide band gaps and thermal conductivity. Gallium nitride (GaN) and indium phosphide (InP) thanks to their high carrier mobilities are utilized for high speed and optoelectronic devices^{24,104,105}, whereas, high-k dielectrics have been integrated

as a replacement to SiO_2 . Nevertheless, the technological constraints originating from the ultimate miniaturization have substantially increased the complexity and cost of the manufacturing tools and modeling methods therefore stressing the need for alternative and spawning a large field of research notably in material science^{106,107}. These innovations have strongly and permanently affected our daily life with the internet of things (IoT) taking an increasing space, the world's population is about 6 billion that is the amount of cell phones circulating. Many devices will be utilized to monitor various signals and may not be as complex and power consuming as a smartphone nevertheless any of them requires some sort of nonvolatile memory. the NVM arena has witnessed the rise of a number of alternatives to the floating gate concept ranging from evolutionary to revolutionary devices and materials. While being under thorough investigation in academia as well as in the semiconductor industry none of these potential candidates has yet emerged as the ideal replacement for floating gate^{108,109}. I myself was working on alternative CT-NVM as senior scientist

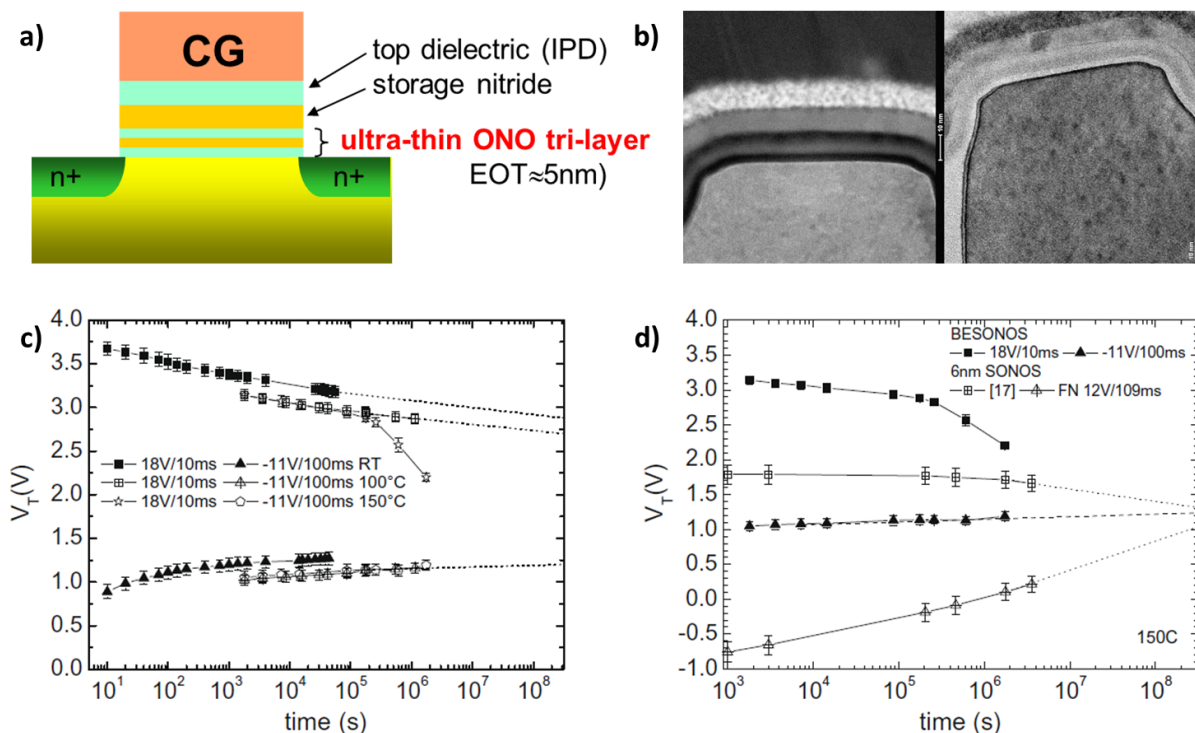


Fig. 2.1 Bang gap engineered nonvolatile memory.(top) Illustration of the vertical heterostructure and cross section TEM image of high k based device. (bottom) temperature dependent data retention for SONOS and BE-SONOS charge trapping devices.⁹

at NXP-TSMC Research Centre located at IMEC - Belgium to develop future non-volatile memories for 45nm and beyond. At that time, I studied various band gap engineered devices *e.g.* SONOS, TANOS, BE-SONOS based on high k materials integration^{9,10,12,13,110,111}. Although, we managed to demonstrate the potential of the CT concept, the data retention could not meet the high temperature requirements, Fig.2.1. It is hard to date to find a universal concept that meets all the criteria in terms of power consumption, programming speed and data retention. As a result, a

large focus is on the material properties and recently 2D materials appeared in the picture thanks to the interesting impact their ultrathin nature brings to the electronic transport properties.

2.2.2 What can we expect from 2D materials?

As CMOS scaling is approaching its physical limits, new devices, circuits and architectures are being investigated. At the device level, one route consists of replacing the Si with higher mobility channels such as Ge or III-V semiconductors. Another one proposes 2D semiconductors such as metal dichalcogenides (MX₂). Should we want to demonstrate a 2D materials based NVM, one should first question the benefit brought by the 2Ds in terms of scaling, Fig.2.2. This roadmap

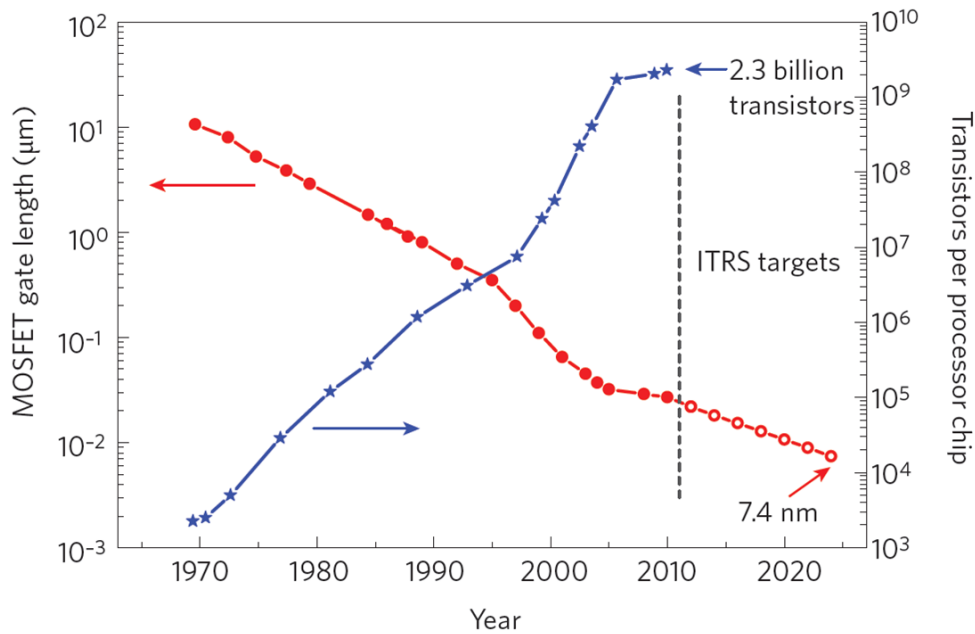


Fig. 2.2 ITRS roadmap showing in blue the number of transistors per chip and in red the transistor gate length¹¹².

has been built upon one material Si and one technology CMOS with a focus on speed *i.e* high I_{on} current or high mobility-light m_{eff} and low I_{off} by maintaining a good electrostatic integrity in order to suppress short channel effects. Indeed, although a 5nm Si MOSFET technology could not be ruled out yet, it is clear that the source-drain tunnelling will be a limitation beyond 5nm, Fig.2.3. This tunnelling is responsible for the degradation of the sub-threshold slope (SS) and high I_{off} current therefore the increase in static power consumption¹¹³. The SS and the I_{off} that varies in $exp(-Eg/mkt)$ require a reasonable bandgap and as a result a new technology must be implemented. Here 2D materials which presents heavy m_{eff} and lower mobility present a scaling advantage as well as Si nanowires that remains also a possible contender¹¹⁴. To optimize the control over the channel, a short characteristic length of short channel FETs is required. This length is defined for single gate SOI MSOFETs as , Eq.2.1:

$$\lambda = \sqrt{\frac{\epsilon_{ch}}{\epsilon_{ox}} t_{ch} t_{ox}} \quad (2.1)$$

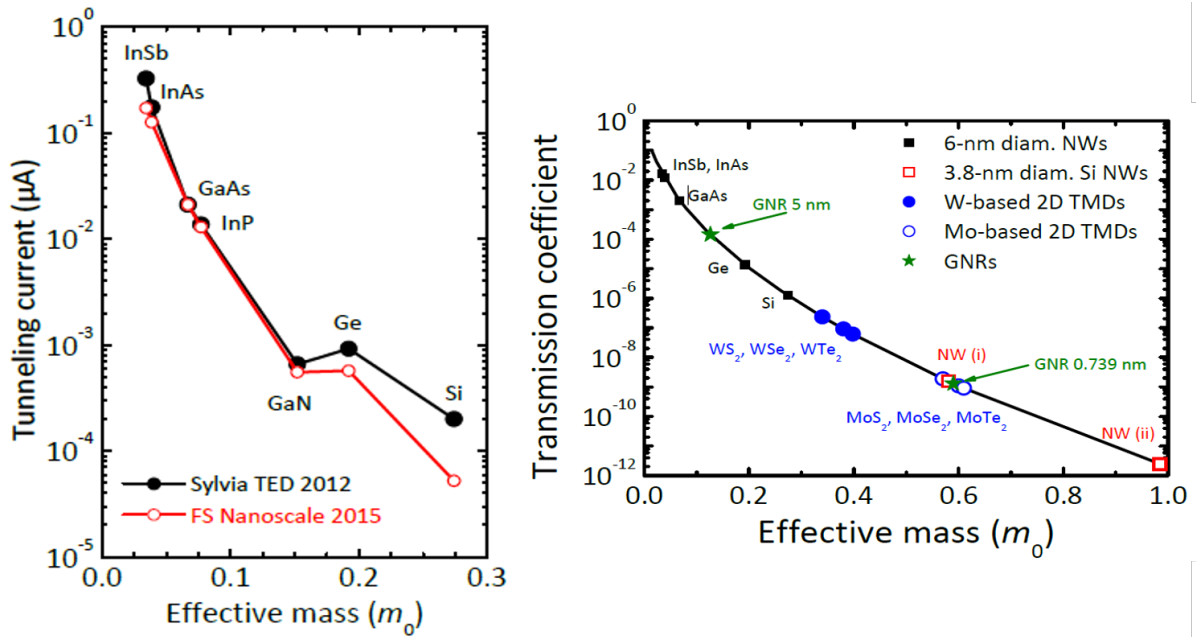


Fig. 2.3 (left) Tunneling current versus the effective masse for various compounds⁴⁷, (right) transmission coefficient versus the effective mass for III-V as well as 2D materials¹¹⁵.

different expressions exist for Finfet, nanowires devices and the trend indicates that thin and narrow channel are the most performant to suppress SCE. Inherently to their ultrathin thickness and lower dielectric constant, short-channel effects are limited in 2D FETs which translates into a better electrostatic control of the gate over the channel barrier¹¹⁶. For instance λ is reduced to only 2 nm for a 5nm thick MoS_2 channel and 1 nm equivalent oxide thickness (EOT) formed by 6 nm HfO_2 . Clearly, should a reliable large scale technology emerges for the production of these materials, GNRs, 2D materials and Si NWs *i.e* high m_{eff} materials are serious candidates for scaling not for the current expectation of the ITRS but rather for gate length below 5nm. This can be achieved thanks to the short scale length and the excellent electrostatics suppressing source drain tunnelling^{117,118}. With such a scalable technology a natural step forward is to produce the memory function that is indispensable for any solid state system or sensor.

2.2.3 2D - CT NVM

The target of the current research is to develop 2D vertical heterostructures for charge trapping nonvolatile memory. We have already developed and patented several building blocks to achieve this goal. GeePs lab (CNRS, UPMC and CentraleSupélec) have filed a patent entitled Method for obtaining a graphene-based field effect transistor⁷⁷, in particular a memory field effect transistor, equipped with an embedded dielectric element application number EP16305161.8. In our proposed embodiment, we introduced the fluorination of a multilayer graphene ribbon on undoped SiC substrate, Fig.2.4a&b, to fabricate a graphene/fluorographene heterostructure for field effect

devices^{*}, Fig.2.4c. Here the device is first patterned and the effective width of the channel is reduced through plasma assisted fluorination to yield an graphene nanoribbon.

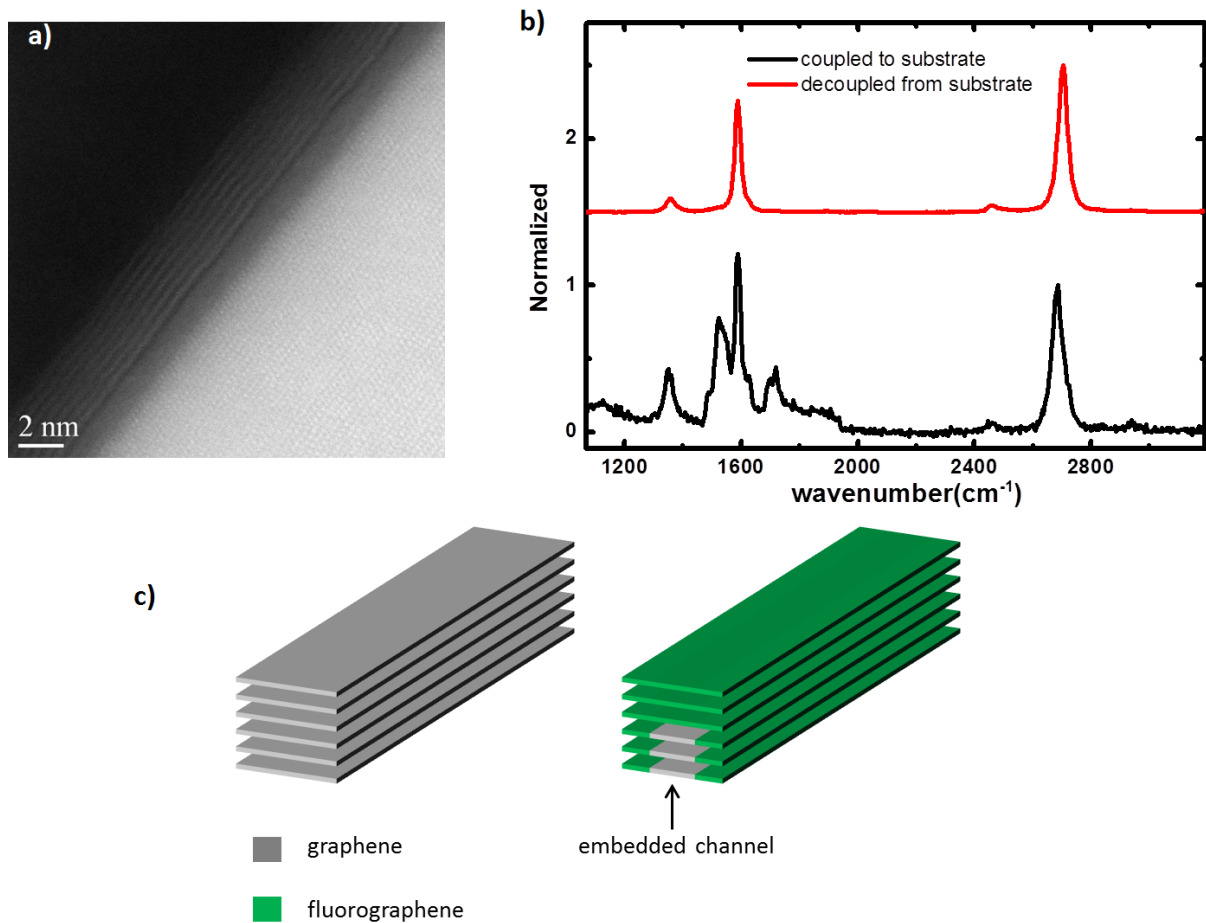


Fig. 2.4 (a) TEM image of multilayer graphene grown on the C-face of SiC substrate. (b) Raman spectrum of a monolayer coupled to the SiC substrate and on the top few layer uncoupled exhibiting a twist angle. (c) Schematic of the plasma assisted graphene channel fluorination yielding an embedded multilayer ribbon.

Among the building blocks of a CT-NVM are :

The channel : As mentioned earlier, short-channel effects are strongly limited in 2D-material based devices. We have various options to fabricate the channel providing the electrons. GNRs Fig.2.5a&b, MoS_2 or $BiSe_2$ are particularly good candidates. The mobility is reasonably high enough \approx few $100 \text{ cm}^2/Vs$ and they present a band gap that allows the transistor to be turned off. Note that for this purpose, the mobility is not a key criterion since the electron, will flow vertically. Our first attempt based on the graphene/fluorographene heterostructure Fig.2.5c yield working devices but with low I_{on}/I_{off} (defined as the highest on current over the charge neutrality point current) although we obtained for a few devices 10^4 ratio at room temperature. The off current is limited by the thermoionic emission that readily occurs at room temperature Fig.2.5d. Our prospect is optimistic considering that graphene nanoribbons with tunable bandgap and from 0.27

* Narrowing the effective channel width of graphene nanoribbon by plasma assisted fluorination submitted to IEEE Electron devices letters

eV to approximately 1 eV have been calculated and fabricated^{119,120}. Moreover, we believe that our contacts were not optimized and a judicious choice will reduce further the leakage current. Note that here the subsequent fluorination passivates the edges of the ribbon (spacers) and reduces further the effective width W_{eff} and on the other hand to render a few fluorinated layers dielectric *i.e.* become a tunnel oxide or a blocking oxide for CT-NVMs.

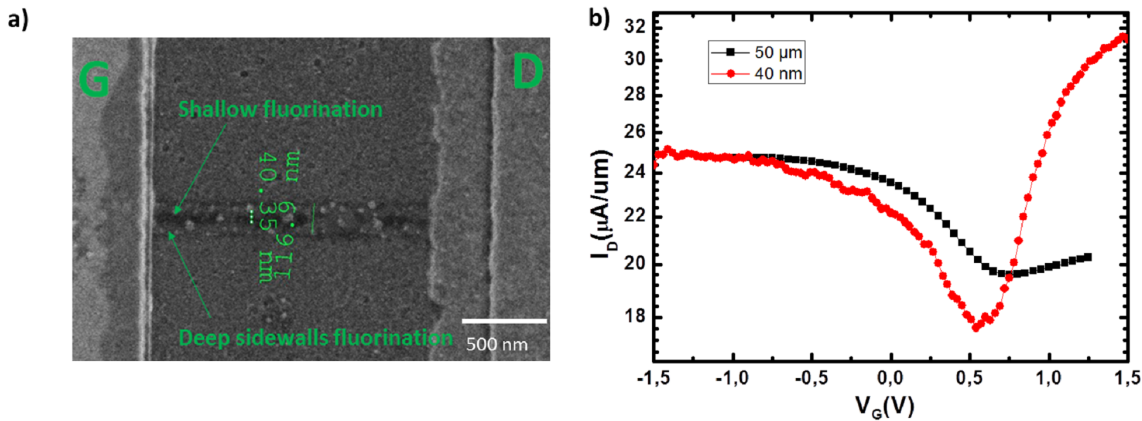


Fig. 2.5 (a) HRSEM image of a fluorinated GNR;b) I-V characteristics of GNRs with 50 μm and 40 nm channel width, a clear improvement is visible for the 40 nm device despite a poor *on/off ratio*.

The tunnel oxide

For this function, we propose two options. the first one is inherent of our proposed embodiment if the channel is made of a GNR fluorinated with a C/F ratio close to 1. The second option requires h-BN/graphene interface and large scale synthesis are emerging, Fig.2.6. A major advantage presented by h-BN is that it does not dope nor trap at the interface. This would avoid any trapping at the interface enabling the carrier to tunnel into the trapping layer preventing threshold voltage shift, Fig.2.7, However this observation remains to be confirmed after cycling a device through Fowler-Nordheim injection. First, the integrity of the material could be much better as opposed to high-k materials already implemented. The ultra-thin interfaces may be less prone to inter-diffusion Fig.2.6) and segregation processes which deteriorate the electronic properties. The thickness uniformity permits a uniform electric field along the width and therefore a controlled voltage to be applied on the gate which translates into the transfer of the carriers at the same speed with a shorth transit time considering the atomic scale thicknesses involved.

The trapping medium

The prerequisite is that material presents sufficient charge trapping states. This latest could be the density of states of the materials and therefore graphene or MoS_2 could be candidates. Typical floating gate devices suffer from a poor capacitive coupling from the gate to the channel and large capacitive coupling to neighbouring devices increasing the cross talk. CT devices however, has a single gate and therefore present a larger capacitive coupling. Current CT devices using SiN as a trapping medium Fig.2.1, are hindered by the variability of V_t upon scaling due to the limited trapping sites and uniformity. Moreover, the retention is also limited and temperature dependent

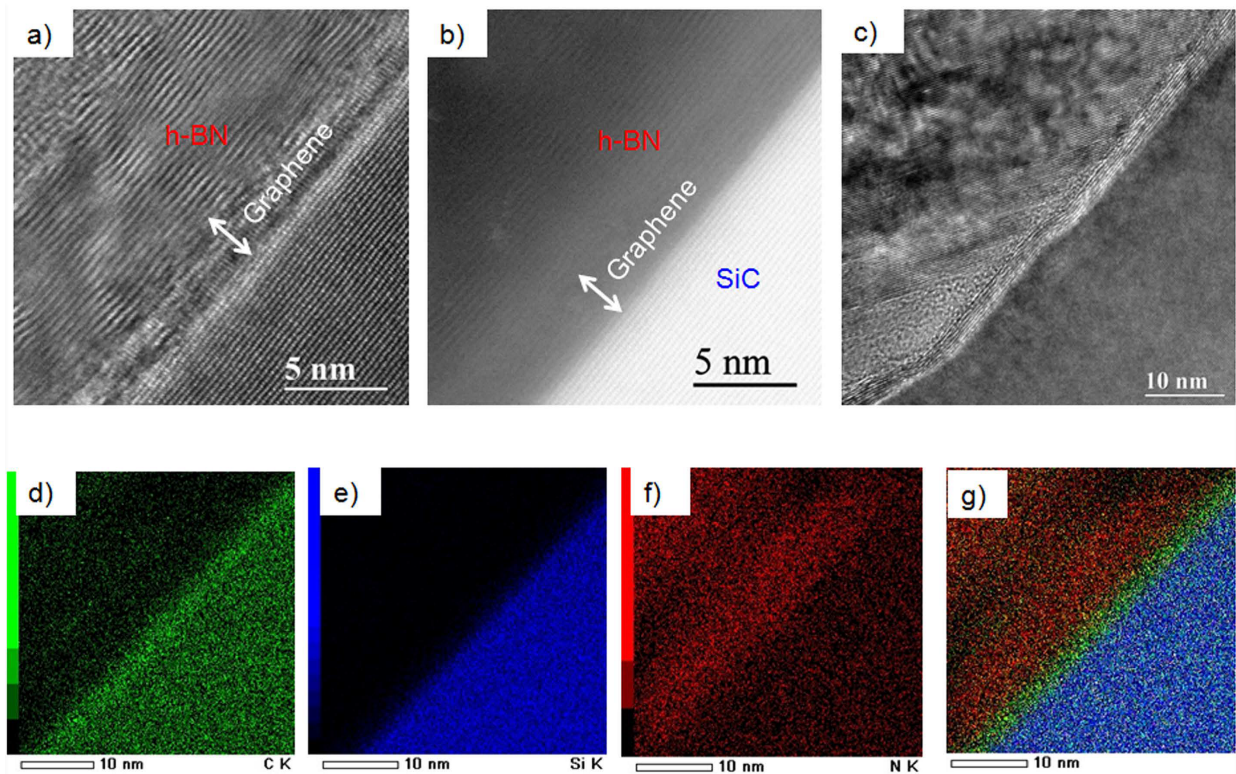


Fig. 2.6 (a) Bright-field Scanning Transmission Electron Microscopy (STEM) image and (b) corresponding High Angle Annular Dark Field (HAADF) STEM image of h-BN on graphene/4H-SiC heterostructure, (c) High-Resolution Transmission Electron Microscopy (HRTEM) image of h-BN on the step edges of graphene on SiC, (d-f) EDX elemental maps showing, respectively, the spatial distribution of C, Si and N in the selected area of the h-BN on graphene/4H-SiC heterostructure. The overlay of the three maps is given in (g)¹²¹.

because the traps are rather shallow and easily escape upon activation even more if either tunnel and/or blocking oxide present conductive paths.

Graphene is indeed a candidate as it presents a high density of states even higher if stacked in multilayer, its workfunction is tunable⁴⁹ and the low dimensionality is a major add on compared to typical FG devices particularly in terms of cross talk. We have already investigated this building block and our preliminary results show a large amplitude of the work function but also that functionalized graphene nanodiscs could be implemented as trapping sites reaching trap density as high as in SiN (10^{19}cm^{-3})*. Graphene can be functionalized to increase the charge trapping sites or tailor the workfunction to locate them deeper in the energy band diagram, Fig.2.8. This would further improve the charge retention especially at high temperature as the carrier will see a larger barrier. Note that fluorographne with C/F ratio below 1 is also an possible option to be investigated as trapping medium. It is conceivable that such nanostructures become less sensitive to random fluctuation as here no hopping mechanism should take place considering the configuration of the trapping medium. Moreover, it is possible to position the electron trap deeper in the

* Integration of functionalized graphene nano-discs as trapping centers for nonvolatile memory submitted

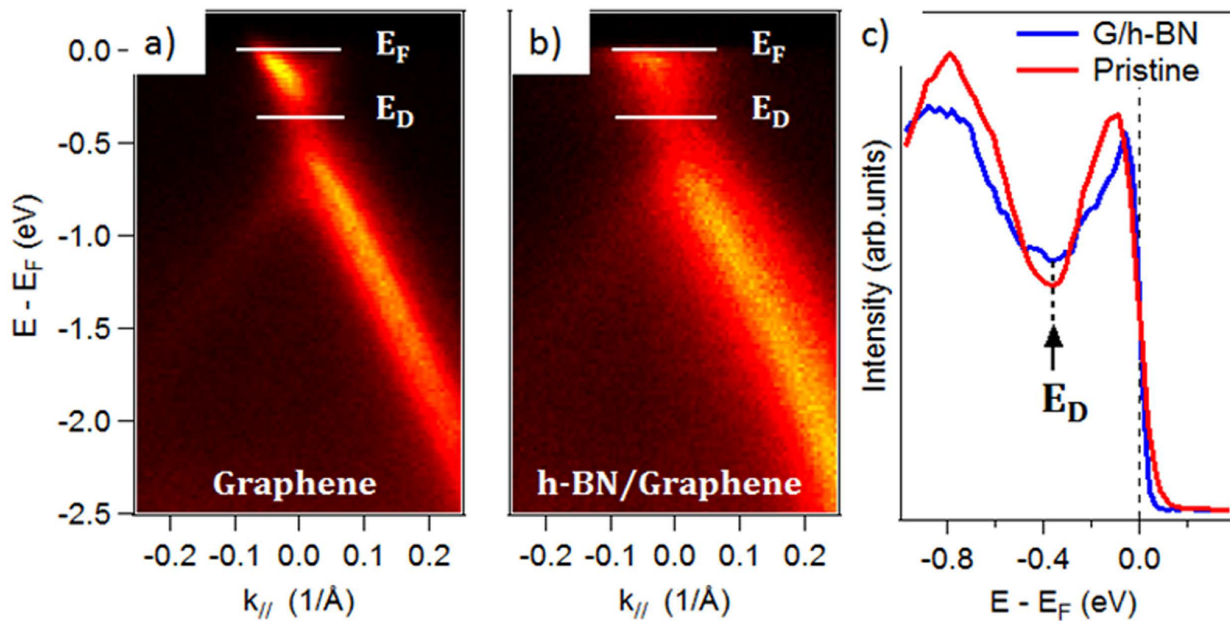


Fig. 2.7 (a,b) ARPES measurements of pristine graphene and h-BN/graphene, measured at $h\nu = 60$ eV, through the K-point, in the Γ K direction; (c) ARPES intensity integrated spectra as a function of the binding energy, extracted from the 2D ARPES map, for the initial pristine graphene (red line) and h-BN/graphene (blue line)¹²¹.

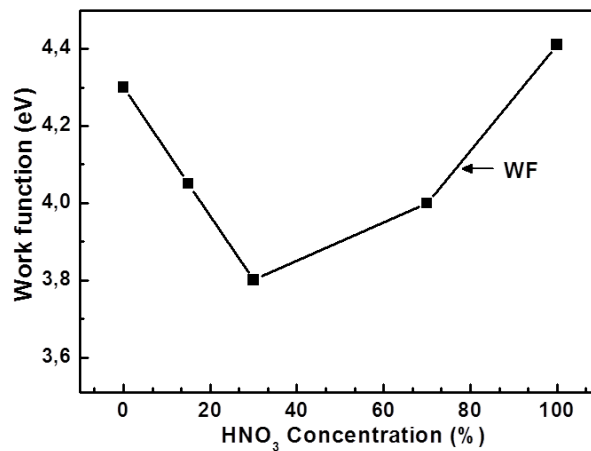
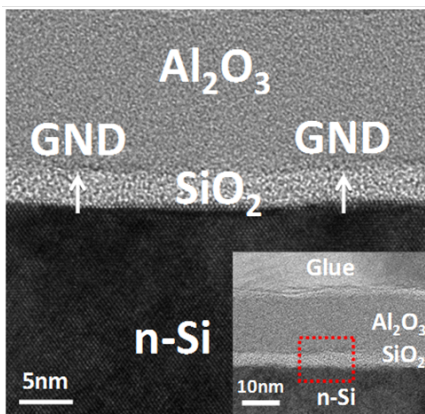


Fig. 2.8 (left) cross section HR-TEM of GNDs on 3-nm SiO_2 and capped with Al_2O_3 to improve the contrast (submitted to Carbon). The GNDs are ≈ 20 nm diameter; (right) Modulation of the workfunction with acid doping⁴⁹.

well using the workfunction tuning demonstrated elsewhere.

The blocking oxide and gate

Our initial embodiment consists of multilayer graphene grown on SiC substrate. The graphene is patterned using ebeam lithography to sub micrometer scale typically 150 nm. The pattern is the subsequently fluorinated using a CF_4 plasma. Fluorine attaches to graphene and diffuse in

few layer on the top and sidewalls. Therefore, the effective width of the channel w_{eff} has further decrease compared to the designed width w . Thus a dielectric crust passivates the sidewalls as well and embeds the graphene nanoribbon (GNR). At last, the deposition of a metal gate allows the fabrication of a trigate GNR device, Fig.2.9. In this configuration, the fluorinated graphene acts as a gate dielectric. However this building block could be implemented on top of MoS_2 channel for instance and therefore the fluorinated GNR would compose the trapping medium and the blocking oxide. Here we extended the embodiment to another configuration to fabricate a full 2D materials charge trapping nonvolatile memory *i.e.* 2D CT-NVM. , Fig.2.9. We are currently discussing this technology with NUS Singapore using their Pulsed Laser Deposition methods. Note that the gate workfunction must be appropriately tailored to suit the band alignment imposed by the heterostructure and the channel doping. This is where graphene presents a major asset even better than being a GNR as its workfunction is easily tunable.

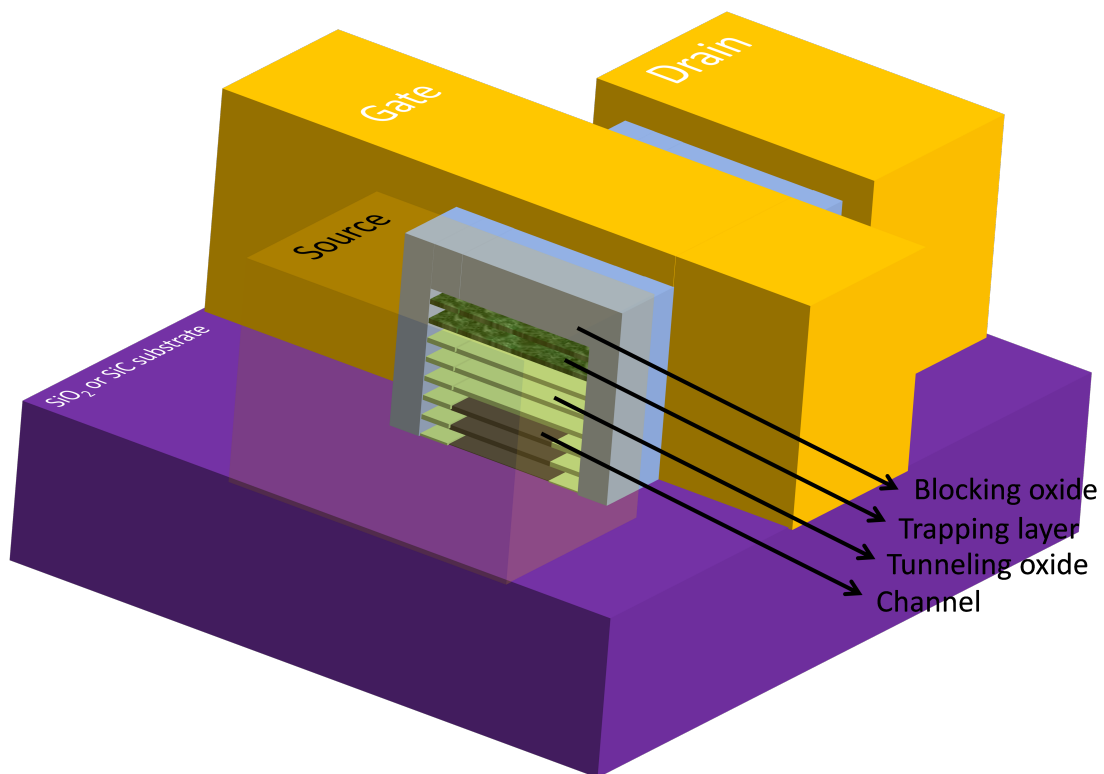


Fig. 2.9 Finfet like 2D - CTNVM proposed using the fluorinated GNR demonstrated before.

Criteria

Band offsets *i.e.* CB: conduction band offset/VB: valence band offset. CB and VB offsets are critical to ensure band gap engineering and maintain the data retention (or electron trapping) in charge trapping devices. Indeed, should the barrier be sufficient the electron will be resistant to thermoionic emission. On the other hand however, the P/E voltages to tunnel electrons could be a bit larger.

Dielectric constant to reduce programming and erase voltage *i.e.* low power

Compromise between improved performance and good reliability *i.e.* device lifetime

Charge distribution in 2D heterostructure by PEEM - WF shift

low power injection mechanisms - Fowler Nordheim (FN) vs. Channel Hot Electron Injection (CHEI)

2.3 Thermoelectric generator (TEG)

2.3.1 Physical basis of low dimensional materials-based energy efficient devices

The recent advances in material sciences and the world wide energy concern, have triggered a large research effort to develop high-performance thermoelectric materials and devices for energy conversion using the integration capabilities of nanotechnology. Interestingly, the optimization of the figure of merit ZT relies on a contradictory trend : materials must exhibit a very low thermal conductivity while both electrical conductivity and Seebeck coefficient must be large, Eq.2.2. In bulk materials, these transport coefficients are interrelated. Therefore technology, material science and device design must all contribute to address this tedious task,¹²².

$$ZT = \frac{S^2 \sigma T}{\kappa_l + \kappa_e} \quad (2.2)$$

S is the thermoelectric power or Seebeck coefficient, σ is the electrical conductivity and κ_l is the lattice thermal conductivity and κ_e is the thermal conductivity of the electronic carriers. Large values of ZT require high S , high σ , and low κ . Increasing the carrier density, n increases the electrical conductivity which is detrimental to the Seebeck coefficient that decreases. The term $S^2 \sigma$ *i.e.* the power factor is optimized for degenerated narrow gap semiconductors with $n \approx 10^{19} \text{ cm}^{-3}$. On the other hand, the thermal conductivity κ is dominated by the phonons contribution to the heat conduction. Alloying has been utilized to reduce κ_l but also to impact the electrons and holes mobility therefore reducing σ . In 1999, M.Dresselhaus *et al.*¹²³ demonstrated that low dimensional materials exhibit an enhanced thermoelectric figure of merit Eq.(2.2) as opposed to their bulk counterparts thanks to the quantum confinement that sharply change the density of states improving S as well as the phonon scattering reducing the lattice contribution to the thermal conductivity. The low dimensionality particularly enhances the density of states near E_F , leading to an enhancement of the Seebeck coefficient, Fig.2.10.

In that regard, low dimensional materials could potentially change the picture. Indeed, here the characteristic length l be it the thickness of a quantum well in a 2D system or the diameter of a wire for 1D system or a quantum dot for 0D system, disentangle to some extent the transport parameters¹²⁴.

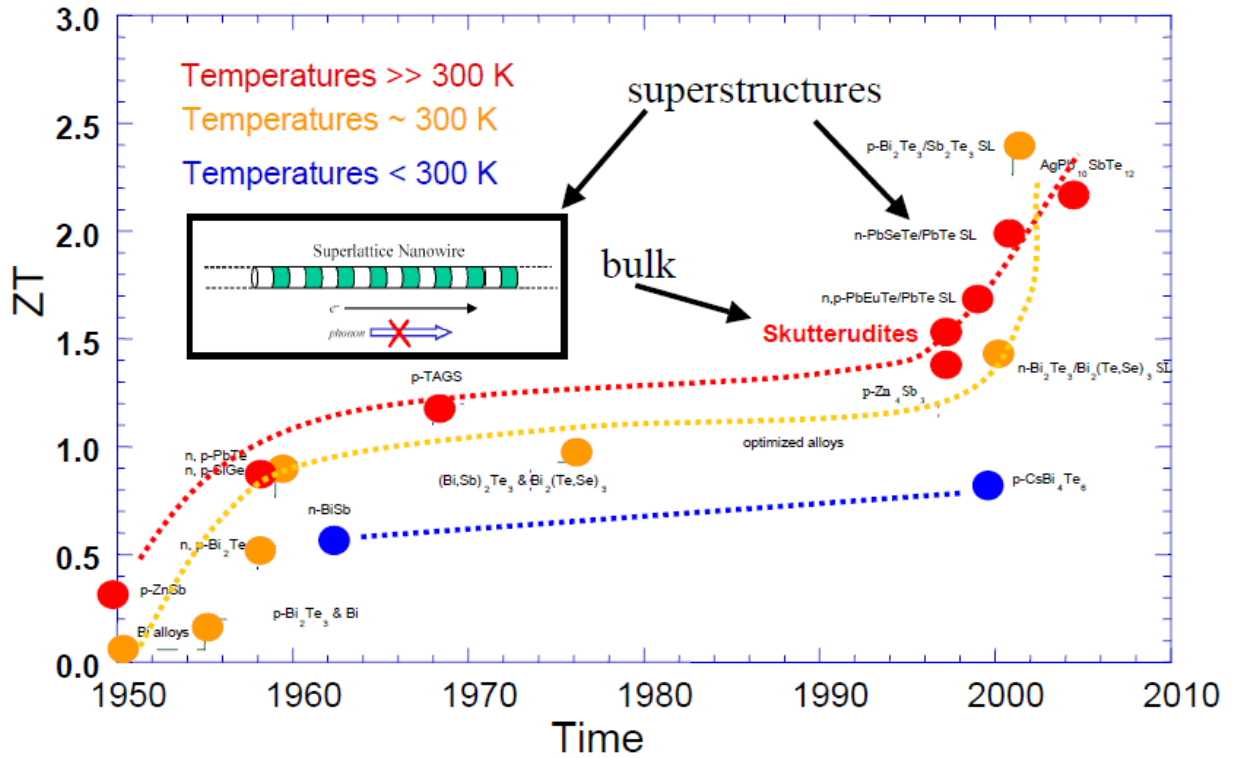


Fig. 2.10 Gradual increase of the thermoelectric figure of merit (ZT) during last 60 years from *K.Knek – FyziklnstavAVR*.

Impact on the thermal conductance : the phonon mean free λ_l path is limited by l whereas the electron mean free path λ_e is not so. Therefore if $\lambda_l \simeq l = \lambda_e$ the lattice thermal conductivity κ_l is reduced with a limited impact on the electron mobility.

Impact on the thermoelectric power S : quantum confinement and electron energy filtering are the main effect that improve S compared to bulk S . In degenerated systems, such as metals and heavily doped semiconductors, the Seebeck coefficient can be expressed by a simplified form of the Mott relation, Eq.2.3:

$$S = \frac{\pi^2 k_B^2}{3e} \left\{ \frac{\partial \ln \sigma(E)}{\partial E} \right\}_{E=E_F} \quad (2.3)$$

This expression remains valid independently of the conduction mechanism be it through band states, localized states or hopping amongst others. Should one consider the band conduction mechanism, the electrical conductivity $\sigma(E)$ is a function of the carrier density $n(E)$ that is itself a function of the density of states $g(E)$ and the mobility $\mu(E)$ or the relaxation time $\tau(E)$, Eq.2.4:

$$\sigma(E) = n(E)e\mu(E) = n(E)e^2 \frac{\tau(E)}{m^*} \quad (2.4)$$

where e is the free electron charge, and m^* the effective mass. Note that in solids with non-parabolic bands, $m^* = m^*(E)$. As a result in order to enhance S one can tailor the energy dependence of the conductivity $d\sigma(E)/dE$ by enhancing the $dn(E)/dE$. Increasing this latest, is achieved by tailoring the energy dependence of the density of states $dg(E)/dE$. This is precisely

the outcome of the quantum confinement with sharp maxima observed for nanowires, Fig. 2.11. On the other hand, one can also increase the energy dependence of the mobility $d\mu(E)/dE$ by

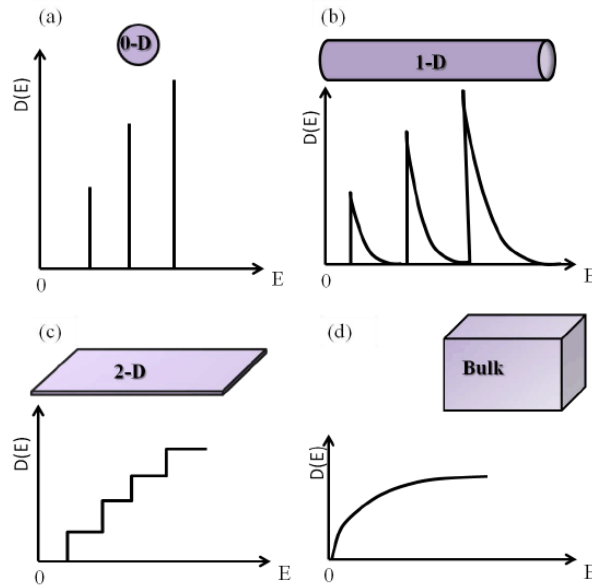


Fig. 2.11 Schematic representation of: (a) 0-dimension (0-D), (b) 1-dimension (1-D), (c) 2 dimension (2-D) and (d) 3-dimension (3-D). The corresponding density of states (DOS) plots for each type is also presented¹²⁵.

increasing the electron energy filtering *i.e.* increasing the scattering time's energy dependence $d\tau(E)/dE$. In parabolic bands semiconductors, the relaxation time is represented by a power law, Eq. 2.5:

$$\tau = \tau_0 E^{\lambda - \frac{1}{2}} \quad (2.5)$$

where λ is the scattering exponent: 0 for scattering of electrons on acoustic phonons, 1/2 for scattering of electrons on neutral impurities, and 2 for scattering of electrons on ionized impurities. Therefore doping the materials *i.e.* introducing ionized impurities is a possible route. Besides scattering, potential barriers in 2D heterostructures can be designed in superlattice¹²⁶. For sufficiently thick barriers where tunnelling is cancelled, the electron transport occurs owing to hot electrons that possess sufficiently high energy for thermionic emission over the barrier. In this type of band gap engineered structures, it is conceivable to substantially increase the Seebeck coefficient with a relatively low impact on the electrical conductivity, Fig. 2.12. Note that only majority carrier system are of interest in heterostructure systems as recombination mechanisms with minority carrier would reduce the conversion efficiency. The Mott relation simplifies if one considers metallic transport, Eq. 2.6 :

$$S \simeq \frac{\pi^2 k_B^2}{3e} \frac{T}{E_F} \quad (2.6)$$

In 2015, Hippalgaonkar *et al.*, demonstrated in single and few layer MoS_2 a record high power factor as large as 8.5 mW/mK^2 at room temperature¹²⁸. The enhanced powerfactor is attributed

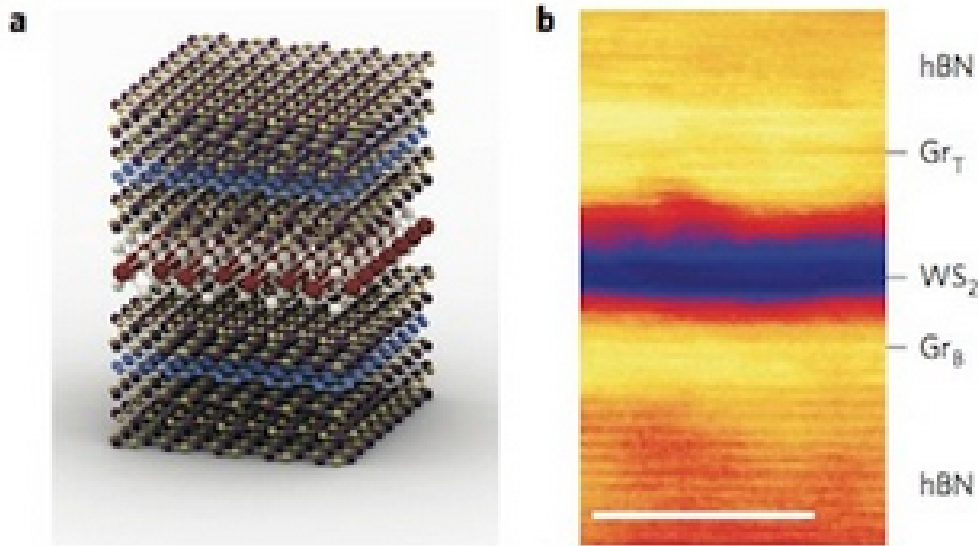


Fig. 2.12 a, Schematic of the single quantum well (SQW) heterostructure hBN/GrB/2hBN/WS₂/2hBN/GrT/hBN. b, Cross-sectional bright-field STEM image of the type of heterostructure presented in a. Scale bar, 5 nm.¹²⁷

to a unique combination of high mobility and high effective mass. This is twice higher than commercially used bulk Bi_2Te_3 therefore showing the potential of 2D TMDCs for thermoelectric applications. At high concentration, in 2D materials, the density of states (DOS) near the Fermi level can be written as, Eq.2.7 :

$$DOS \simeq \frac{g_s g_v m^*}{2\pi(\hbar)^2} \quad (2.7)$$

where $g_s = 2$ and $g_v = 2$ are the spin and valley degeneracies at the Fermi energy, E_F , respectively, m^* is the effective mass and \hbar is the reduced Planck's constant. Therefore, $E_F \propto n_{2D}/m^*$ that yields to $S \propto m^*/n_{2D}$. Since $\sigma = n_{2D}e\mu$, the powerfactor $S^2\sigma \propto (m^*)^2\mu/n_{2D}$ scales with the mobility for a given carrier concentration.

For the last few decades, researchers have developed extensive efforts to overcome the maximum room-temperature ZT 1 of commercial thermoelectric materials. In 1999 Dresselhaus et al proposed to enhance the ZT through nanostructuring. Recently, there has been a substantial activity around topological insulators (TI), a new class of electronic materials. TIs exhibit similar material properties such as heavy elements and narrow bulk gaps, with typical TE materials. The topological surface states (SSs) surrounding the TIs offer additional surface transport channel therefore the possibility to disentangle and modulate the transport parameters related to either electrical conductivity or thermal conductivity¹²⁹. As a matter of fact, Bi_2Te_3 and Sb_2Te_3 , known for decades as the best room temperature thermoelectric and narrow gap materials, happen to be TIs, Fig.2.13. The key property of this new class of material lies on its surfaces, *i.e.*, the topological surface states (TSS). These latter in the absence of magnetic impurities are immune to back scattering at the edges of the material. As a result, TSS are expected to exhibit high mobility and could become highly promising candidates in ultra low power nanoelectronics.

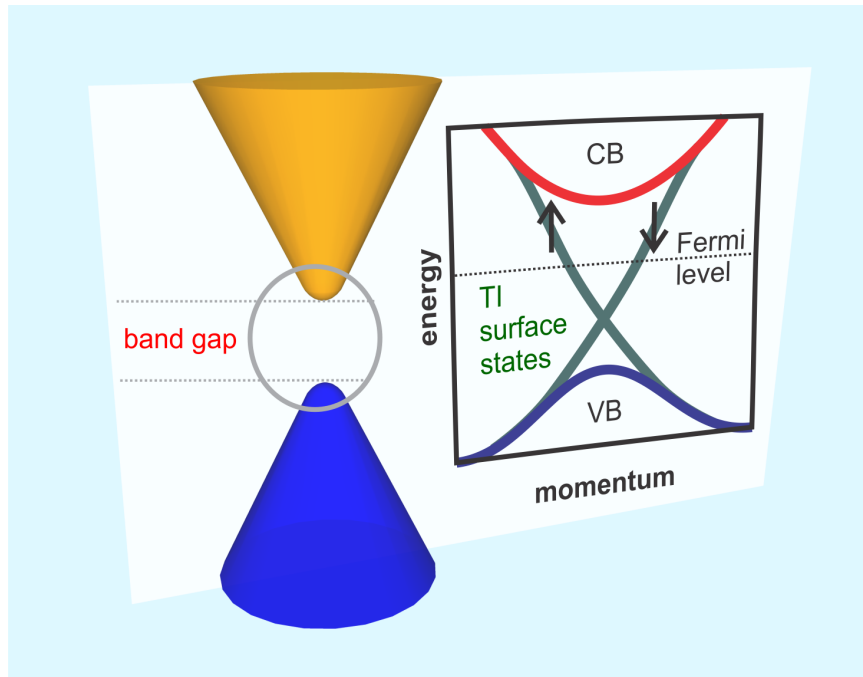


Fig. 2.13 Band structure of a TI, showing the valence (blue) and conduction (orange) bands, with the spin-locked surface states crossing the bulk band gap.¹³⁰

2.3.2 Thermoelectric generator

In parallel to nanoelectronic devices, I intend to develop thermoelectric harvesting systems using at the first stage TI such as $BiSe_2$. The immunity to backscattering provides the TSSs of TIs a high mobility that could enable energy efficient devices where the TI material becomes a high conductivity (low resistivity) conduction channel with reduced Joule heating. Note that this property opens also opportunities in transistors or interconnects¹³¹. In the United States, the DARPA MESO programme investigates heterostructures made of TIs with magnetic materials that enable band gap engineering and offer perspectives for low power transistors such as the BisFET first proposed for bilayer graphene¹³². The mobility of the TSSs can be further improved by patterning nanoribbon, this is a major advantage over graphene whose mobility is impacted by edges defects. As stated above, one strategy to improve the ZT figure of merit in thermoelectric devices is to decouple the electron and the thermal transport. This sheds a new light on TIs as they inherently decouple the electronic transport carried by the TSSs whereas the thermal transport is carried out by the bulk. There has been several report demonstrating the added value of TIs for TEG. Purdue University is developing high ZT TEGs based on surface excitonic with coupled complementary TSS as channels¹³³. When two TSS from the same TI or an additional one are placed face to face with opposite carriers, excitons (electron-hole pairs) could form and condense into an excitonic condensate (EC). This configuration could produce an electronic superfluid with no power dissipative electronic transport. This has already been observed in segregated graphene monolayers¹³⁴, Fig.2.14. However this configuration requires the gating of each TI surface to provide proper carrier and density and to prevent electrons and holes from recombining. It is hard to quantify the voltage required but one could imagine a hybrid PV-TEG system where the Voc of a solar cell

could gate the TI based TEG¹³⁵. I first experienced thermoelectricity during my PhD at IEMN

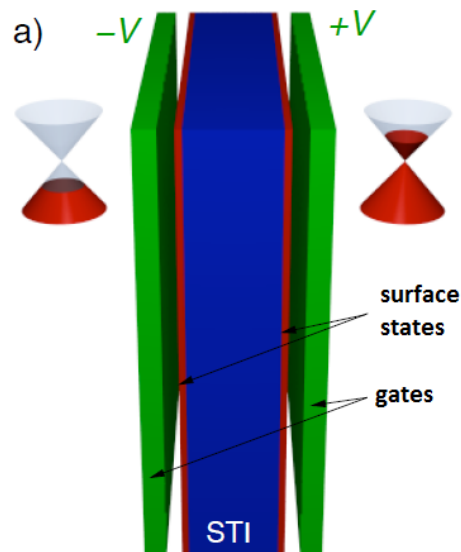


Fig. 2.14 Schematic of a topological excitonic condensate based on two coupled, complementary TI surfaces. Each surface is controlled by a gate to induce proper carrier type and density. High mobility TSS may enhance the ZT, and if excitonic condensate occurs, the superfluidic (dissipationless) electronic transport may further enhance the ZT dramatically¹³³.

(1999-2002) where i optimized the thermoelectric thermopower of a polysilicon thermopile and demonstrated an infrared microsensor². Notably we demonstrated through a careful design that it is possible to circumvent the convection losses and increase the sensitivity³. This structure has been further improved by Pr D. Leclercq's group at IEMN-CNRS and several patents were filed. These designs present supported thermoelements that maintain a temperature gradient between the hot and the cold junctions. It is now being implemented as a thermogenerator in the OPEN FOOD SYSTEM project supported by the OSEO funding body (9.1 Meuros)* where IEMN lab amongst other academic partners are involved with household appliances leaders such as SEB and TEFAL, Fig.2.15. At NXP-TSMC research centre, I patented a device that can be fabricated on a CMOS substrate¹⁵. The thermal contrast is created from the shallow trench isolation (STI) strips. My initial embodiment includes a light pipe to locally heat the hot thermojunction for non contact measurements. However, this can be adapted using a metal filler to conduct heat directly onto a TI thermoelement, thus avoiding the bonding of an absorber and making a monolithic TEG device. So far most of the work around the perspective of TIs and 2D materials for TEGs provides useful data on transport properties but little experimental developments to fabricate optimized TEGs has been carried out.

* www.openfoodsystem.fr/

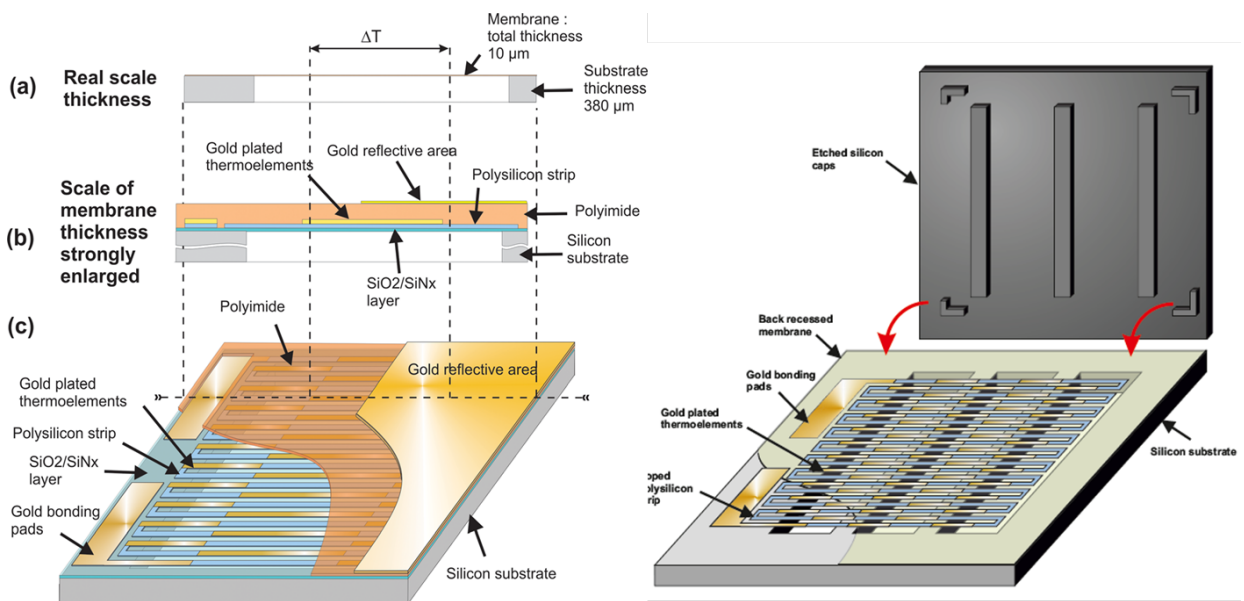


Fig. 2.15 (a) Schematic of a single-membrane infrared microsensor: (a) cross section in real scale, (b) cross section along a line of the thermopile strip (membrane thickness enlarged), (c) sight in sectional view. (b) Schematic of micro TEG with the silicon absorber patterned and transferred onto the hot thermojunctions¹³⁶.

2.4 Conclusions and Perspectives

The advent of two-dimensional (2D) crystals offer a wealth of new challenges and opportunities to the device research. Inherently to their ultra thin nature and their effective mass, the electrostatic picture can be substantially enhanced and new device architectures in both planar and vertical 2D heterostructures such as tunnel FETs may appear in a close future. Moreover as we observed on graphene, the modulation of the transport properties and work function through various functionalization methods is a major asset to customize electrodes and/or channels. Another aspect that has been recently put back under the spot lights considers the thermoelectric properties of layered materials particularly the topological insulators that are expected to enhanced the thermoelectric figure of merit ZT using the surface states (TSSs) that decouple electronic from heat conduction. Engineering wise, these observations are very promising and I target two types of applications *i.e.* non volatile memory (2D CT-NVM) and thermoelectric conversion that both need to be addressed within the scope of material sciences and device engineering. As the investments in this technology on the national and international scene keeps increasing it is of out most importance that solid state demonstrators are fabricated. Regarding 2D materials such as graphene and beyond I am setting a collaborations with research groups that develop large scale 2D materials. This technology could be implemented to fabricate our 2D CT-NVM device. On the other hand, UPMC - INSP lab has applied to extend its MBE capabilities to the growth of vertical 2D heterostructures. In addition, it is already possible to exploit the existing expertise in the growth of TIs such as Bi_2Se_3 to devise suspended TEG.

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Appendix I - Selected articles

Characterization of Phosphorus and Boron Heavily Doped LPCVD Polysilicon Films in the Temperature Range 293–373 K

M. Boutchich, K. Ziouche, P. Godts, and D. Leclercq

Abstract—In this paper, thermal properties of phosphorus and boron-doped low pressure chemical vapor deposition (LPCVD) polysilicon layers with regard to sensor applications are presented. Thermoelectric coefficient and relative resistance variations of polysilicon are investigated within the temperature range of 293–373 K.

Test structures and characterization benches have been developed to obtain measurements with precision of 5%. Ion implantation has been experimented to achieve low electrical resistivities and high Seebeck coefficients. It can be seen that temperature coefficient of doped polysilicon resistance are negative, approach zero, or positive depending on the doping concentration. These results are, to our knowledge, the first reported for such dopants concentrations and are important for design and optimization of high sensitivity thermal sensors using n- and p-doped—LPCVD polysilicon thermopile.

Index Terms—LPCVD-doped polysilicon, Seebeck coefficient, thermoelectricity, thermopile, relative resistance variations, thermal sensors.

I. INTRODUCTION

POLYSILICON has many important applications in IC and microsystem technology. Our study takes part of the work on polycrystalline silicon as a convenient material for thermal sensors. A variety of thermoelectric sensors integrated on silicon wafers and using polysilicon thermopiles have already been fabricated [1]. In order to develop a new high sensitivity infrared thermal sensor, we studied thermoelectric properties of phosphorus and boron heavily doped low pressure chemical vapor deposition (LPCVD) polysilicon from 2×10^{15} at/cm² to 10×10^{15} at/cm² doses. Dopants concentrations were chosen to achieve low electrical resistivity because of Johnson noise. Our aim is to use a new n- and p-type thermopile design that consists of a sequence of p–n diodes short cuted by ohmic contacts at the junctions. Each thermocouple delivers an emf proportional to the thermoelectric power defined as the difference between the two thermoelements Seebeck or thermoelectric coefficients. In order to integrate a large density of thermocouples and then improve the sensor sensitivity, we have to provide low electrical resistivity strips with good thermal properties such as Seebeck coefficient. Only

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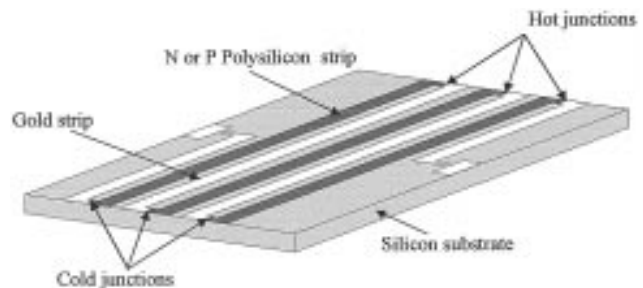


Fig. 1. Scheme of the thermopile chip.

a few papers have been published about polysilicon thin films characterization subjected to thermal applications [2]. In this letter are presented measurements of heavily doped polysilicon thermoelectric power and relative resistance variations $\Delta R/R$ in the temperature range of 293–373 K.

II. THERMOPILE FABRICATION

LPCVD polysilicon films with a 4500 Å thickness are deposited on thermally oxidized 2-in 100 silicon wafers (SiO₂ thickness 1.2 μm). A 500 Å thick dry oxide layer deposited at 1000 °C is used to prevent from exodiffusion. In order to reach the middle of the polysilicon layer, 70 and 180 keV acceleration voltages are used respectively for boron and phosphorus implantation. Annealings at 1000 °C for 1 h and at 1100 °C for 10 min are performed on different samples in nitrogen atmosphere to obtain an uniform distribution of dopants species across the polysilicon layer [3]. A significant improvement in sheet resistivity as well for boron doped layer as for phosphorus one are achieved with 1100 °C-10 min annealing corresponding to the best uniform distribution revealed by SIMS analysis. After dry oxide removing, a S-shaped strip, TLM and Van der Pauw test structures are patterned using RIE. As shown on Fig. 1, ohmic contacts are deposited by lift off on the strip to realize Au/doped polysilicon thermocouples. Chips are passivated with a 1000 Å PECVD nitride layer and thermopile contact pads are opened by RIE. At least, the wafers are sawed in 7×38 mm² chips. To characterize thermoelectric coefficients and relative resistance variations, two tests benches were developed.

The first test bench designed is devoted to thermoelectric coefficient measurements. It consists of two copper cubic pieces independently heatable in order to impose a temperature difference ΔT between the ends of the thermopile. Each end of the chip is inserted in a copper heat sink with good thermal contact.

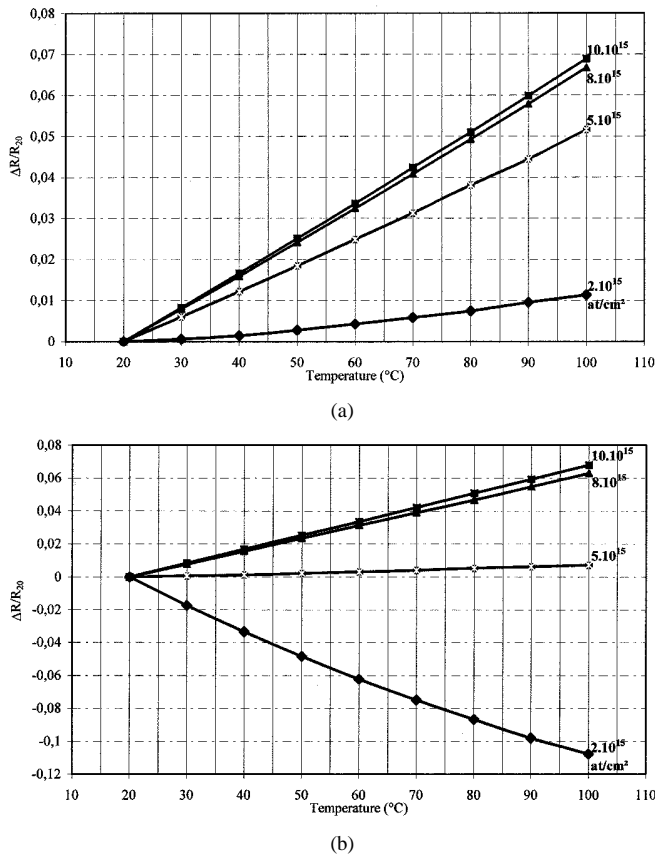


Fig. 2. (a) Relative resistance variations of boron-doped polysilicon versus temperature and (b) relative resistance variations of phosphorus doped polysilicon versus temperature.

The emf delivered is directly proportional to the thermoelectric coefficient α as $V = N \times \alpha \times \Delta T$, N denoting the number of thermocouples.

For relative resistance variations measurements, we developed a second experimental setup that consists of a block of copper lying on a hot plate. An inserted thermocouple enables us to record average temperature of the chip that is stuck on the piece of copper with silicon grease to provide good thermal contact [2] [4]. The hot plate is controlled with a temperature regulator within the range of 293 to 373 K. Contact pads of the thermopile are connected to a multimeter by wire bonding.

III. CHARACTERIZATION RESULTS

- 1) Relative resistance variations of boron and phosphorus-doped LPCVD polysilicon over the temperature range 293–373 K are shown in Fig. 2(a) and (b) with the implantation dose as parameter. Interesting points can be extracted. In this temperature range that represents typical operating range of almost all the infrared thermal sensors, relative resistance variations are quasi-linear. Temperature coefficient corresponding to the slope of the curve may be selected over a wide range, both positive and negative or approaching zero by selecting doping concentration. This property presents a great interest for sensors applications especially for temperature drift control [5] [6]. The shift in slope observed on Fig. 2(b) could be in-

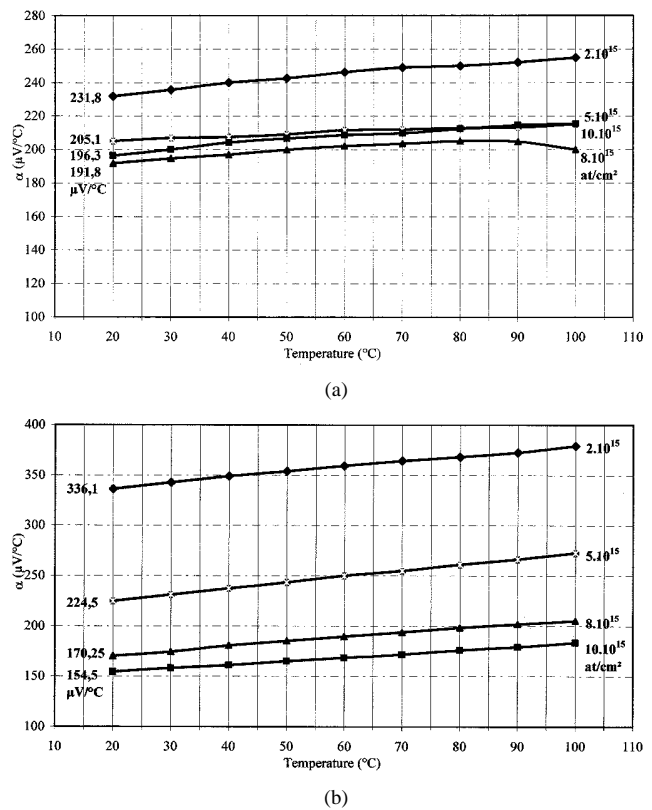


Fig. 3. (a) Thermoelectric coefficient of boron-doped polysilicon versus temperature and implantation doses. Thermoelectric coefficients at room temperature are represented on the left of each curve and (b) thermoelectric coefficient of phosphorus-doped polysilicon versus temperature and implantation doses. Thermoelectric coefficients at room temperature are represented on the left of each curve.

terpreted in terms of carriers mobilities that are affected by the temperature raise. According to Arora *et al.* [7] and Seto [8] experiments, mobility depends upon the nature of the dopant and starts to decrease slowly with increasing temperature for phosphorus and boron concentrations up to 5×10^{19} at/cm³. In this temperature range and for those dopant concentrations where the barrier height is small, grain boundaries have only modest influence on electrical conduction [9]. Consequently, polysilicon behaves as monocrystalline silicon leading to the positive gradient in resistivity versus temperature. As a result, a self temperature compensated thermopile can be fabricated with judicious chosen dopants concentrations and species.

- 2) For sensors based on thermal principles involving a temperature gradient detection, Seebeck effect with semiconductor thermopiles has proved to be very useful. Polysilicon exhibits thermoelectric coefficients that considerably exceed the range of values obtained with commonly used metal thermocouples. Because of the weak database available on Seebeck coefficient, we endeavored to characterize our doped polysilicon films. The Seebeck effect cannot be measured directly in a single material for symmetry reasons, only relative coefficients can be experimentally determined. Thanks to the low Seebeck coefficient of gold ($2 \mu\text{V}/^\circ\text{C}$), Au/doped-polysilicon thermo-

couples thermoelectric power can be assimilated to doped polysilicon Seebeck coefficients. Fig. 3(a) and (b) shows that thermoelectric coefficients of boron and phosphorus doped polysilicon films increase linearly with temperature. Moreover, with those heavy dopants concentrations, the films exhibit large thermoelectric coefficients and low electrical resistivities. These very interesting results allow us to consider a new IR thermal sensor design with a large density of phosphorus and boron polysilicon thermocouples.

IV. CONCLUSION

Heavily doped boron and phosphorus LPCVD polysilicon films have been characterized in the temperature range of 293–373 K. Au/polysilicon thermopiles were fabricated in standard IC technology and test benches devoted to thermoelectric coefficient and relative resistance variations measurements have been developed. At room temperature and for the most heavily doped polysilicon thermopiles, thermoelectric coefficients values such as $196.3 \mu\text{V}/^\circ\text{C}$ for p-type and $154.5 \mu\text{V}/^\circ\text{C}$ for n-type were achieved that correspond to $350.8 \mu\text{V}/^\circ\text{C}$ for a thermocouple made up n- and p-type thermoelements. These results reveal interesting behaviors of thermopiles thermo-

electric coefficients and electrical resistances. Those data are very useful for modeling sensor sensitivity and temperature drift. A new improved IR thermal sensor using established characteristics will be available in the near future.

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Package-free infrared micro sensor using polysilicon thermopile

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Abstract

In this paper, a new IR thermal micro sensor using an original design and silicon micro technology is presented. The operating principle of the sensor is based on the Seebeck effect. A high thermoelectric power thermopile has been developed using thermoelectric properties of phosphorus and boron doped LPCVD polysilicon. Moreover, low stress membranes have been recessed under each hot and cold junction. The temperature gradient is maintained by increasing the thermal resistance under the thermocouples. A former study allows us to determine the Seebeck coefficients and relative resistance changes of phosphorus and boron LPCVD polysilicon layers within the temperature range of 293–373 K. The sensitivity values reached $72 \mu\text{V}/(\text{W}/\text{m}^2)$ for $5 \text{ mm} \times 5 \text{ mm}$ sensor with low influence to convection. This planar and symmetrical configuration requires no specific packaging, thus minimizing the manufacturing cost compared with existing realizations. The micro sensor is manufactured within the framework of a national project (CNRS-INTERLAB).

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Keywords: Packaging; Polysilicon; Thermopile; Membranes; IR micro sensor; NETD

1. Introduction

Infrared micro sensors are generally constituted of three functional parts. First, a radiative coating is used, which also selects the bandwidth. Next, there is a thermopile detector, which converts temperature differences into emf by the Seebeck effect, and finally, a substrate lying on a heat sink which stabilizes the temperature of the sensor. Using silicon technology, it is necessary to circumvent the high thermal conductivity of the silicon substrate. A classical solution consists of using micro-machining suspended structures, such as membranes or cantilevers. The hot junctions are gathered in the vicinity of an absorbent zone located on a membrane or a cantilever with low thermal conductivity minimizing the conduction heat losses. The cold junctions are located on a heat sink, generally the silicon substrate. These configurations lead to important thermal resistance between the hot and

cold junctions of the micro thermocouple (hence the high sensitivity). A variety of such thermoelectric sensors integrated on a silicon wafer and using polysilicon as thermopile have already been fabricated and commercialized [1–3]. However, the significant thermal dissimilarity between the two types of thermojunctions makes these sensors highly sensitive to gas conduction and convection phenomena. Their encapsulation is therefore of paramount importance [4,5].

Taking into account the advantages presented by the suspended structures, we have developed a new concept of IR micro sensors on membranes, which does not require any specific packaging [6]. The originality of this concept lies in the distribution of the hot and cold junctions, with each supported by a membrane (Fig. 1). Many technological solutions have been implemented to optimize the sensor sensitivity. A new photosensitive polyimide that presents interesting absorbent properties in the IR bandwidth and processing facilities is processed. Heavy phosphorus and boron doped polysilicon strips have been processed in order to achieve low resistivity and high Seebeck coefficient for the thermopile. Bi-layer low

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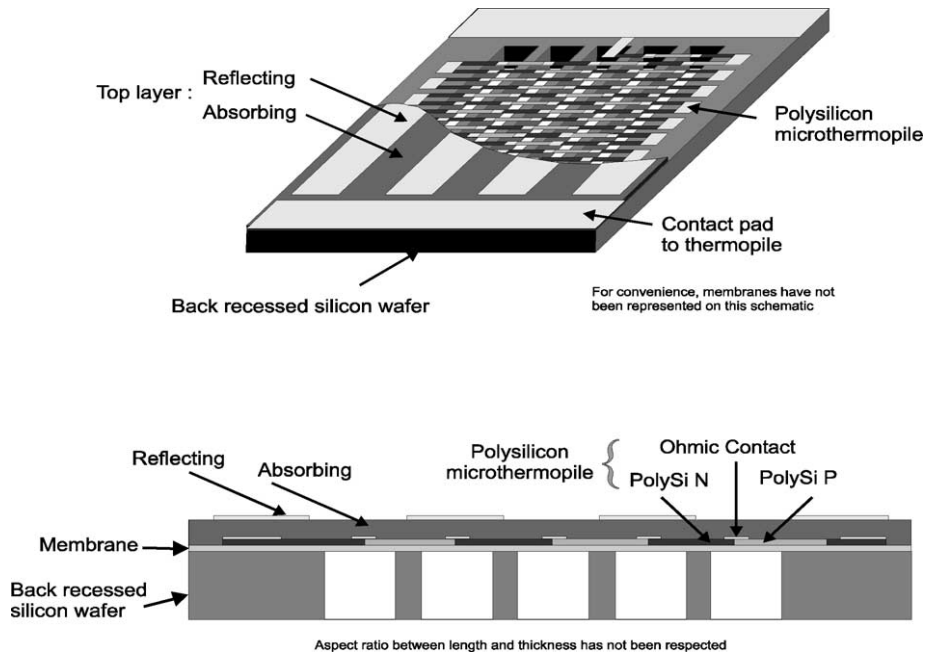


Fig. 1. Schematic of the unpackaged micro sensor (top: global view, bottom: cross section).

stress membranes have been realized to support hot and cold junctions by recessing the silicon substrate and then provide an important thermal resistance that strongly contributes to maintain a large temperature gradient.

2. Modeling

The heat transfer in such multiple periodic membrane devices can be modeled using a single membrane model under the assumption that each suspended structure is thermally independent. The portion of the sensor modeled here consists

of a membrane supported by two silicon pillars as shown in Fig. 2(a). A simple equivalent structure is represented in the same figure, where λ_{eq} is the equivalent thermal conductance of the membrane Fig. 2.

The thermal conductance for the reflecting zone is given by:

$$\lambda_{eq}e_t = \left(\lambda_1e_1 + \lambda_2e_2 + \lambda_3e_3 + \lambda_4e_4 + \lambda_5e_5 \frac{p}{w} \right) \quad (1)$$

where $\lambda_1, \lambda_2, \lambda_3, \lambda_4, \lambda_5$ and e_1, e_2, e_3, e_4, e_5 represent the thermal conductivities and the thicknesses of the SiO₂, SiN, polyimide and polysilicon layers. Also, e_t depicts the total

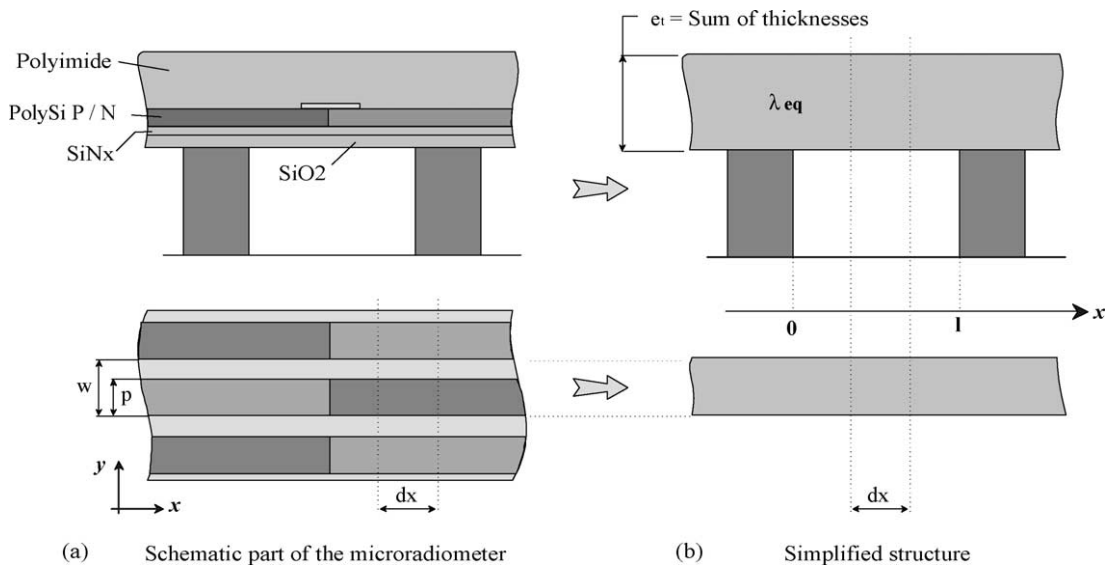


Fig. 2. (a) Cross section and top view of the sensor, (b) equivalent structure used for the modeling.

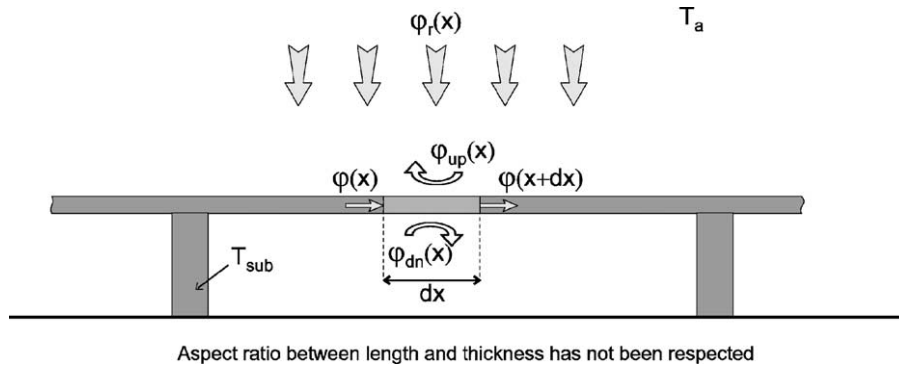


Fig. 3. Heat transfer in the equivalent structure and its surrounding.

thickness of the membrane, p the width of the polysilicon line and w the sum of p and the width of interline Fig. 2.

Bi-dimensional numerical modeling has shown that a one-dimensional treatment for heat conduction can be used. On the one hand, this can be justified by the high contrast of thermal conductivity between membrane and air layer (100:1). Alternatively, the very important aspect ratio between length and thickness of the membrane (1000:1) may validate this. Elsewhere, the high density of thermoelectric strips of high thermal conductivity allows us to neglect the temperature variations in the y -axis (Fig. 2). Three mechanisms of heat flow transfer: conduction, convection and radiation must be taken into account [7].

Considering the element, dx , on the equivalent single layer (Fig. 3), the heat balance can be expressed as:

$$\varphi(x + dx) = \varphi(x) - \varphi_{up}(x) - \varphi_{dn}(x) + \varphi_r(x) \quad (2)$$

where $\varphi(x)$ represents the conductive heat flow density circulating in the single layer, $\varphi_{up}(x)$ and $\varphi_{dn}(x)$ the convective heat flow densities exchanged with the environment and $\varphi_r(x)$ the net thermal flow density induced by IR radiation.

Using the Fourier law, Eq. (2) can be solved, resulting in the temperature across the membrane (of length l) to be expressed as indicated in Eq. (3).

$$T(x) = \left(T_{sub} + \frac{A}{\gamma^2} \right) \left[\text{ch}\gamma x - \text{th}\gamma \frac{1}{2} \text{sh}\gamma x \right] - \frac{A}{\gamma^2} \quad (3)$$

where γ^2 represents the propagation coefficient (Eq. (4)):

$$\gamma^2 = \frac{h + h'}{\lambda_{eq} e_t} \quad (4)$$

and

$$\frac{A}{\gamma^2} = \frac{hT_a + h'T_{sub} + \varphi_r}{h + h'} \quad (5)$$

Additionally, T_a and T_{sub} characterize the air and substrate temperatures, h symbolizes the convection coefficient above the membrane and h' below it.

By examining the above equation a maximum Seebeck voltage can be obtained when the hot and cold thermojunctions are located in the center of the absorbent and reflecting

zones. Consequently, the temperature difference between the hot and cold thermojunctions (subscripted 1 and 2, respectively) is:

$$\Delta T = \frac{h}{h + h'} (k_1 - k_2) (T_a - T_{sub}) + \frac{1}{h + h'} ((1 - k_1)\phi_{r1} - (1 - k_2)\phi_{r2}) \quad (6)$$

where k_1 and k_2 are the constants defined by the absorbent and reflective structures of respective length L_1 and L_2 (cf. expressions 7 and 8).

$$k_1 = \frac{1}{\text{ch}(\gamma_1(L_1/2))} \quad (7)$$

$$k_2 = \frac{1}{\text{ch}(\gamma_2(L_2/2))} \quad (8)$$

When the sensor is exposed to an IR radiation of irradiance E , and if the absorbent and reflective coatings (of respective absorptivities a_1 , a_2) are considered as gray bodies the net flows can be expressed by:

$$\varphi_{r1} = a_1(E - \sigma T_1^4) \quad (9)$$

$$\varphi_{r2} = a_2(E - \sigma T_2^4) \quad (10)$$

Again, in view of the small dimensions of these membranes, temperatures T_1 and T_2 (in K) will be similar to the average sensor temperature, T_s . Subsequently, the previous equations can be approximated by:

$$\varphi_{r1} = a_1(E - \sigma T_s^4) \quad (11)$$

$$\varphi_{r2} = a_2(E - \sigma T_s^4) \quad (12)$$

Then, the expression of the emf delivered by the micro sensor becomes:

$$V = N\alpha \left[\frac{h}{h + h'} (k_1 - k_2) (T_a - T_{sub}) + \frac{E - \sigma T_s^4}{h + h'} ((1 - k_1)a_1 - (1 - k_2)a_2) \right] \quad (13)$$

Table 1
Characterization results for the three sensors A, B, and C

	Active area (mm ²)	Number of membranes	Membrane length (μm)	Electrical resistance (kΩ)	Sensitivity S_E (μV/(W/m ²))	C_{T_a} (mV/K)	NETD at 300 K (mK)
A	5 × 5	5	970	398	72	2.8	0.18
B	5 × 5	4	635	500	47	1.5	0.32
C	3 × 3	3	220	93	17	0.9	0.38

From this equation, the performances of the sensors can be identified. The parameters of interest were the illumination sensitivity, S_E , the air temperature dependence coefficient, C_{T_a} and the noise equivalent temperature difference, NETD. Here, S_E is defined by:

$$S_E = \left(\frac{\partial V}{\partial E} \right)_{T_s, T_a, h, h' = \text{csts}} \quad (14)$$

Thus, Eq. (14) can be re-written in the form of Eq. (15) using Eq. (13):

$$S_E = \frac{N\alpha}{h + h'} [(1 - k_1)a_1 - (1 - k_2)a_2] \quad (15)$$

When the absorption law of the materials used to realize the radiative coating is known, the sensitivity in any spectral bandwidth (IR, UV) can be calculated from Eq. (15). The air temperature dependence coefficient is a parasite coefficient defined by:

$$C_{T_a} = \left(\frac{\partial V}{\partial T_a} \right)_{E, T_s, h, h' = \text{csts}} \quad (16)$$

or using Eq. (13):

$$C_{T_a} = N\alpha \frac{h}{h + h'} (k_2 - k_1) \quad (17)$$

The influence of this parasite coefficient appears only if the temperature of the air is different from the temperature of the sensor. Adjusting the length of the absorbent and reflecting membranes can nullify this term.

The noise equivalent temperature difference represents the lowest temperature detectable by the sensor. To account for the temperature variation of the target and the illumination we have introduced the following definition:

$$\text{NETD} = \frac{U_B}{S_{T_t}} = \frac{U_B}{4S_E\sigma_0 T_t^3} = \frac{\sqrt{4kT_s R \Delta F}}{4S_E\sigma_0 T_t^3} \quad (18)$$

where S_{T_t} represents the sensitivity of the sensor to the target temperature with T_t the target temperature, $k = 1.38 \times 10^{-23} \text{ J K}^{-1}$ the Boltzmann constant, R the electrical resistance and ΔF the bandwidth.

$$S_{T_t} = \left(\frac{\partial V}{\partial T_t} \right)_{T_s, T_a, h, h' = \text{csts}} \quad (19)$$

This model highlights the flexibility of the original structure that enables the disturbances to be minimized due to the unpackaged structure.¹ Parameters such absorptivity and

thermoelectric power have been characterized and introduced [8].

3. Device fabrication

Three types of microsensors (A, B, C) were manufactured while varying the number of membranes and active area (Table 1).

The fabrication of these micro sensors requires seven conventional photolithographic levels [8,9]. All fabrication stages have been carried out on a (1 1 0) 3 in., $380 \pm 25 \mu\text{m}$ thick silicon substrate. Due to its high thermal conductivity, the thickness of the silicon substrate is not critical (from a thermal perspective). However, the (1 1 0) crystallographic orientation enables both the micro-machining of vertical sidewalls and the patterning of a membrane that is of equal aperture to that of the mask. Such a process minimizes the micro-sensor area.

After careful cleaning of the substrate, the growth and deposition of the thin films for the membrane and the thermopile detector have been carried out. This constitutes the first functional part of the micro radiometer in the front end of the substrate. In order to achieve significant temperature differences at the tips of each micro thermocouple, the membrane that supports the micro thermopile must be fabricated with low thermal conductivities materials. Moreover, in order to prevent breaking after release, the stress of each layer must be under control. Following the growth of a $1.4 \mu\text{m}$ thermal silicon oxide (SiO_2), a $0.5 \mu\text{m}$ thick rich silicon LPCVD silicon nitride film SiN has been deposited. The thickness and composition of each thin film was carefully studied and optimized in the LAAS laboratory [10] to achieve a low stress bi-layer membrane. Next, both a $0.45 \mu\text{m}$ LPCVD polysilicon and a 20 nm LPCVD silicon nitride Si_3N_4 layer have been deposited. Once this first stage achieved, the micro thermopile consisting of polysilicon has been ion-implanted with boron ($1.10^{16} \text{ at/cm}^2$, 70 keV) and phosphorus ($1.10^{16} \text{ at/cm}^2$, 180 keV) through the silicon nitride, which was used as a cap layer to avoid dopant exodiffusion during the drive-in annealing (performed at 1100°C for 10 min).²

After annealing, the silicon nitride layer has been removed using phosphoric acid H_3PO_4 . A reactive ion etching step us-

² The ion implantation parameters have been optimized in a former study in order to achieve high thermoelectric power N/P doped polysilicon micro thermocouples [11–13].

¹ These inherently appear in unpackaged structures.

ing SF₆ gas has been performed, which resulted in S-shaped N/P-doped polysilicon strips, each having a 50 μm width and an inter-track space of 20 μm. Further, to obtain micro thermocouples composed of a p–n junction, Ti (20 nm)/Au (200 nm) ohmic contacts have been deposited using evaporation and lift off techniques.

The second functional part in the front end of the substrate is the radiative coating. An 18 μm photosensitive polyimide photo resist is spun on the substrate followed by annealing at 55 °C during 75 min in a convection furnace. This step enables part of the solvent to evaporate and makes the polyimide stiffer. Contact pads have been patterned by UV exposure and development.

A long polymerization annealing cycle followed, which made the polyimide insoluble and conferred to it its absorptive property. Rectangular areas of Au reflectors have been deposited by lift-off. Hot and cold thermojunctions were thus located under each absorbing and reflecting area. Finally, a reactive ion etching step using CF₄/CHF₃ gases was performed to pattern the membrane openings on the back-end mask, which was composed of initially deposited SiO₂/SiN thin films. Note that to increase the thermal resistance between the hot and cold zone, membranes have been recessed using thermostatic hydroxide potassium (KOH 40%, 80 °C). This resulted in a free-standing membrane structure. Micro sensors were released by little pressure. Finally, wires have been welded on the electrical contact pads to characterize the device.

4. Characterization results and prospects

Each micro sensor has been placed facing a radiation source composed of a plane thermostatic plate. It consisted of a copper plate (15 cm × 15 cm) that was recovered by a 0.97 emissivity thin film. The temperature is controlled using a plane resistor attached to the back and regulated by a PID. From the modeling, the voltage delivered by the sensor can be described by the following:

$$V = S_E(E - \sigma T_s^4) + C_{T_a}(T_a - T_{\text{sub}}) \quad (20)$$

In order to accurately determine S_E it is necessary to estimate the critical sensor-target distance from which the parasite signal (due to the air temperature) can be neglected, compared to the radiative signal E (W/m²). Indeed, a distance far from the target results in the temperature of the air to equal the temperature of the sensor.

The voltage delivered by each sensor was plotted against the distance target-sensor (Fig. 4). A shape factor F_{cp} representing a purely radiative balance between the target and the sensor, is superimposed. A significant change in the slope can be observed under a critical distance estimated to 3.5 cm. However, the sensor's response is purely radiative beyond this distance. That is why the sensitivity S_E is determined by measuring the voltage delivered by the sensor as a function of

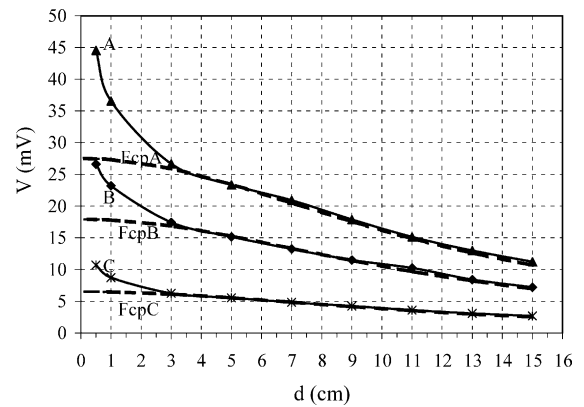


Fig. 4. Voltage delivered by the thermopile vs. source-sensor distance for sensors A, B, and C.

the power density E (W/m²) at a distance target-sensor equal to 5 cm. From the value of S_E the air temperature dependence coefficient C_{T_a} can be deduced and the noise equivalent temperature difference computed. The results are presented in Table 1.

Response time measurements have also been performed with a fast obturator disposed in front of the target. It appears that the device has a low responsive time of 75 ms compared with existing micro sensors [14,15]. This property can be improved by decreasing the membranes' aperture, yet the simulations show that a subsequent change will lead to a temperature gradient decrease, followed by a lower sensitivity. As a result, a trade-off exists, which depends on the targeted application.

Note that the parameter C_{T_a} has been evaluated for the characterized prototypes which had the same absorbent and reflecting membranes lengths. In the aim to produce optimized sensors with the dependence coefficient of air temperature cancelled out, these membranes lengths must be adjusted in order to obtain $k_1 = k_2$ (Eq. (17)). The model has been run with this condition to extract the evolution of the sensitivity to the illumination and the NETD with the number of membranes, as shown in Fig. 5. Absorbent and reflective membrane lengths are also displayed. The optimum number of membranes appears to be 5.

5. Conclusion and discussion

Using standard silicon technology high sensitivity planar 5 mm × 5 mm and 3 mm × 3 mm infrared micro sensors with an original design have been developed. High Seebeck coefficient doped polysilicon thermocouples have been used as thermopiles. The sensitivity has been predicted using a simplified model that includes dimension and material physical properties and for the best performing realized sensor the theoretical sensitivity is 68 μV/(W/m²), which is in good agreement with experimental results 72 μV/(W/m²). Optimized structures are proposed to be totally immune to the

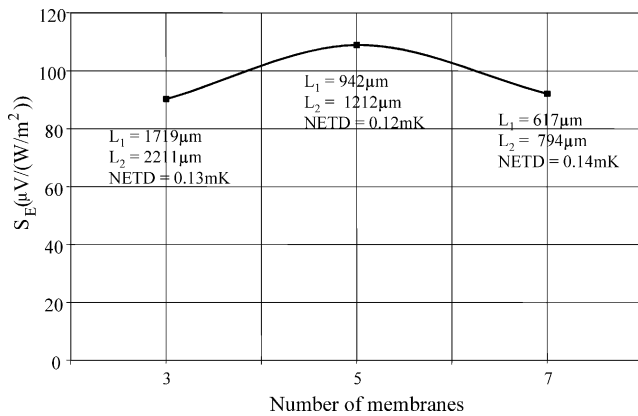


Fig. 5. Sensitivity and NETD vs. number of membranes for optimized micro sensors. L_1 and L_2 are the lengths of absorbent and reflecting areas, respectively.

air temperature with sensitivity reaching $110 \mu\text{V}/(\text{W}/\text{m}^2)$, which are at least twice more sensitive than commercialized sensors [14], but yet comparable to current state of the art sensors ($4 \text{ mm} \times 1.44 \text{ mm}$, $113 \mu\text{V}/(\text{W}/\text{m}^2)$), such as that achieved by [15]. These last sensors [14,15] are composed of a four-element chip mounted onto a sealed TO-39 or TO-5 package that also includes filters and filling gases (usually an inert atmosphere, such as Krypton, in order to enhance the device's performances). For applications where sensor location is a critical issue, the packaging proposed in this paper appears to be appropriate since it depends solely on the thickness of the sensor ($\sim 400 \mu\text{m}$) thanks to the distributed configuration of the detector and also the integration of the IR filter onto the substrate. The chip can be mounted on a single chip carrier without any specific encapsulation thus minimizing the volume occupied. Considering the cost and issues relative to MEMS packaging [16]. It is believed that the configuration proposed in this paper should be cost effective. In addition, micro power generation from external heat sources is a growing field for which such devices (contact sensors such as Heat flux meter and/or contact less sensors such as IR sensors) are now targeting [17].

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Biographies

Mohamed Boutchich received his PhD at Lille University (France), Institute of Electronic Microelectronic and Nanotechnology (IEMN) in 2002. He has been in charge of the design and fabrication of a new packaging for IR microsensor in silicon based technology for temperature measurement and thermal imaging applications. Since July 2003, he became a research associate in Cambridge University Engineering Department (CUED), working on the APOEM project: Active Packaging Optical Electronic Microsystems.

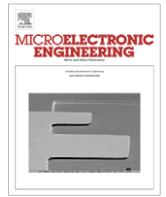
Katir Ziouche was born in Raimbeaucourt, France, in 1972. He joined the Institut d'Electronique, de Microelectronique et de Nanotechnologie in 1996 and received the PhD in electronics in 1999 from Lille University. He was appointed as a lecturer in electronics and electrical engineering at Lille Institute of Technology in 2000. He is in charge of the research and development of new processes for fabrication of thermal microsensors.

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Evaluation of layered tunnel barrier charge trapping devices for embedded non-volatile memories

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ABSTRACT

This paper presents experimental results on band gap engineered charge trapping devices for embedded non-volatile memories. Different material systems with high-*k* dielectrics and metal gates were fabricated using 193 nm lithography and the electrical evaluation was performed on 256 bits mini-arrays. The structure relies essentially on a layered tunnel ONO (oxide-nitride-oxide) barrier that replaces the tunnel oxide in conventional SONOS devices. In addition, we have implemented high-*k* dielectrics, metal gates and sealing layer in order to achieve low programming voltage and improve the data retention especially at elevated temperature. Whereas, high-*k* and metal gate systems allow low programme/erase voltages attractive for embedded non-volatile memories, the conventional band gap engineered SONOS (BE-SONOS) offers better high-temperature data retention. However, compared to a SONOS device with a standard “thick” tunnel oxide of 6 nm close to the EOT of the layered tunnel ONO barrier, it appears that BE-SONOS memories suffer from charge loss toward the channel and therefore we believe that the band gap engineered feature of the ONO barrier requires alternative materials.

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1. Introduction

The scaling perspectives of floating gate memory devices are being seriously challenged. Nowadays, this successful technology which has been a standard for decades is facing fundamental problems. The tunnel oxide thickness typically close to 8 nm cannot be scaled down to preserve the data retention. As a result, programming voltages remain high and the write/erase speed does not improve [1]. In addition, the reduction of the coupling ratio and cross talk interferences are compromising the future of embedded floating gate flash technology beyond 45 nm. The non-volatile memory arena has witnessed the rise of a number of alternatives to the floating gate concept ranging from evolutionary to revolutionary devices and materials [2,3]. While being under thorough investigation in academia as well as in the semiconductor industry, none of these potential candidates has yet emerged as the ideal replacement for floating gate. It appears that the performance (speed, endurance, retention at room and high-temperature) of these new concepts [4,5] does not yet fulfill the conditions required for various applications. Among these alternatives, the band gap engineered charge-trapping concept, proposed by Likharev [6] and further advanced by Macronix has shown promising performance [7–

9]. One of the major advantages of the charge trapping technology compared to floating gate is its immunity to the local defects in the tunnel oxide. Moreover, many studies proved performance gain thanks to the implementation of high-*k*/metal gates combinations [10–13]. On the other hand, reliability concerns such as read disturb, erase saturation and data retention have hindered the acceptance of charge trapping memories such as band gap engineered SONOS devices as a replacement to floating gate. Intensive theoretical as well as experimental efforts have permitted to overcome most of these challenges. However, bottlenecks especially in high-temperature data retention remain and new material systems must be investigated.

In this work, 256 bits NOR memory arrays of different band gap engineered mini-arrays were fabricated and tested with a custom made test vehicle and tester. The investigated structures are discussed with emphasis on the typical memory characteristics, i.e. program/erase (P/E) curves, endurance and data retention.

2. Band gap engineered structures

Beyond the 45 nm CMOS node, high-*k* dielectrics as well as metal gates are considered for the CMOS baseline fabrication process that could make them available for embedded integration. Among these materials, hafnium silicate (HfSiO_x) and hafnium aluminate (HfAlO_x) as well as aluminum oxide (Al₂O₃) with metal gates such

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as titanium nitride (TiN) are being considered as options [14,15]. In this work, we have assessed the potential of different material systems in combination with a band gap engineered silicon oxide/silicon nitride/silicon oxide (ONO) tunnel layer in an attempt to reduce the P/E voltage and improve the data retention.

Table 1 summarizes the devices fabricated for this study. In addition to the conventional BE-SONOS (band gap engineered silicon-oxide-silicon nitride-oxide-silicon) and BE-MANOS (band gap engineered metal-aluminum oxide-silicon nitride-oxide-silicon) introduced by Macronix [8–10], we have studied the potential of hafnium-based silicates and aluminate for the blocking oxide in combination with a HTO (High-Temperature Oxide) sealing layer (SL) and a metal gate. The purpose of the sealing layer is to increase the energy barrier seen by thermally excited electrons and therefore prevent the loss of electrons into the blocking oxide conduction bands during the write operation as well as during retention. Thanks to its wide band gap (9 eV), SiO₂ presents the appropriate offsets for both electrons and holes whereas high-*k* insulators have a narrower band gap than SiO₂. Moreover their band offsets are close to or even lower than the silicon nitride (Si₃N₄) conduction band. The sealing layer must be sufficiently thick to block direct tunneling.

3. Devices and technology

3.1. Overview

The mini-arrays presented in this work are conventional one transistor (1T) NOR arrays with memory transistors. The arrays contain 256 bits (transistors) integrated up to the metal1 level for the bit lines. The arrays are programmed and erased by direct tunneling of electrons/holes from the Si substrate. Threshold voltage (V_T) measurements are performed with 0.5 V applied on the selected bit line whereas the non-selected word and bit lines are grounded. The control gate voltage is automatically adjusted until a bit line current criterion of 5 μA is fulfilled.

3.2. Technology

The mini-arrays were fabricated using 193 nm DUV lithography for the active and gate definition. Four different structures were deposited. All have in common the layered ONO as well as 6 nm of Si₃N₄ storage medium deposited by low pressure chemical vapor deposition (LPCVD). The stacks differentiate by their blocking dielectric. After STI (shallow trench isolation) definition, the wafers are subjected to a cleaning operation. The layered ONO barrier is a

critical structure that required process development in order to achieve a closed film of 3 nm LPCVD Si₃N₄, Fig. 1. Subsequently, ISSG oxide (*in situ* steamed generated) is grown on the substrate followed by a dedicated clean operation in order to modify the nature of the ISSG from hydrophobic to hydrophilic. The 3 nm tunneling Si₃N₄ of the layered tunnel ONO barrier is then deposited by LPCVD at 700 °C. Finally, a 2.5 nm HTO oxide layer is deposited in an oven at 780 °C on top of the 3 nm Si₃N₄ to form the ONO barrier. The conventional BE-SONOS devices contain a 10 nm HTO oxide for the blocking dielectric. The high-*k* based memory transistors contain either hafnium silicate (HfSiO_x) with 47% Si deposited by metal organic chemical vapor deposition (MOCVD) and nitrated with an *in situ* ammonia NH₃ anneal [14,15], aluminum oxide (Al₂O₃) or hafnium aluminate (HfAlO_x) deposited by atomic layer deposition (ALD) and subsequently subjected to a post-deposition anneal in nitrogen N₂ atmosphere. The post-deposition anneal is particularly important for the Al₂O₃. In addition to the densification of the film and a shrink in thickness of approximately 2 nm, the conduction band offset of the Al₂O₃ increases upon crystallization, this property has a major impact on the performance of the Al₂O₃-based devices such as (tantalum nitride-aluminum oxide-

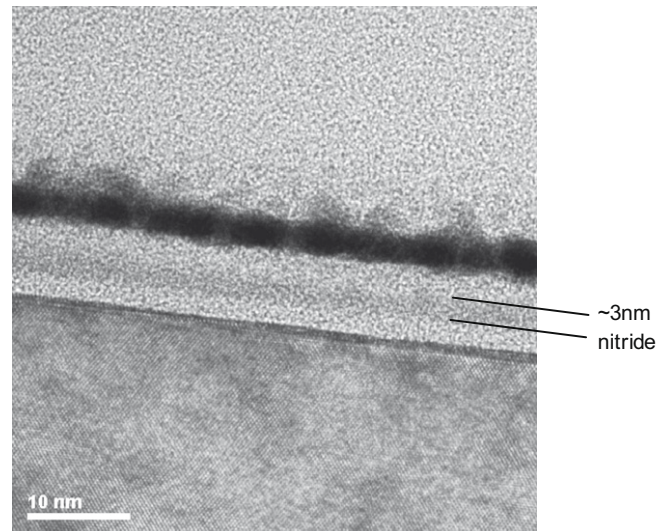


Fig. 1. TEM picture of the ultra-thin ONO barrier implemented in all band gap engineered splits. The contrast shows the 3 nm of Si₃N₄ between the tunnel ISSG oxide and the top HTO oxide of the barrier. Note that the black film has been added during the TEM sample preparation to enhance the contrast.

Table 1
Fabricated and studied band gap engineered devices. The ONO layered barrier and the trapping medium are common to all stacks.

Structure	BE-SONOS	BE-MANOS	BESHINOS with sealing layer	
Blocking dielectric and gate				
ONO layered barrier				

silicon nitride-oxide) TANOS [16]. The metal gate consists of MOCVD TiN, chosen for its favorable effective work function (eWF) with respect to the blocking dielectric, i.e. HfSiO_x , HfAlO_x and Al_2O_3 films (~ 4.7 eV). All gates are covered with 100 nm *n*-doped polysilicon followed by the standard SiN spacer formation and junctions' activation. After contact silicidation, and metal 1 (aluminum) patterning, the wafers are annealed in a forming gas mixture (H_2/N_2). Fig. 2 shows a TEM picture of a finished band gap engineered SONOS memory transistor. In parallel to the band gap engineered de-

vice, a SONOS device was fabricated with 6 nm of tunnel oxide, 6 nm of Si_3N_4 trapping medium and 10 nm of HTO blocking oxide.

4. Memory characteristics

4.1. P/E characteristics

Program and erase characteristics (P/E) are presented in Fig. 3a-d. The devices are initialized to the same erased/programmed state

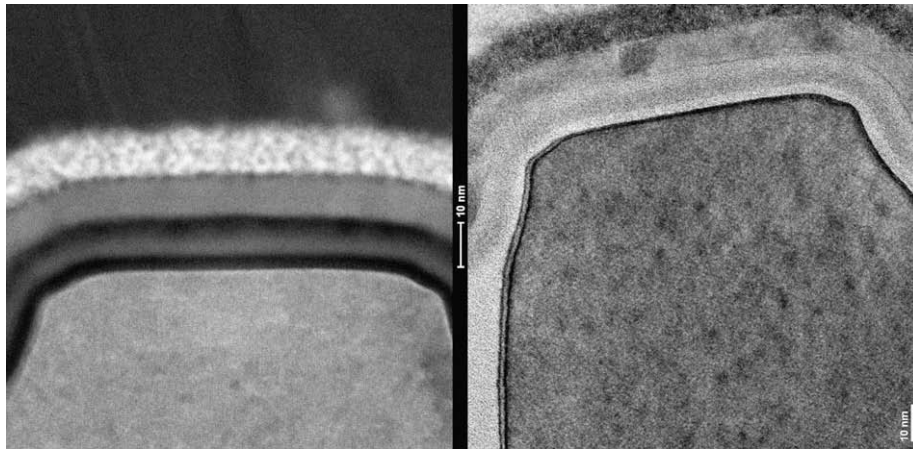


Fig. 2. TEM cross-section of a BE-SONOS stack after full integration. The stack is composed of the O(1.5 nm)/N(3 nm)/O(2.5 nm) layered barrier, 6 nm of trapping nitride, 10 nm of blocking silicon oxide and 10 nm of TiN metal gate capped with 100 nm of *n*-doped polysilicon.

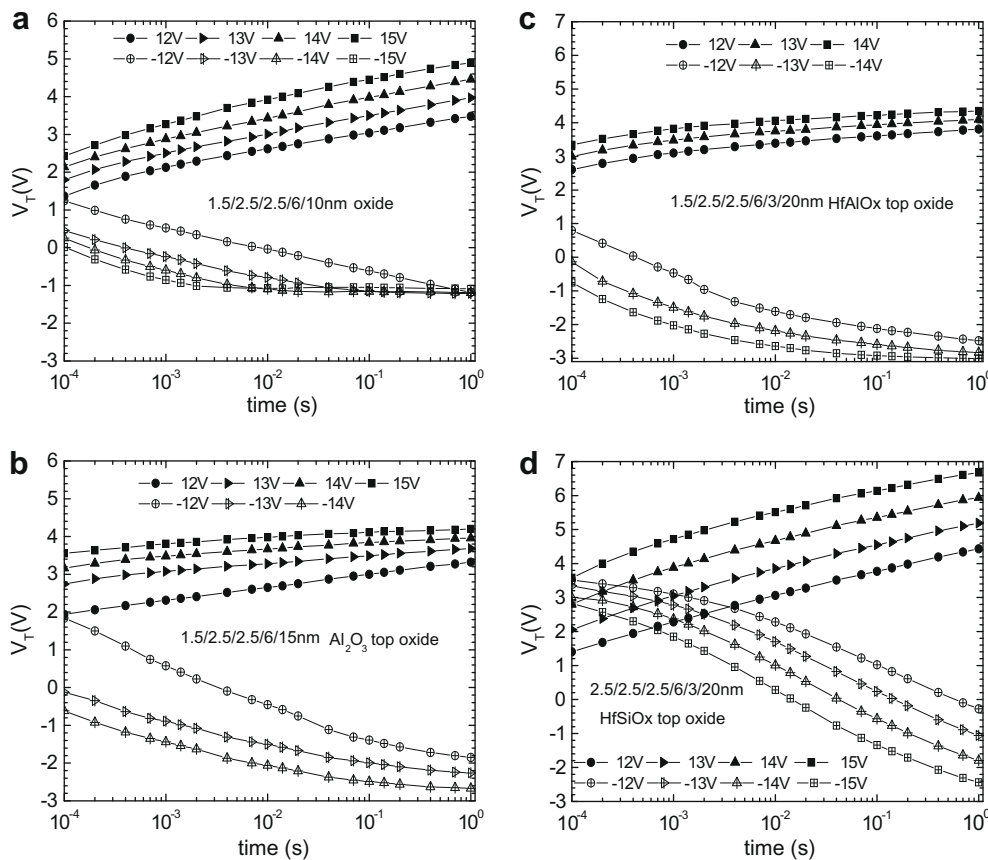


Fig. 3. Programme/erase curves of (a) BE-SONOS, the structure consists of the tunnel ONO (1.5/2.5/2.5 nm), a trapping layer 6 nm Si_3N_4 common to all structures and 10 nm of HTO blocking oxide. (b) BE-MANOS with (1.5/2.5/2.5 nm) ONO and Al_2O_3 as blocking oxide. (c) BE-SHINOS/HfAlO_x with 3 nm of HTO sealing layer and 20 nm of HfAlO_x as blocking oxide. (d) BE-SHINOS/HfSiO_x with 3 nm of HTO sealing layer and 20 nm of HfSiO_x as blocking oxide. For this latter the tunnel oxide (O1) was increased to 2.5 nm since devices with HfSiO_x material usually allow low programming voltage. The data acquisition was performed on non-cycled mini-arrays.

prior to measuring each P/E curve. For a given material system, all characteristics are acquired under the same conditions. Fig. 3a shows the P/E curves of BE-SONOS mini-arrays. The neutral threshold voltage (V_T) of this structure is approximately 1.0 V. The P/E voltages are chosen to be at most equal to current embedded flash voltages i.e. ± 15 V. BE-SONOS devices can be programmed with voltages ranging from +12 to +15 V reaching a maximum V_T of 2–4 V with pulses up to 10 ms long. On the other hand, erase saturation at approximately -1 V appears already at -13 V. Note that the erase saturation can be postponed to lower V_T level using depletion implants. This option has not been implemented here [10,13].

Fig. 3b shows the P/E curves of BE-MANOS mini-arrays. The neutral threshold voltage (V_T) is approximately 1.4 V. It is possible to achieve a 5 V window with ± 13 V/10 ms; such low voltage is interesting as it is below current voltages used in floating gate flash devices although the programming time is typically in the μ s range for flash. In addition, this structure exhibits a good resistance to erase saturation. The phenomenon appears for voltages beyond -14 V and more than 100 ms erasing time. This low erase saturation level is related to the SiN/Al₂O₃/TiN interface as for TANOS [16,17]. However as for BE-SONOS, the V_T versus V_{gate} characteristic remains poor. Fig. 3c and d shows the P/E curves of BE-SHINOS mini-arrays using HfAlO_x or HfSiO_x as a blocking dielectric. In these two systems, the dielectric is combined with a 3 nm HTO sealing layer to increase the energy barrier. Both HfAlO_x as well as HfSiO_x structures exhibit large programming windows. However, the HfSiO_x is more appealing owing to the lower EOT provided by the high- k material of the device despite a high neutral threshold voltage (V_T) ~ 2.3 V. The major feature is its apparent immunity to erase saturation. The phenomenon does not appear even for pulse width as large as 1 s. Mini-arrays can be programmed with voltages ranging from +12 to +15 V reaching a maximum V_T of

6 V for the programming and down to -2 V for the erase. A 6 V window is readily achievable with +14 V/15 ms and -14 V/100 ms. The resistance to erase saturation of this system is attributed to the 3 nm HTO oxide sealing layer inserted between the Si₃N₄ trapping layer and the top HfSiO_x blocking oxide. The extra energy barrier reduces the electron flow and hence postpones both program and erase saturation to much higher and lower V_T , respectively.

4.2. Endurance

Fig. 4a–d represents the endurance curves of the mini-arrays of systems BE-SONOS, BE-MANOS and BE-SHINOS. The programmed and erased V_T start to shift upward after 10^4 P/E cycles indicating that negatives charges are trapped in the stack or at an interface. The fact that all traces exhibit quasi-identical features indicates that the origin may be unique and it is possible that these negative charges are trapped within the ultra-thin nitride of the layered tunnel ONO barrier because previous SONOS experiments with tunnel oxide thicknesses between 1.5 and 2.5 nm did not show such degradation. However, the programming windows obtained are not affected by the V_T walk-out observed. The read voltage can be chosen in the middle of the window with no risk of crossing the programmed or the erased V_T trace. Interestingly, BE-MANOS (Al₂O₃ blocking dielectric) splits present a V_T window symmetrical around 0 V. This means that the read voltage can be chosen as low as 0 V, eliminating any risk of read disturb.

4.3. Data retention

Data retention is the bottleneck that precludes the wide acceptance of charge-trapping memories as a replacement to floating gate devices especially in high-end applications. Note that to avoid

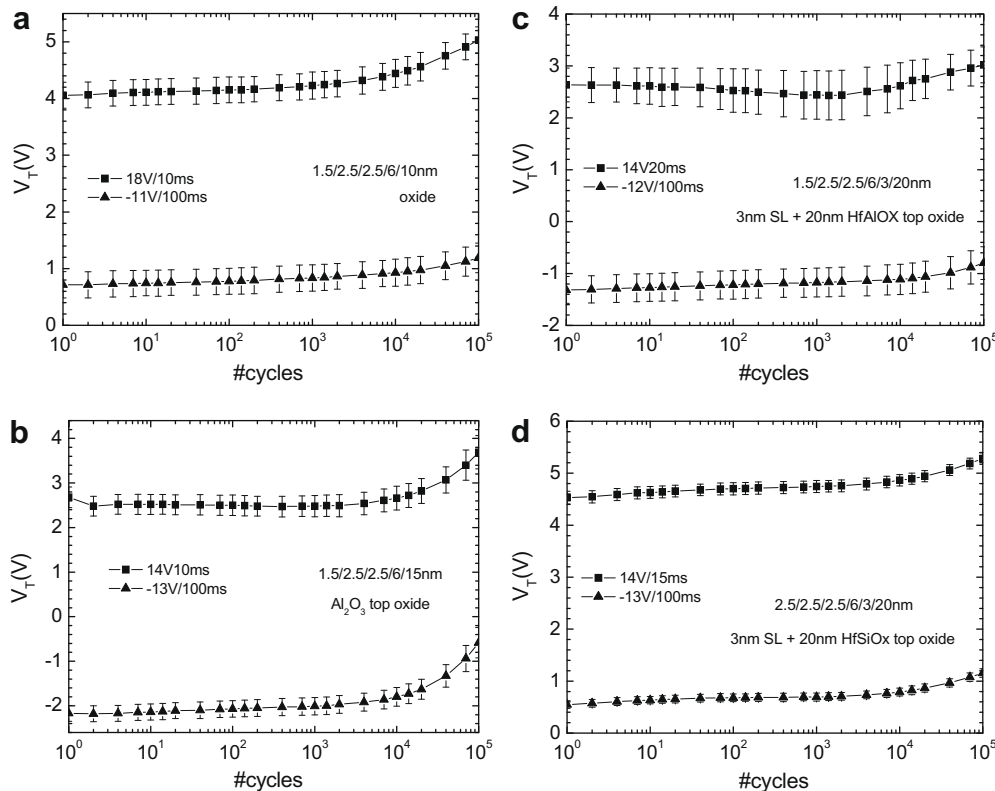


Fig. 4. Endurance characteristics of the four structures investigated. The light walk-out observed in all traces indicates that there is minor degradation of the stack and the origin maybe regardless of the structure.

hasty conclusions, data retention measurements should systematically be performed for a minimum of 24 h at room temperature. At elevated temperature, the test should be carried out for more than 24 h as thermal discharge could be balanced by the direct tunneling of charges and may only appear after a long period of time [18]. Fig. 5a–d displays the data retention of non-cycled mini-arrays at room temperature. All measurements were performed for a minimum of 24 h and extrapolated to 10 years. The devices were not cycled to capture the intrinsic behavior of the stacks. P/E parameters were set in order to avoid erase saturation as well as to achieve at least a 3 V initial window. Note that since the depletion implant scheme was not implemented, the neutral V_T of these devices is relatively high, 1, 1.4, 0.9 and 2.3 V for BE-SONOS, BE-MANOS, BE-SHINOS/HfAlO_x and BE-SHINOS/HfSiO_x, respectively. This explains the steepness of the erased states especially for BE-MANOS and BE-SHINOS. On top of each plot, the trace of 2.2 nm tunnel oxide SONOS mini-array retention was superimposed for comparison. All high- k based structures present a decay rate for the programmed state very similar to standard 2.2 nm SONOS. Moreover, since the erased states are well below the neutral V_T , the slope is steeper. As a result, BE-MANOS and BE-SHINOS, Fig. 5b–d, exhibit remaining windows extrapolated to 10 years comparable or smaller than the SONOS reference see Fig. 5b–d. The only advantage is the possibility to erase below the neutral V_T as opposed to SONOS. On the other hand, BE-SONOS mini-arrays present a slower decay rate compared to SONOS. However, to achieve a 3 V initial window, the device must be programmed with +18 V/10 ms that is 3 V beyond voltages used in current embedded flash memories. In embedded applications, voltage scaling is as important as size scaling, the periphery to generate these 18 V would be too large and power consuming. After write and erase pulse, the BE-SONOS device loses about 30% of its programming window in a matter of seconds. This explains why we had to resort to such a high programming voltage in order to secure a 3 V start-

ing V_T window for the data retention measurements Fig. 6. At room temperature, the BESONOS, Fig. 5a seems to be the only structure providing an advantage compared to standard SONOS in terms of data retention. It has comparable retention and has the ability to erase slightly below the neutral V_T . Yet, the extrapolated remaining V_T window is small, ~ 1 V. All high- k -based structures suffer from the poor interfaces at the SiN/top dielectric interface, Fig. 5b–d. The 3 nm SiO₂ sealing layers implemented in BE-SHINOS devices do not improve the data retention as expected and therefore top losses remain a major contributor to the decay.

Fig. 7 shows the data retention curves of the BE-SONOS structure at elevated temperature. The 100 and 150 °C curve superimposes for few days indicating the same discharge mechanism. However, after 1 week measurements, the 150 °C trace sharply drops leading

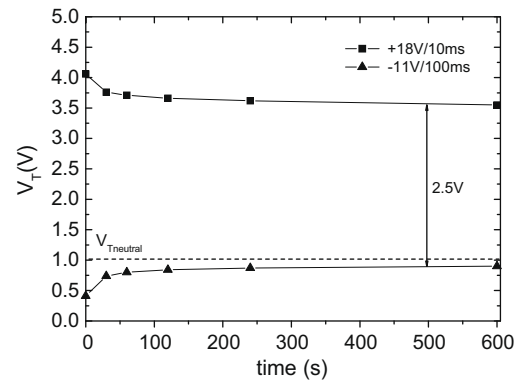


Fig. 6. Room temperature data retention characteristics of the four structures investigated. Measurements have been performed for a minimum of 24 h. The remaining window is extrapolated to 10 years specification. A standard SONOS characteristic was added on each plot for comparison. The data acquisition was performed on non-cycled mini-arrays.

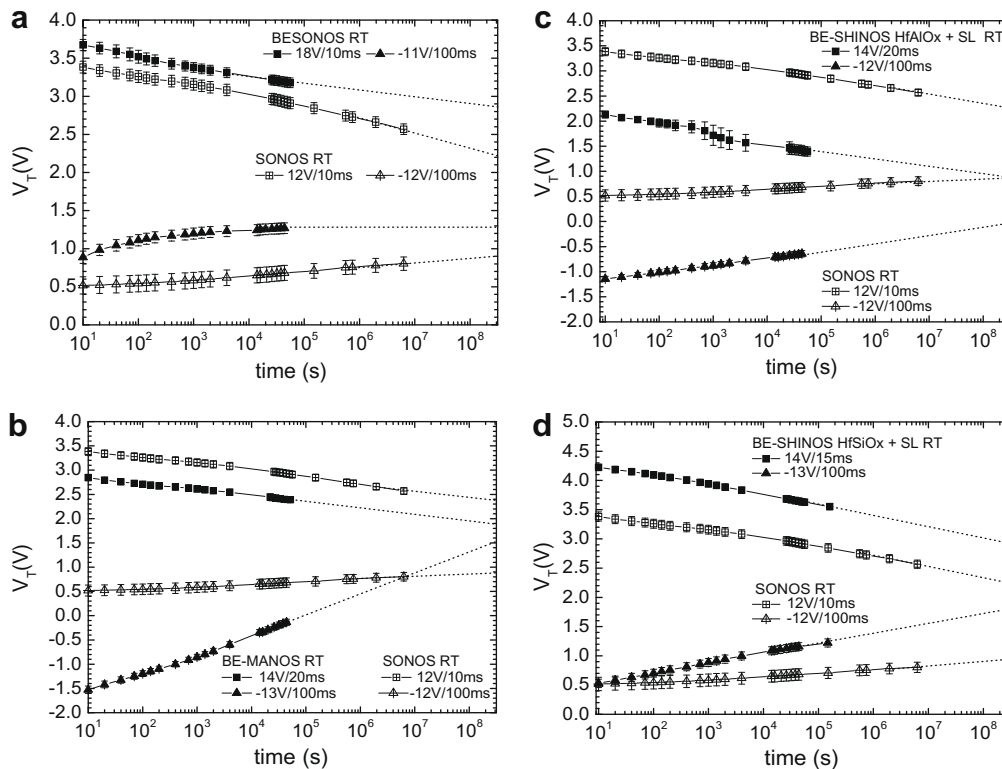


Fig. 5. Evolution of the programming and erased threshold voltage with time after a +18 V/10 ms and -11 V/100 ms pulses. A 30% loss is readily observable 10 min after the write/erase operation.

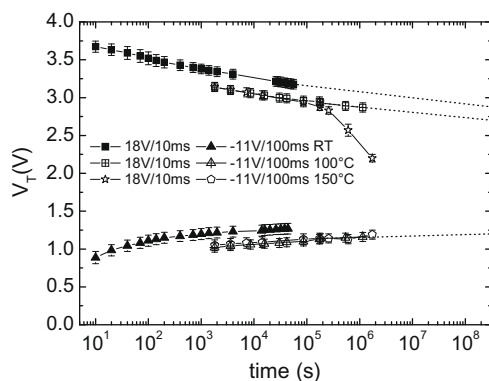


Fig. 7. Data retention measurements of a non-cycled BE-SONOS mini-array at room temperature, 100 and 150 °C. The traces exhibit the same decay rate up to a week beyond this point 150 °C devices start to decay sharply.

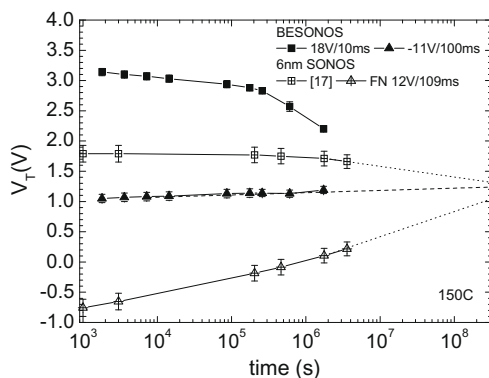


Fig. 8. Data retention at 150 °C of BE-SONOS mini-array compared with a 6 nm thick tunnel oxide SONOS device. The data acquisition was performed on non-cycled devices. BE-SONOS mini-array shows a window closure before the 10 years specification whereas SONOS devices exhibit 0.4 mV remaining window extrapolated to 10 years.

to an extrapolated window closure well before the 10 years specification. Fig. 8 compares this latter with a 6 nm thick tunnel oxide SONOS mini-array that was fabricated in parallel using a similar integration scheme. The tunnel ONO of BE-SONOS corresponds to a ~ 6 nm EOT hence this comparison. Note that for the thick tunnel oxide SONOS, one must resort to alternative hot carrier programming mechanism (e.g. [19]) as it is not possible to erase the memory using Fowler–Nordheim or direct tunneling. For a comparable initial V_T window, the BE-SONOS device presents a smaller remaining window as opposed to thick tunnel oxide SONOS, a sharp drop on logarithmic scale occurs in the programmed states after a month of measurements at 150 °C. In this comparison, the blocking dielectric is identical i.e. 10 nm of SiO_2 , therefore the discharge must occur through the band gap engineered ONO layer.

5. Conclusion

In this paper, four band gap engineered charge trapping structures were evaluated for low-power embedded non-volatile memory applications. However, due to the high voltage required to achieve a reasonable programming window, we have extended the study to implement high- k and metal gates as well as sealing layers in order to evaluate the potential of such concept for embedded low-power applications. The programming windows achieved

are much larger with BE-SHINOS structures. However, the programming efficiency is rather poor considering the V_T/V_{gate} ratio. The endurance curves are very much comparable whatever the top dielectric indicating that no major degradation occurs during cycling. In addition, the light walk-out observed is not detrimental for the read operation. The data retention measurements at room and elevated temperature revealed that the best structure remains the BE-SONOS with oxide as a top dielectric. BE-SONOS exhibits a 1 V remaining V_T window extrapolated at 10 years at 100 °C and is therefore competitive with charge trapping structure such as TANOS with the major advantage of not requiring any high- k and metal gate integration. However, at 150 °C the data retention is still poor and a thick tunnel oxide SONOS would perform better [9]. Although the materials utilized for BE-SONOS remain standard and reliable, the large voltages required to achieve a reasonable initial V_T window exclude this concept for low-power embedded non-volatile memory. The comparison of a BE-SONOS with a thick tunnel oxide SONOS shows that the data loss occurs through the band gap engineered ONO layer.

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Amorphous silicon diamond based heterojunctions with high rectification ratio

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ABSTRACT

We have fabricated and characterized diamond based heterojunctions composed of homoepitaxial diamond (B-doped film: *p* type) and hydrogenated amorphous silicon (a-Si:H film: *n*-type). All devices include an intrinsic amorphous silicon interface (i-a-Si:H). (*J*-*V*) characteristics of a-Si:H heterojunctions measured from 300 K to 460 K present a very high rectification ratio (in the range 10^8 – 10^9) and a current density of 10 mA/cm² under 2 V of forward bias. The reverse current up to -4 V is below the detection limit in the whole temperature range. The devices present two regimes of operation indicating that more than one mechanism governs the carrier transport. These characteristics are compared with a Schottky barrier diode (SBD) using a tungsten carbide metal on top of the *p*-type diamond as a Schottky contact. The SBD device exhibits *J*-*V* characteristic with an ideality factor *n* close to one and the heterojunction follows this trend for low bias voltages whereas for bias voltage above 1 V a second regime with larger ideality factors *n*~3.6 is observed. These results point out the prominent role of transport mechanisms at heterointerface between the a-Si:H layers and the *p*-type doped diamond which degrades the current injection. The breakdown voltage reached -160 V indicating the good quality of the deposited layers.

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1. Introduction

Despite the tremendous challenges to overcome for its synthesis and doping [1], diamond remains an attractive wide band gap semiconductor (5.5 eV) for a range of electronic devices [2] especially those requiring high power and operating in harsh environment (temperature, radiations) [3]. Amongst the concepts that raised a lot of interest are Schottky-barrier diodes (SBD) [4], Schottky-barrier Photodiode (SPD) [5,6] as well as *pn* [7] and *p-i-n* junction (PND) with (N)-doped diamond [8]. The development of reliable bipolar devices is a key technological building block for the design and fabrication of electronic devices. For that purpose, it is necessary to obtain device-grade quality for the *n* as well as the *p*-type diamond. Although a lot of efforts have been devoted to incorporate donor atoms such as (P)-Phosphorus or (As)-Arsenic [9,10] into semiconductor diamond, the resistivity as well as junction characteristics such as built-in voltage and rectification ratio remain too poor to envision competitive device performance. In addition, increasing the donor concentration beyond a certain level has proven to be detrimental to the diamond film integrity. The aforementioned technological issues to fabricate bipolar devices on diamond homojunctions have raised

interest into the study of heterojunction with semiconductor materials such as amorphous silicon (a-Si:H) or recently with Aluminum nitride (AlN) [11] or Zinc Oxide (ZnO) [12]. Such a structure combines the properties of both semiconductors and may lead to outstanding performance in terms of rectification ratio. Moreover, if fabricated with transparent electrodes, *pn* and/or *p-i-n* diamond based heterojunctions [13,14] find applications in photo detection as well as light emitting diodes.

In this work, we have fabricated *p-i-n* diodes based on the heterojunction of *p*-type diamond and amorphous and microcrystalline silicon films. We mainly focused on the diamond/a-Si:H structure for which we measured the dark current density–voltage (*J*-*V*) characteristics as well as capacitance–voltage (*C*-*V*) characteristics versus temperature. From these measurements, we identified two regimes of operation and extracted the ideality factor *n*. The heterojunction has been pushed to breakdown and through modelling we estimated the electrical breakdown field in each material.

2. Experimental

The *p*-diamond epilayers were homoepitaxially grown by MPCVD (Microwave Plasma Chemical Vapor Deposition) on heavily B-doped *p*-diamond (100) $2.5 \times 2.5 \times 0.5$ mm³ substrates commercially available. The B concentration ([B]) measured by secondary ion mass spectroscopy (SIMS) is estimated to be close to 1×10^{20} cm⁻³

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[15]. The diamond epilayers were grown by the dissociation of CH_4 and H_2 gas precursors. The B species inside the MPCVD chamber were incorporated into the diamond epilayer with a concentration ranging from 10^{15} to 10^{16} cm^{-3} . The ratio of CH_4 to H_2 was 0.08%, and the corresponding flow rates of CH_4 and H_2 were 0.4 and 500 sccm, respectively. The reactor pressure was fixed at 106 hPa during growth. The growth was performed at $\sim 800^\circ\text{C}$. 500 nm of diamond epilayer was deposited using these process parameters. Following the diamond growth, the samples were oxidized for 1 h in a boiling acid solution of $\text{H}_2\text{SO}_4/\text{HNO}_3$ (1:1) to remove the surface conductive hydrogenated layer and introduced in a standard RF glow discharge reactor for the amorphous and microcrystalline silicon deposition. Hydrogenated amorphous silicon and microcrystalline silicon layers were deposited at 175°C on these substrates by plasma enhanced chemical vapour deposition [16]. A 30 s hydrogen plasma treatment of the p-type diamond epi layer was performed just before the deposition of a 50 nm intrinsic a-Si:H from the dissociation of pure silane at 7 Pa under an RF power of 5 mW/cm^2 . After the intrinsic a-Si:H we deposited 50 nm thick n-type amorphous or microcrystalline silicon films by adding phosphine to silane in the case of n + a-Si:H layers and using a high dilution of silane and phosphine in hydrogen to achieve $\mu\text{c-Si:H}$ growth. Fig. 1 shows the Raman spectra with the typical features centered at 480 cm^{-1} and 520 cm^{-1} for the a-Si:H and $\mu\text{c-Si:H}$ films, respectively, on top of the epitaxial diamond layer. This measurement shows that the silicon based film can be grown on diamond substrates with no detrimental impact on their microstructure.

The thickness and optical properties of the layers $\sim 50 \text{ nm}$ each were determined from ellipsometry measurements on samples co-deposited on Corning glass substrates with nm accuracy. Four aluminium (Al) based Ohmic contacts were then deposited by evaporation. The last stage of the fabrication process consisted of a reactive ion etching (RIE) step with SF_6/O_2 mixture in order to isolate the devices in MESA structures of $500 \mu\text{m} \times 500 \mu\text{m}$ contact. This area was chosen in order to secure the positioning of the measuring probe. Owing to the high conductivity of the diamond substrate, the backside of the device was stuck with conductive paste directly onto metal leads. Both contacts were connected using measurement probes positioned in the characterization set-up. Fig. 2 shows a schematic cross-section of the devices. The current–voltage (J – V) characteristics were acquired via a Keithley 617 electrometer and capacitance–voltage (C – V) characteristics were measured using frequency dependent Agilent E4980A LCR meter with 0.01 V and 0.01 pF accuracy respectively. The sample was connected to two probes and embedded in a temperature controlled cryostat. All measurements were carried out under vacuum and for temperatures in the range from 300 K up to 460 K. Temperature stability was better than 0.1 K.

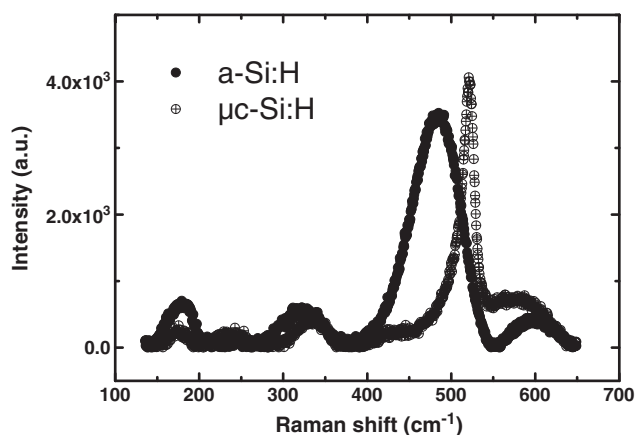


Fig. 1. Raman spectra of a-Si:H and $\mu\text{c-Si:H}$ deposited on diamond.

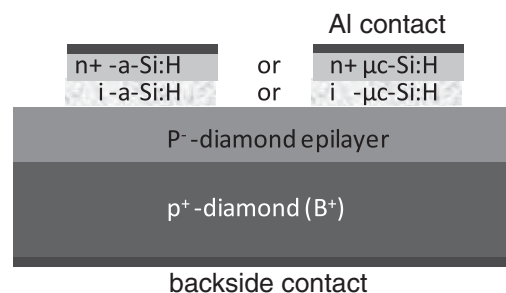


Fig. 2. Schematic description of the diamond based heterojunction (cross section).

3. Results

The J – V characteristics (not shown) of the diamond based heterojunctions were measured at room temperature for both diamond/n + microcrystalline silicon and diamond/n + amorphous silicon heterojunction. The microcrystalline based heterojunction presents a rather high reverse current as compared to the amorphous based device. In addition, most of the microcrystalline silicon based devices were not exploitable because of the blistering that appeared during film growth, resulting in a severe damage of the microcrystalline silicon layer. Therefore, the following results and discussion are only related to the diamond/i-a-Si:H/n + a-Si:H heterojunctions. Fig. 3 shows the $1/C^2$ plots measured from 300 K to 460 K at 10 kHz. From these measurements, we determine the doping concentration as well as the built-in voltage by fitting these traces. The calculated space charge density is equal to $5.7 \times 10^{15} \text{ at/cm}^3$ in agreement with the doping concentration of the p^- diamond film deposited for this experiment. The built-in voltage (V_{bi}) corresponding to the intercept with the abscissa varies with temperature from 2.01 V at 300 K to 1.7 V at 460 K consistent with the variation of the turn-on voltage observed in the J – V characteristics. We utilized numerical simulation tool ATLAS 2-D software to determine the extension of the space charge region and the energy band diagram [17]. The geometrical and material parameters were chosen in agreement with our fabrication process. The whole diamond layer is readily depleted at -2.5 V reverse bias. The experimental space charge region is estimated around 570 nm which correspond approximately to the thicknesses of the epi diamond and the intrinsic a-Si:H. Fig. 4 shows the current–voltage characteristics (J – V) of the heterojunction diodes in semi-logarithmic scale. The reverse current is below the detection limit up to 440 K, a small increase is observed above this temperature.

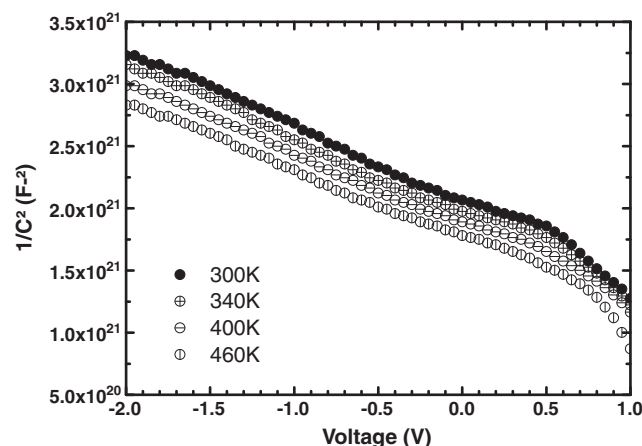


Fig. 3. Mott–Schottky plots of $1/C^2$ versus voltage deduced from capacitance–voltage measurements at various temperatures. of the slope of the linear zone determines the space charge density whereas the intercept with the abscissa gives the built-in voltage V_{bi} .

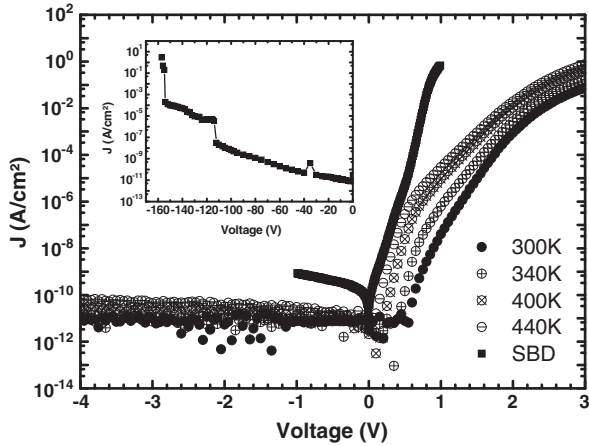


Fig. 4. Current–voltage characteristic of a diamond/a-Si:H/n + a-Si:H heterojunction versus temperature. The SBD characteristic, measured at room temperature, is shown for comparison. The inset shows the reverse current versus voltage until breakdown at -160 V at 300 K.

The heterojunction diodes exhibit a pronounced rectifying behaviour (up to 10^9 or more) for a current density of 10 mA/cm² at $+2$ V bias.

A SBD (0.79 mm²) device fabricated on the same diamond sample has been characterized and its characteristic is also shown in Fig. 4. This device was fabricated using a semi-transparent tungsten carbide (WC) Schottky contact electrode for Deep UV application [15]. Its characteristic exhibits an ideality factor n equal to 1.1 and a barrier height of 1.42 eV. The inset of Fig. 4 shows the electrical breakdown of the diamond/a-Si:H heterojunction. Breakdown occurs at -160 V indicating the good quality of the films.

4. Discussion

The estimated depletion zone obtained from the simulations is consistent with the C – V measurements and confirm that the depletion zone extend in the entire epi diamond layer. Note that the capacitance variation with temperature is small and the slope of the $1/C^2$ plots exhibits little variation. This result shows that the doping concentration is constant with temperature and therefore most of the boron atoms are already fully ionized at room temperature.

The dark current in a Schottky diode device can be expressed as:

$$J = J_0(T) \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right]$$

Where $J_0(T)$ is the saturation current density defined by:

$$J_0(T) = AA^*T^2 \exp\left(-\frac{q\phi_b}{kT}\right)$$

V is the applied voltage at the junction, k is the Boltzmann constant, n the ideality factor, T the absolute temperature, A the contact area and A^* the Richardson constant equal to 96 A/cm²·K² taking the hole effective mass of $0.8 m_0$. The magnitude of the ideality factor n and the variation of $J_0(T)$ as a function of temperature provide information on the carrier transport mechanism. From Fig. 4, it is possible to distinguish 2 regimes of operation indicating the presence of different transport mechanisms. For very low bias i.e. $0 < V < 1$ V, the characteristic of the heterojunction with temperature follows the SBD's model and therefore presents a similar ideality factor $n \sim 1.1$. However, for the second regime of operation i.e. $1 < V < 2.5$ V, n is much larger than the value of 2 expected from the Sah–Noyce–Shockley theory [18]. In this regime, n reaches 3.6 and remains approximately constant with temperature. This observation is in contradiction with

the trend observed in other heterojunctions where n decreases with increasing temperature [19,20]. Such an anomalous n value indicates that the current is not limited by drift nor by diffusion, but gives evidence of the presence of alternative transport mechanisms such as space charge limited current (SCLC). Note that, the heterojunction exhibits a reverse current two orders of magnitude lower than the SBD demonstrating the remarkable blocking property of the intrinsic a-Si:H layer. The excess reverse current observed in the SBD is presumably due to the barrier inhomogeneities between the diamond and the WC contact.

Fig. 5 shows a $\text{Log}J$ – $\text{Log}V$ plot of the current density versus the voltage in the second bias region versus temperature. In this bias range, the J – V characteristic is well described by a space charge limited current (SCLC) transport mechanism and follows a power law:

$$J = KV^m$$

Where K is a constant dependent on the trap distribution [21]. The power factor m also characteristic of the trap distribution varies from 14.9 at 300 K to 9.8 at 440 K with a fitting error better than 0.04. It is agreed that for $m > 2$ the conduction is controlled by deep energy states. These parameters are related to the defects distribution but the variation and the magnitude of m cannot be over interpreted at this stage as the traps in a-Si:H are both modelled by exponential as well as Gaussian distributions. The determination of the exact fitting parameters is beyond the scope of this paper.

To illustrate the transport within the heterojunction, we use the energy band diagram depicted in Fig. 6. The experimental parameters introduced are: $E_{g\text{diam}} = 5.5$ eV, an electronic affinity $q\chi_{\text{diam}} = 0.5$ eV and the energy level of acceptor states $E_A - E_V = 0.37$ eV in B-doped diamond. The intrinsic a-Si:H is modeled with a band gap $E_{g\text{a-Si:H}} = 1.7$ eV and a $q\chi_{\text{a-Si:H}} = 3.8$ eV. The n + a-Si:H is similar to the intrinsic a-Si:H but adding the energy level of donor states $E_C - E_D = 0.25$ eV. The density of states (DOS) in the a-Si:H consists of two exponential band tails with characteristic energies kT_C and kT_V of 0.03 and 0.05 eV for the conduction and the valence band, respectively, with a pre-exponential factor of 4×10^{21} cm⁻³ eV⁻¹ completed with two Gaussian deep defect distributions of donors and acceptors with a maximum value 2×10^{19} cm⁻³ eV⁻¹ and a standard deviation of 0.21 eV. The diamond/i a-Si:H interface presents a large conduction band offset ΔE_C as opposed to the valence band offset ΔE_V preventing electron's transfer. Simulations confirm this latest assumption even at high bias. As a result, the conduction within this heterojunction is essentially due to holes in the valence band and the aforementioned mechanisms would occur at the valence bands interface between

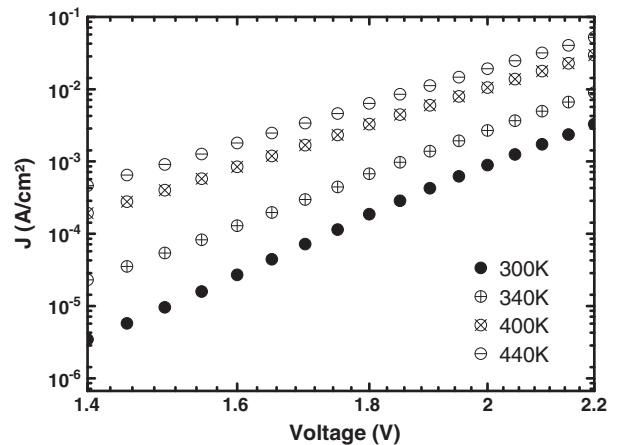


Fig. 5. Current–voltage characteristics in log–log scale for the diamond/a-Si:H/n + a-Si:H heterojunction versus temperature.

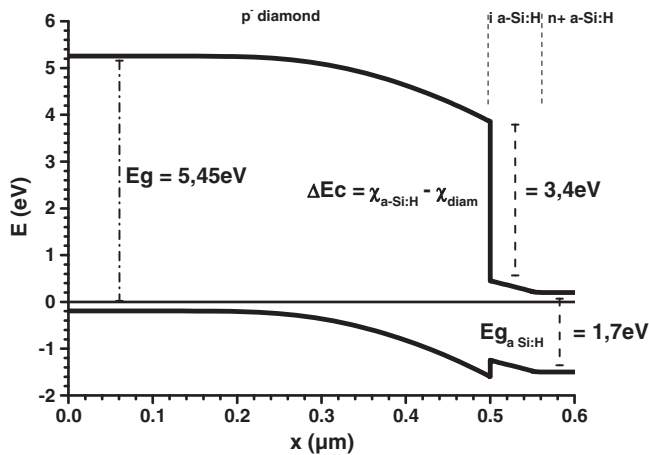


Fig. 6. Schematic of the energy band diagram for diamond/a-Si:H/n+ a-Si:H at equilibrium 12.

the diamond and the a-Si:H [22]. However, further investigation and refined modelling are required in order to identify the proper transport mechanism for this particular heterojunction and fully capture the underlying physics.

With regard to the breakdown of the device, we believe that the depletion region sustaining such a high electric field consists of the whole thickness of the p-diamond layer (500 nm) in addition to the intrinsic a-Si:H thickness (50 nm). Simulations using the model depicted in Fig. 6 show that the electric field at -160 V is 3.4 MV/cm in the diamond and 1.6 MV/cm in the intrinsic a-Si:H layer. As a result, the breakdown most likely occurs in the amorphous silicon material considering the magnitude of the electric field observed. This indicates that adding a thin intrinsic amorphous silicon film between the diamond and the contact may improve the breakdown performance. Moreover, this would help to alleviate the diamond surface inhomogeneities and therefore improve the reliability of the devices.

5. Conclusions

In this work, we have presented the temperature dependence of the electrical characteristics in diamond/a-Si:H heterojunctions. These devices show a strong rectifying ratio up to 10^9 at ± 2 V and mA current densities. Carriers transport appears to be governed by different mechanisms according to regime of operation. Comparing with a Schottky barrier diode fabricated on the same diamond epilayer and exhibiting an ideality factor $n \sim 1.1$, the heterojunction

J - V seems to follow an ideal diode characteristic for low bias voltages. At higher bias voltages, we observed a large ideality factor with a value of 3.6, independently of temperature. This could partly be explained by space charge limitation at the interface but further investigations are required to validate this assumption. The breakdown voltage reached -160 V i.e. 1.6 MV/cm in the 50 nm intrinsic amorphous silicon layer. Such a thin amorphous silicon layer could be implemented in power switches in order to reduce the thick diamond layers usually implemented in Schottky diodes. The cycling of the devices with temperature showed a robust operation with no variation of the C - V as well as the J - V characteristics demonstrating the potential of such structures in harsh environments.

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Atmospheric pressure route to epitaxial nitrogen-doped trilayer graphene on 4H-SiC (0001) substrate

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Large-area graphene film doped with nitrogen is of great interest for a wide spectrum of nanoelectronics applications, such as field effect devices, super capacitors, and fuel cells among many others. Here, we report on the structural and electronic properties of nitrogen doped trilayer graphene on 4H-SiC (0001) grown under atmospheric pressure. The trilayer nature of the growth is evidenced by scanning transmission electron microscopy. X-ray photoelectron spectroscopy shows the incorporation of 1.2% of nitrogen distributed in pyrrolic-N, and pyridinic-N configurations as well as a graphitic-N contribution. This incorporation causes an increase in the D band on the Raman signature indicating that the nitrogen is creating defects. Ultraviolet photoelectron spectroscopy shows a decrease of the work function of 0.3 eV due to the N-type doping of the nitrogen atoms in the carbon lattice and the edge defects. A top gate field effect transistor device has been fabricated and exhibits carrier mobilities up to 1300 cm²/V s for holes and 850 cm²/V s for electrons at room temperature. © 2014 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4903866>]

Since its discovery, graphene has attracted tremendous interest for condensed physics and material science as well as advanced technologies.^{1,2} Recent progress in graphene synthesis opens up different routes to investigate new building blocks based on hetero-interfaces between 2D-nanomaterials.^{3,4} Such materials systems will undoubtedly shape the future of nanoelectronic devices⁵ and researchers keep on optimizing synthesis technologies, i.e., mechanical exfoliation, laser exfoliation techniques,^{6,7} thermal decomposition of SiC, chemical vapour deposition (CVD), and liquid-phase exfoliation of graphene.⁸⁻¹⁰ Moreover, low cost processes have been developed such as laser-induced exfoliation of graphite, the reduction of graphene oxide (RGO) using radiative processes¹¹⁻¹⁴ or laser-induced unzipping of carbon nanotubes.¹⁵ RGO, CVD, and SiC graphene exhibit opto-electronic properties that could potentially outperform any alternative material and permit its implementation into a wide spectrum of applications with devices like field effect transistors (FETs), solar cells, and sensors.¹⁶⁻¹⁸ Nevertheless, to envision applications, the electronic properties of synthesized multilayer graphene still remain to be tailored to become competitive.¹⁹ For that purpose, a substantial part of the research is devoted to develop doping strategies using III-V elements, i.e., boron (B) and nitrogen (N) for p and n type, respectively.²⁰⁻²² Substitutional doping would modulate the band structure of the material and therefore its electronic properties. On the other hand, as synthesized graphene may present defect sites, it is possible that nitrogen or boron bond preferably to defects and/or edges particularly

on SiC graphene.²³⁻²⁵ However, considering the structure of graphene, doping must be adapted to its technology. Among the favoured approaches is the modulation of the electronic properties through *in situ* doping during synthesis and charge transfer using hetero-interfaces, e.g., nano colloids, polymers, and self-assembly monolayers.²⁶⁻²⁸ Regarding the *in situ* doping approach, one method consists of introducing nitrogen during the growth process. As a result, nitrogen atoms migrate to the interface forming Si-N-C bonds that reduce the carrier mobility (μ).^{29,30} A second approach consists of annealing the sample post growth under nitrogen atmosphere.²⁴ Again, the density of defects increases and is detrimental to the carrier mobility.

Here, we describe a method to grow N-doped epitaxial graphene on 4H-SiC (0001) under atmospheric pressure. The homogeneity of the as-grown layers was confirmed by atomic force microscopy (AFM), and the trilayer graphene was characterized by scanning transmission electron microscopy (STEM), Raman and X-ray and ultraviolet photoemission spectroscopy (XPS/UPS). Different nitrogen species were incorporated spontaneously into the graphene during the cooling of the sample at 1550 °C and under nitrogen flux. The bonding configurations of the C-N components and the electronic properties of the N doped graphene were characterized using XPS, UPS, and FET devices. The device of N-doped graphene exhibits a mobility of 1300 cm²/V s for holes and 850 cm²/V s for electrons. Our experimental observations permit a better understanding of the nitrogen doping of 2D materials as well as for the development of graphene-based electronic devices.

Graphene layers were grown on commercially available 4H-SiC (0001) substrates in an infrared rapid thermal annealing chamber. The SiC substrates were annealed on a graphite susceptor at around 1550 °C in argon pressure of less than 800 mbar for 10 min.³¹ In order to study the effect

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of the nitrogen atoms on the electronic properties of epitaxial graphene, the sample was exposed to nitrogen under cooling at room temperature for 15 min. These samples are labelled as N-doped graphene. The graphene layers were then transferred *ex-situ* from the growth chamber to Raman spectroscopy, XPS/UPS measurement systems. The Raman measurements were performed with a frequency-doubled NdYag laser operating at 532 nm as excitation source with up to 20 mW continuous wave output power.

XPS and UPS measurements for the study of the chemical composition and the work function (WF), respectively, have been performed using a PHI 5000 Versaprobe spectrometer (Physical Electronics) operating at a base pressure of 10^{-9} mbar. For the XPS analysis, a focused monochromatized Al K α X-ray source ($h\nu = 1486.6$ eV) was used. The WF was measured by UPS using a He I discharge lamp ($h\nu = 21.2$ eV). It was determined from the secondary electron cut-off. The position of the Fermi level was calibrated by measuring the Fermi edge of a sputtered cleaned gold sample. During the work function measurements, a bias of -8 V was applied to the sample. N-doped graphene was utilized to fabricate a $20 \mu\text{m}$ gate length and $50 \mu\text{m}$ gate width FET device using 7 nm of Al_2O_3 gate oxide deposited by atomic layer deposition (ALD). The electrical measurements were performed in an ambient environment using an Agilent B1500A semiconductor device parameter analyser. The characterization of metal-insulator-metal structures was performed by means of capacitance-voltage (C-V) measurements at a frequency of 20 kHz using a HP4284A high precision LCR meter.

Figure 1 presents AFM, TEM images, and micro-Raman spectroscopy, obtained on the N-doped trilayer graphene sample. Figures 1(a) and 1(b) present the AFM images of the graphene grown on a SiC (0001) substrate. The AFM image

shows a highly homogenous topography with a step density of $10\text{--}15$ nm height and atomically flat terraces of about $7 \mu\text{m}$ wide on average (Figure 1(a)). In AFM phase images (Figure 1(b)), at the step edges we observed the appearance of different regions, which corresponded to multilayer ribbons located at the very edge of the terrace. In order to investigate the interface and the thickness, cross-sectional STEM experiments were performed on N-doped epitaxial graphene. This cross-sectional view was observed along the (11–20) SiC zone axis (Figure 1(c)). As observed from the STEM images, the N-doped graphene grown on SiC, produced here, is predominantly composed by trilayer graphene. In the STEM image, the 3C-SiC lattice planes are straight, sharp, parallel to the surface, and equidistant. The interlayer separation is about 0.34 ± 0.01 nm, and the graphitic layers are atomically flat and show a continuous film.

In addition to acquiring AFM and STEM images, we characterized the graphene layer using Raman spectroscopy. In Figure 1(d), typical spectra of pristine graphene and N-doped graphene are shown, which correspond to measurements made on two locations of a terrace. One can notice that the graphene contributions are also observed, as expected on the pristine and N-doped trilayer they are identified by three main structures: (i) the D band, (ii) the G band, and (iii) the 2D band. For pristine graphene, the D peak is weak, indicating the low density of defects. In the case of N-doped graphene, we note an increase of the D band and one more contribution due to the (D') bands at 1620 cm^{-1} , corresponding to the disorder-induced feature, which is known to occur in sp^2 carbon with defects. The high intensity of D band, as well as the presence of the D' band, suggests that nitrogen breaks the local symmetry of the graphene lattice. In addition, we note that the 2D peak reduces in intensity and the FWHM increases from 40 cm^{-1} to 70 cm^{-1} as typically observed in N-doped graphene.²⁹

All previous experiments were performed on N-doped graphene, but the differences with respect to pristine graphene layers are not discussed, since the presence of nitrogen cannot be clearly detected using these techniques. In order to probe the effects of nitrogen dopants on the electronic properties of graphene layer, we performed XPS and UPS on the N-doped graphene layer. We probed the electronic properties of the samples using photoelectron spectroscopy (XPS) of nitrogen doped graphene layer (Figure 2). Figure 2(a) displays the deconvoluted C 1s core level XPS spectrum of N doped graphene. The C 1s spectrum showed four components at 283.7 , 284.6 , 285.4 , and 286.5 eV in binding energy.²⁹ These components correspond to the SiC bulk (noted SiC), the graphene layer (noted G), the interface layer (noted IL), and the C-N bounds (C-N), respectively. The small new peaks at 286.5 eV suggest the bonding formation of doped nitrogen atoms to be $\text{sp}^2\text{-C}$ or $\text{sp}^3\text{-C}$ atoms. The thickness of the graphitic film is calculated from the ratio between the intensity of the G and SiC components of the XPS spectrum. This ratio fits well with an exponential decay of trilayer of graphene coverage in agreement with the TEM measurement. Figure 2(b) shows the Si 2p spectrum for an N-doped graphene sample. It is dominated by a peak at 101.1 eV corresponding to the bulk silicon and presents a shoulder at higher energies. The shoulder is composed of a

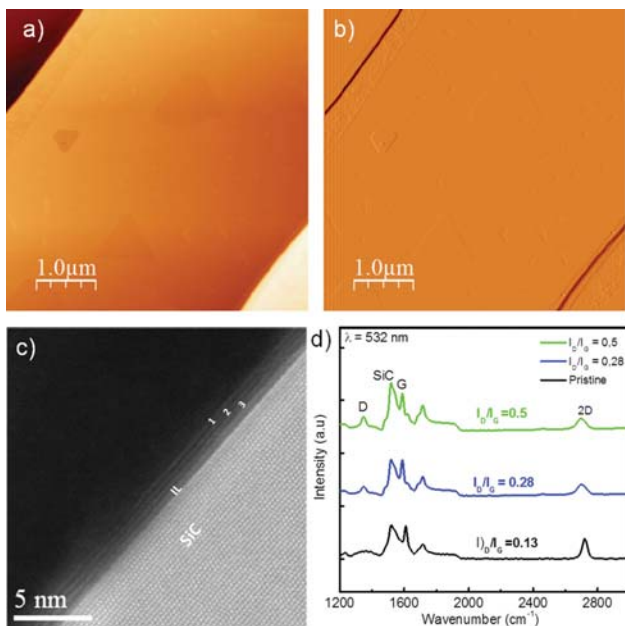


FIG. 1. (a) AFM topography of N-doped graphene sample. (b) AFM phase image of N-doped graphene. Graphene layer covers the entire substrate. (c) Cross-sectional High-resolution STEM image of N-doped graphene. (d) Comparison of Raman spectra taken for different I_D/I_G ratios on N-doped graphene and comparison to pristine sample.

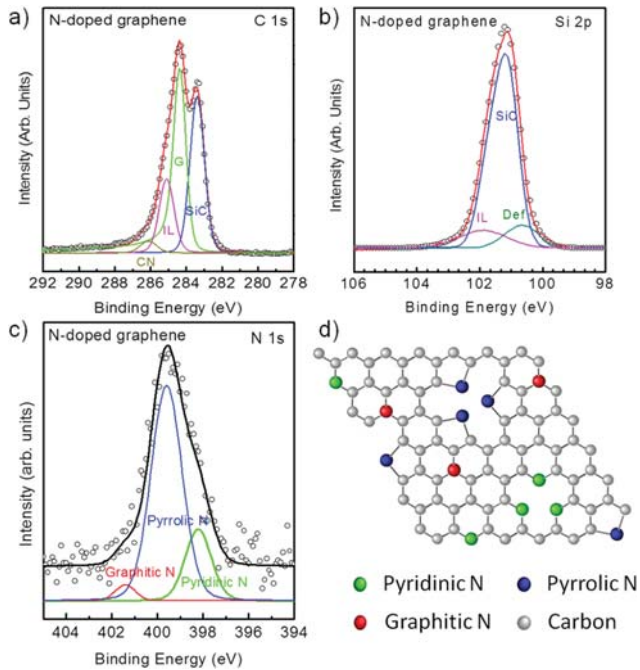


FIG. 2. (a) C 1s spectrum for N-doped graphene. The deconvolution using Doniach-Sunjjic line shape analysis shows the SiC, G, IL, and carbon nitrogen (CN) bonding configurations. (b) Si 2p XPS spectrum for N-doped graphene. (c) N 1s XPS spectrum for N-doped graphene showing 3 different nitrogen configurations. (d) The atomic configuration showing pyridinic-N, pyrrolic-N, and graphitic-N as well as graphene lattice and vacancies. XPS measurements were carried out at an angle of 45° with respect to the sample normal.

peak at 102.0 eV assigned to the IL between the graphene and the SiC (0001) substrate. Another peak at 100.7 eV is attributed to Si clusters of broken Si-C bonds formed during the graphitization process.^{29–32} Figure 2(c) shows the deconvoluted N 1s of the N-doped graphene sample. This peak is decomposed in three components centered at 398.2 eV, 399.6 eV, and 401.4 eV assigned, respectively, to pyridinic, pyrrolic, and graphitic configurations, respectively, as shown in Figure 2(d). It is admitted that graphitic-N is the most efficient doping configuration.³³ In our context, pyrrolic and pyridinic-N appear to be the dominant bonding configurations. Interestingly, no Si-N-C bonds are visible.³⁴ This observation indicates that the nitrogen is predominantly bonded in the graphene plane and edges and did not diffuse to the interface. This diffusion may have been prevented by the trilayer nature of the graphene in our sample. From photoemission spectra, we can estimate the nitrogen concentrations at the sample surface. The total amount of nitrogen atoms can be calculated from the N 1s and C 1s peak areas ratio in the bulk sensitive configuration weighted by the relative cross sections. The nitrogen content in pyridinic, pyrrolic, and graphitic configurations is 21.3%, 75%, and 3.7%, respectively.

We performed UPS analysis to determine the shift in work function induced by N atoms and verify the nature of the doping of graphene layers. UPS data were acquired several times from the overall sample and the averaged results are shown in Figure 3(a). This shows the UPS spectra around the secondary electrons cut-off region of the pristine and N-doped graphene. The position of the Fermi level was calibrated using a gold sample. The secondary electron cut-off was determined by extrapolating two solid lines from the background and

straight onset in the secondary electron cut-off region of the spectra. WF is determined from the secondary electron cut-off as $WF = h\nu - E_{th}$, where $h\nu$ and E_{th} are the photon energy of excitation light (He I discharge lamp, 21.2 eV) and the secondary electron cut-off energy, respectively. As a reference, we utilized a sample of pristine monolayer graphene but without N-doping, the WF measured is 4.3 eV, similar values have been reported previously and trilayer undoped graphene is estimated to be ~ 4.4 eV.³⁵ We therefore conclude that the N-doping process implemented in this work on trilayer epitaxial graphene has demonstrated its effectiveness to shift to a minimum of 0.3 eV, the WF from 4.4 eV to 4.1 eV confirming the n-type doped of the graphene layer (Figure 3(b)).

To investigate the transport properties of N-graphene samples, a top gate FET device was fabricated and tested at room temperature. Cr/Ni Source-drain electrodes were defined by optical lithography and subsequent metal evaporation then 7 nm thick aluminum oxide (Al_2O_3) gate oxides was deposited by ALD. Al top gate was deposited by e-beam evaporation. A picture of the device is shown in Figures 4(a) and 4(b). The drain current versus gate voltage (I_d-V_g) and drain voltage (I_d-V_{ds}) curves of the N-doped graphene sample show ambipolar transistor effect and the minimal current detected corresponding to the Dirac point (V_{Dirac}) is located at -1 V and reaches -1.5 V for some devices, no saturation is observable on the I_d-V_{ds} characteristic (Figures 4(c) and 4(d)). The top gate device operates as a p-channel FET for $V_g < V_{Dirac}$ whereas it operates as n-channel FET for $V_g > V_{Dirac}$. Since V_{Dirac} is located at -1 V, the device clearly reveals the n-type doping character of N incorporation in the graphene. The gate leakage value starts at 10^{-12} and increases up to 10^{-10} A with increasing bias. The carrier mobility (μ) can be assessed using $\mu = L \times (\Delta I_d / \Delta V_g) / (W \times C_g V_d)$, where C_g is the gate capacitance per unit area (ca. 200 nF/cm² measured by capacitance-voltage measurement); L and W are the length and the width, 20 μ m and 50 μ m, respectively; and V_d is 0.5 V. The mobility for holes and electrons is about 1300 cm²/V s and 850 cm²/V s, respectively, but saturates at voltages below -2 V and beyond 0 V. The on/off ratios are 1.7 and 1.5 for holes and electron channel, respectively. Moreover, there is an onset of saturation observed for the electron channel. The carrier concentration $n_s \sim 2 \times 10^{12}$ cm⁻² is estimated from C_g using $q \cdot n_s = C_g (V_g - V_{Dirac})$, with V_g the gate voltage and q the elementary charge. This value is relatively low as opposed to N-doped graphene obtained previously.²⁹ Note that the ALD- Al_2O_3 process is oxygen rich that may possibly compensate the N doping. This point is further stressed by the fact that we observed that the C-N bonds pyrrolic-N and pyridinic-N favor functionalization thanks to the sp_z bonds.³⁴ Recently, It has been demonstrated that subsequent oxidation steps reduce the energy difference between the Dirac point and the Fermi level and as a result the carrier density drops to $\sim 1.8 \times 10^{12}$ cm⁻².³⁶ Nevertheless, the striking feature of this device is its carrier mobility that is nearly as high as pristine graphene obtained on Hall bars by Pallecchi *et al.* in prior work but at 4 K and without any gate oxide.³⁷ We conclude therefore that although oxygen may have hindered the nitrogen doping to an extent, limited scattering or traps centers have diffused at the interface and the carriers mobility

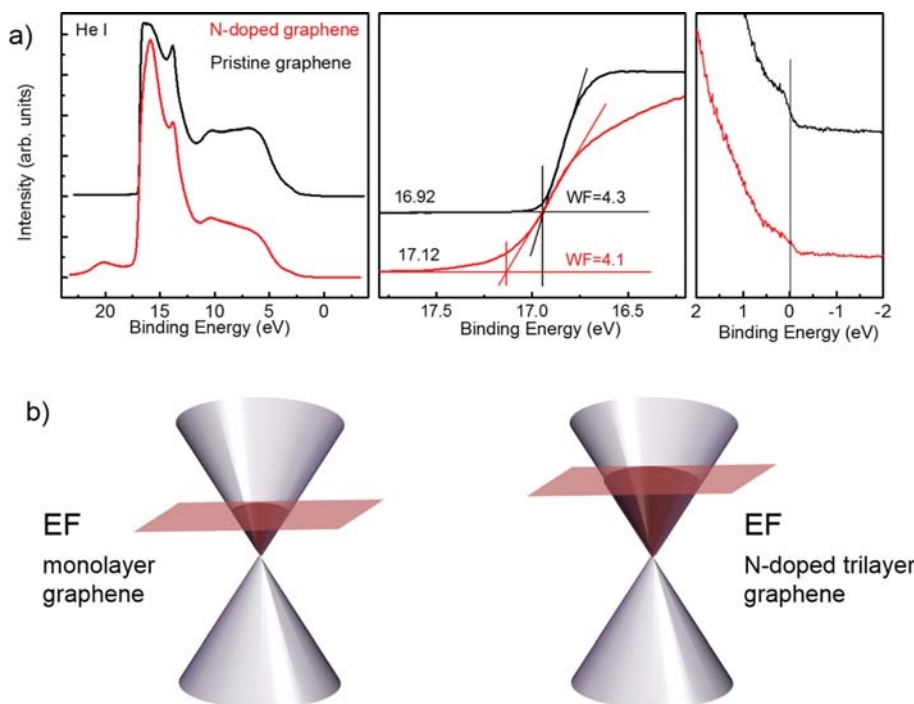


FIG. 3. (a) UPS spectra of the pristine and N-doped graphene. UPS data were acquired several times on the overall sample and were averaged. Left panel shows global spectrum/middle and right panels show the secondary electron cut-off and the Fermi level regions, respectively, to determine the WF. The monolayer sample taken as reference exhibits a 4.3 eV WF, whereas the N-doped sample reaches 4.1 eV. (b) Band structures of the pristine and N-doped graphene showing the variation in WF.

estimated could have been even larger before gate completion. In addition, no hysteresis was observed while sweeping V_g back and forth indicating that no trapping occurred at the Al_2O_3 /graphene interface. Note that current silicon high speed devices exhibit few $100 \text{ cm}^2/\text{V s}$ and suffer from short channel effects. Yet, considering the low on/off ratios logic devices are unrealistic however there is potential for radio-frequency FETs as the cut off frequency F_T increases with mobility,³⁸ but one should consider parasitic resistances to properly assess the potential for such applications. On the other hand, nanoribbons patterned on N-doped graphene with optimized gate dielectric³⁹ could open the band gap required for logic applications. Such a scheme coupled to this atmospheric growth and doping method is a simple and cost effective approach to produce graphene based nanoelectronic devices.

In summary, we have investigated a doping approach to insert nitrogen into trilayer graphene on SiC (0001) under atmospheric pressure. AFM image and Raman spectroscopy give evidence of the predominance of trilayer graphene across the sample. This doping method is highly attractive for the efficient incorporation of doping species into the graphene lattice. The C-N bonding configurations are predominantly pyrrolic, pyridinic, and graphitic as confirmed by the XPS spectra. Nevertheless, the graphitic-N incorporation into the graphene network reduces the work function from 4.4 eV for the pristine graphene to 4.1 eV for the N-doped graphene as observed by UPS. In addition, we fabricated a top gate FET device using Al_2O_3 as a gate oxide. The device exhibits a V_{Dirac} at -1 V indicating the n-type of the graphene and mobilities of $1300 \text{ cm}^2/\text{V s}$ for holes and $850 \text{ cm}^2/\text{V s}$ for electrons at room temperature.

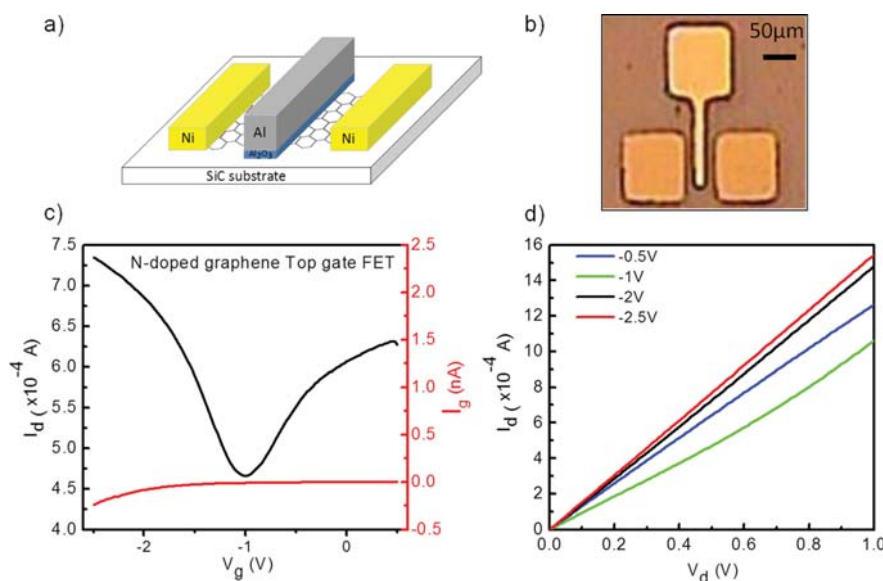


FIG. 4. (a) Schematic of the graphene based FET device. (b) Optical image of a device fabricated on the N-doped trilayer graphene with 7 nm Al_2O_3 gate oxide. The channel length is $20 \mu\text{m}$ and the width $50 \mu\text{m}$. (c) Current-voltage characteristics of top gate FET on N-doped graphene at room temperature. I_d - V_g curves showing ambipolar behavior with V_{Dirac} at -1 V measured for $V_d = 0.5 \text{ V}$. (d) I_d - V_d curves for various gate voltages showing linear characteristics the minimum for various V_g voltages.

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Excitation transfer in stacked quantum dot chains

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Abstract

Stacked InAs quantum dot chains (QDCs) on InGaAs/GaAs cross-hatch pattern (CHP) templates yield a rich emission spectrum with an unusual carrier transfer characteristic compared to conventional quantum dot (QD) stacks. The photoluminescent spectra of the controlled, single QDC layer comprise multiple peaks from the orthogonal QDCs, the free-standing QDs, the CHP, the wetting layers and the GaAs substrate. When the QDC layers are stacked, employing a 10 nm GaAs spacer between adjacent QDC layers, the PL spectra are dominated by the top-most stack, indicating that the QDC layers are nominally uncoupled. Under high excitation power densities when the high-energy peaks of the top stack are saturated, however, low-energy PL peaks from the bottom stacks emerge as a result of carrier transfers across the GaAs spacers. These unique PL signatures contrast with the state-filling effects in conventional, coupled QD stacks and serve as a means to quickly assess the presence of electronic coupling in stacks of dissimilar-sized nanostructures.

 Online supplementary data available from stacks.iop.org/SST/30/055005/mmedia

Keywords: quantum dot chains, photoluminescent mapping, electronic coupling, cross-hatch patterns, InAs, vertical stacking, excitation transfer

(Some figures may appear in colour only in the online journal)

1. Introduction

Semiconductor quantum dots (QDs) grown by molecular beam epitaxy (MBE) are often stacked in order to increase the active optical volume and to tune the emission or detection wavelength and polarization of the QD ensembles [1, 2]. Stacking QDs is achieved through thin spacer layers which physically separate but often electronically couple adjacent QD layers [3]. Understanding the coupling nature of vertically stacked QD structures is of fundamental importance to the operation and optimization of QD-based devices such as memory [4], lasers [5] and solar cells [6, 7]. Though useful, coupling is not always necessary or desired, particularly for broadband applications which benefit from the superposition

of different wavelengths from individual QD layers [8]. If present, electronic coupling results in the lowering of the excitonic ground-state (GS) energy, and consequently a red-shift of photoluminescent peak [3, 9]. The degree of coupling is thus usually inferred from the magnitude of the energetic red-shift relative to those emitted from a single QD layer structure [3]. This approach can be misleading in stacked QDs as the strain profile at the growth front is affected by the underlying nanostructures: subsequent QD layers usually nucleate at a lower deposition amount [9, 10]. If grown at the same two-dimensional (2D) equivalent thickness throughout, upper QD layers would be bigger than those of the lower QD layers, with a concomitant red-shift due to size—not coupling. One way to unambiguously identify the presence and

evaluate the strength of coupling is to vary the spacer thickness and observe the changes in PL signals as a result of excitation transfer of carriers. This approach has been adopted to study coupling between, for example, stacked QDs [11] and stacked quantum dots and wells [12]. Alternatively, one can fix the spacer thickness, vary the size of each stack, perform PL measurements and simply count the number of GS peaks: a single (multiple) GS peak indicates the presence (absence) of coupling [11]. This article adopts the latter approach to study an unusual coupling property of stacked quantum dot chains (QDCs) on cross-hatch pattern (CHP) templates.

QDCs or laterally-coupled QDs have garnered significant interest in the past decade [13] and have recently gained renewed interest due to their unique geometry suitable for fundamental transport studies [14] and polarization-sensitive optoelectronic devices [15]. However, QDCs are rarely studied in stacked forms due to their complex optical characteristics [16], particularly when coupling can simultaneously occur laterally and vertically as is the case here. In this paper, stacked InAs QDCs on InGaAs/GaAs CHP templates grown by molecular beam epitaxy (MBE) are characterized by photoluminescence (PL) and a complete PL fingerprint of QDCs/CHP structures is reported. Under high excitation power densities, stacked QDCs do not exhibit state-filling effects as would be observed in stacked QDs. The otherwise excited-state carriers are instead transferred toward the lower QDC layer, an effect attributed to the combination of extended wavefunctions, resonant tunnelling and thermalization.

2. Experimental

The structures investigated comprise multiple stacks of InAs QDCs grown on partially-relaxed InGaAs film on GaAs by solid-source MBE Using Riber's 32P MBE system, and after *in situ* thermal cleaning of GaAs (001) surface, growth starts from 300 nm GaAs buffer layer, followed by 25 nm In_{0.2}Ga_{0.8}As, 10 nm GaAs spacer, and 1, 3, or 5 stacks of InAs QDC/10 nm GaAs spacer pairs. The cross-hatch pattern surface of the InGaAs layer serves as a template on which chains of QDs form along the orthogonal [110] and [1 $\bar{1}$ 0] directions. The smoothness of the growth fronts and the formation of QDs are monitored *in situ* via streaky and spotty reflection high-energy electron diffraction (RHEED) patterns, respectively. Each QD layer is grown until the RHEED pattern changes from streaks to spots, i.e., at the onset of QD formation. The 2D equivalent thicknesses of the bottom-most stack are 1.7 monolayer (ML) and the remaining stacks are 1.3 ML. Finally, all samples are capped with 100 nm GaAs for PL measurements. Two PL set-ups are employed. For free-space, macro-PL setup, the samples are fixed in a cryostat, excited by a broad beam (2.39 mm spot size), 514.5 nm Ar⁺ laser, and emission detected by a liquid nitrogen-cooled InGaAs point detector (Hamamatsu's G7754) using standard lock-in techniques. For confocal, micro-PL setup, the sample is mounted on a piezoelectric-driven platform (Witec's

alpha300), excited by a narrow beam ($\sim 1 \mu\text{m}$ spot size) frequency-doubled 532 nm Nd:YAG laser operating in continuous mode, and emission detected by a thermoelectrically-cooled InGaAs array detector (Andor's DU491A). Spatial- and energy-resolved PL maps are acquired from the micro-PL setup by raster scanning and simultaneously collecting point spectra. All maps shown represent PL intensities integrated over a 10 meV bandwidth around energies of interest.

3. Results and discussion

Conventional InAs Stranski–Krastanow (SK) QDs grown on flat GaAs (001) are randomly distributed and typically emit a single PL peak at around $1 \mu\text{m}$ with a full width at half maximum (FWHM) of a few 10 s meV [17]. Certain growth conditions can extend the wavelength to the 1.3–1.55 μm telecom window [18] or lead to bimodal or multimodal size distributions with multiple PL peaks [19–21], while random distribution remains. In contrast, InAs QDs grown on CHPs are guided, forming chains along the orthogonal [110] and [1 $\bar{1}$ 0] directions, each direction with its own size, size distribution, and wetting layer (WL) due to the asymmetry of the underlying dislocations [22]. The formation of QDs along the orthogonal dislocation chains has been established by plan-view transmission electron microscopy (TEM) [23], whereas vertical correlation of QDs with 10 nm GaAs spacer has been confirmed by cross-sectional TEM [24]. The 60° dislocations at the lower InGaAs/GaAs interface, typical in zincblende heteroepitaxy, cause surface strain fields that affect adatoms motion during growth [25], but do not affect the intrinsic emission efficiency of the overlying QDs [26]. The PL spectrum of a QDC layer would thus contain many more PL peaks than those of conventional SK QDs due to the co-existence of many optically active structures.

This section is divided into three parts. The first part describes the PL maps and spectra of the 1-stack QDC layer, showing all the possible luminescent peaks. The second part shows that luminescence is dominated by the uppermost QDC layer which is nominally uncoupled to the underlying QDC layers. The third part shows that the luminescence from the bottom QDC layers emerges at high excitation level, and provides a qualitative explanation of the underlying mechanism.

3.1. Single QDC layer: basic emission peaks

The 1-stack QDC sample emits in the 1–1.4 eV range similar to conventional SK QDs, but with a much richer optical feature. Figures 1(a)–(f) show spatial- and energy-resolved spectral maps of the same $20 \times 20 \mu\text{m}^2$ area of the sample at 80 K. The PL maps, integrated over increasing energies from 1.005 eV in figure 1(a) to 1.275 eV in figure 1(f), show spatially non-uniform emissions with a cross-hatch pattern resembling the surface undulation of the underlying InGaAs/GaAs template. Figure 1(a) shows that at 1 eV, the lower energetic end of the spectra, emissions emerge from bright patches which look like stripes along the [1 $\bar{1}$ 0] direction. The

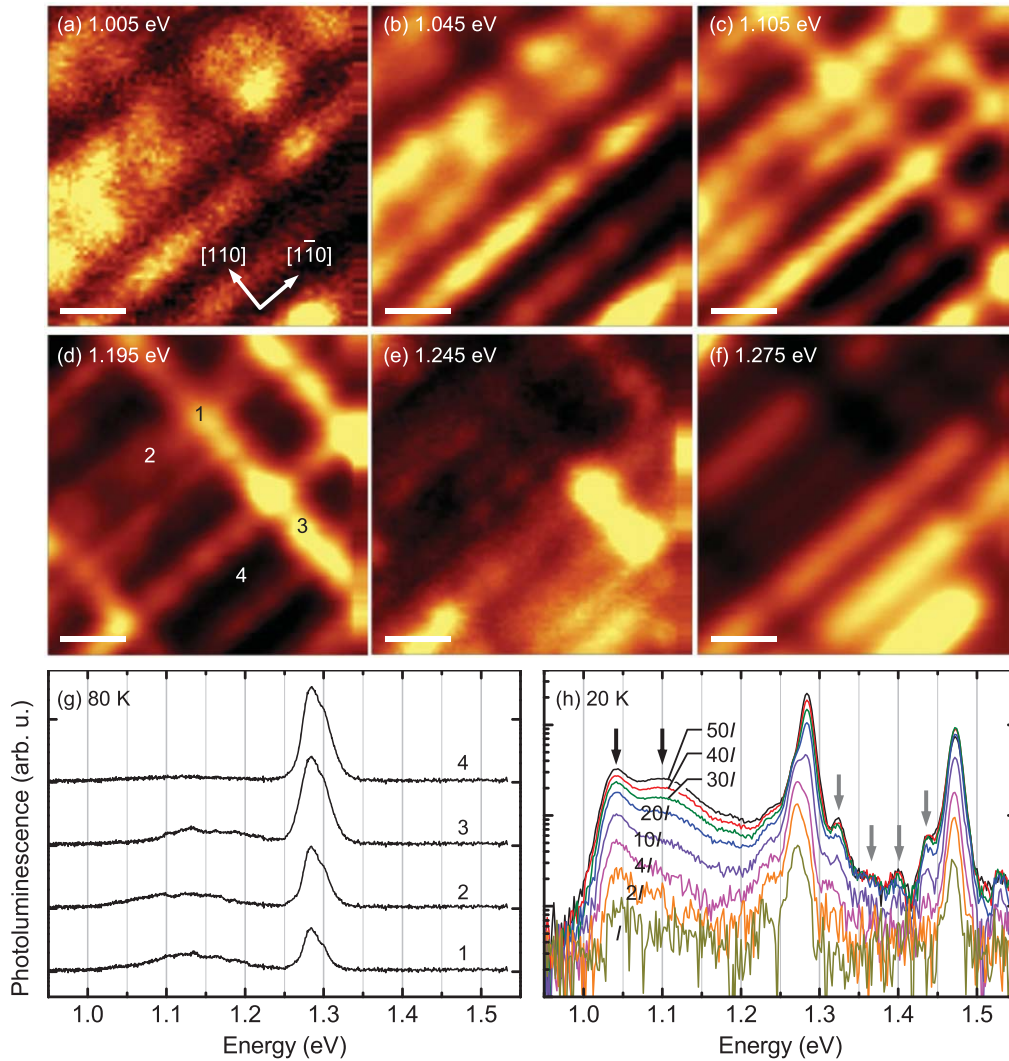


Figure 1. PL of a single InAs QD chain layer on an InGaAs/GaAs cross-hatch pattern. Same-area, $20 \times 20 \mu\text{m}^2$ micro-PL maps at increasing integrated intensity from (a) 1.005 to (b) 1.045, (c) 1.105, (d) 1.195, (e) 1.245 and (f) 1.275 eV. Spectra at pixels 1–4 in (d) are shown in (g): pixel 1 is taken at an intersection between $[1\bar{1}0]$ and $[110]$ dislocation lines, 2 on a $[1\bar{1}0]$ dislocation line, 3 on a $[110]$ dislocation line, and 4 on a dislocations-free area. (h) Macro-PL spectra measured at increasing excitation power density from, bottom to top, $I = 0.11 \text{ W cm}^{-2}$ to 2, 4, 10, 20, 30, 40 and 50 times I . The scale bars in (a)–(f) are $4 \mu\text{m}$. Spectra in (g) are offset for clarity.

stripes become clearer and better resolved as the energy increases to 1.045 eV in figure 1(b). The dottiness of the lines making up the stripes is simply a reflection of the variation in local QD density, in good agreement with the morphology of uncapped samples (see the supplementary data, available at stacks.iop.org/SST/30/055005/mmedia). When the energy increases to 1.105 eV in figure 1(c), emissions from the existing $[1\bar{1}0]$ direction begin to fade while those from the orthogonal, $[110]$ direction emerge. The emissions from the $[110]$ and $[1\bar{1}0]$ stripes overlap and yield the characteristic CHP luminescence observed in figure 1(c). As the energy continues to increase to 1.195 eV in figure 1(d), the $[1\bar{1}0]$ emission peters out, whereas the $[110]$ emission intensifies. And as the energy keeps on increasing to 1.245 eV in figure 1(e) and 1.275 eV in figure 1(f), the $[110]$ and $[1\bar{1}0]$ emissions are extinguished, replaced by bright patches emerging in the previously dark areas—i.e., the bright/dark

regions in figures 1(a) and (f) are reversed. (The reversal is easily recognized in the first video in the supplementary data).

The QDs can be categorized, in evolution sequence [27] and with corresponding labels shown in figure 1(d), into four distinct groups: 1. at the intersection of the orthogonal $[110]$ and $[1\bar{1}0]$ dislocations, 2. on the $[1\bar{1}0]$ dislocation lines, 3. on the $[110]$ dislocation lines, and 4. on the remaining areas. The four QD ensembles emit slightly differently. Figure 1(g) shows point spectra at pixels 1–4 in figure 1(d), corresponding to the four QD ensembles above. Emissions from pixels 1–3 comprise two principal peaks: a broad peak centered at around 1.15 eV and a narrow peak at 1.27 eV. In contrast, emission from pixel 4 comprises only one narrow peak, also centered at 1.27 eV.

The broad peaks result from QD chains along the $[1\bar{1}0]$ and $[110]$ directions as unequivocally proven by microscopy and spectroscopy. The micro-PL maps in figures 1(a)–(f)

provide the microscopic proof, whereas the macro-PL spectra in figure 1(h) provide the spectroscopic confirmation. It has long been known that the underlying InGaAs/GaAs CHPs are asymmetric: the $[1\bar{1}0]$ stripes nucleate earlier, have greater density, and result in surface steps which are taller than the $[110]$ stripes [28]. The asymmetry is transferred to the overgrown layers, resulting in QDs along the $[1\bar{1}0]$ direction forming slightly earlier and are thus taller and emit at a lower energy than those along the orthogonal $[110]$ direction [22, 27, 29]. The microscopic images in figures 1(c)–(d) provide a clear visual evidence of QD luminescence decorating the $[1\bar{1}0]$ and $[110]$ stripes, at slightly different energies. This small energy difference however cannot be resolved in the corresponding point spectra: figure 1(g) shows that pixel 2, taken along the $[1\bar{1}0]$ direction, emits at a slightly lower peak energy than pixel 3, taken along the orthogonal $[110]$ direction. Though these two peaks are spatially resolved in microscopy, they are spectrally unresolved as a result of micro-PL setup's fast integration time. The macro-PL setup, in contrast, has a much longer integration time and can provide complementary spectra with greater signal-to-noise ratios. Figure 1(h) shows excitation power-dependent macro-PL spectra of the same sample (but on a different area) at 20 K. The lowest two energetic peaks—1.04 eV for the $[1\bar{1}0]$ -aligned QDs and 1.10 eV for the $[110]$ -aligned QDs highlighted by the black arrows—can now be clearly resolved at high excitation powers.

The narrow 1.27 eV peak is asymmetric: the left and right sides of the 1.27 eV peak in figure 1(g) tail off slightly differently—a characteristic of two unresolved Gaussian peaks with different FWHM. The closely-spaced emissions arise from the superposition or spectral overlap of the small free-standing QDs and the underlying InGaAs CHP template. The PL map in figure 1(f) shows that the areas that give off this luminescence are those between the cross hatches which happen to be the nucleation sites for free-standing QDs, too.

The four small peaks between 1.3 and 1.47 eV (observed only in the macro-PL setup as indicated by the grey arrows in figure 1(h)) are most likely associated with multiple wetting layers, some of which were previously identified [22]. For conventional InAs/GaAs SK QDs, a single WL exists and emits at around 1.44 eV. This is true even if bimodal size distributions are present [21], as long as the growth front is flat. For InAs QDs on InGaAs CHPs, the growth front is not flat. In fact, the surface steps in the $[1\bar{1}0]$ and $[110]$ directions are different [28]. The WL underneath the QD chains along the $[1\bar{1}0]$ and $[110]$ directions can thus be expected to be different—for example, they could form one-dimensional wetting wires [30]—but similar structures investigated so far reported just a single WL energy [22].

The multiple WL peaks above are only observed close to the carbon-impurity, 1.49 eV peak and the bulk GaAs, 1.52 eV peak. Measurements taken at different areas where the 1.49 and 1.52 eV peaks are absent do not reveal the multiple WL peaks. This indicates the possibility that bulk C centers render ineffectual the carrier capture by QDs from the GaAs matrix and the WLs, and explain the elusiveness of the multiple WL luminescence. It is a normal practice for those

carrying out PL measurements to shine the exciting laser on a spot that yields the best signal and in so doing move away from areas with large local concentrations of C, and hence miss the WL peaks.

It is worth pointing out that the multimodal size distribution of the 1-stack layer which gives rise to multiple emission peaks has not been optimized for broadband applications. If desired, one can increase the inhomogeneity of the spectrum by, for instance, growing the QDs at a higher rate or subjecting them to rapid thermal annealing [31]. In addition, one can also increase the luminous efficacy of real devices by soft-annealing under hydrogen so that most defects are neutralized and do not adversely affect long-term reliability [22].

3.2. Multi-stack QDCs: dominant emission from top-most layers

In reflection-based PL set-ups, the 1-stack QDC layer enjoys an unobstructed output window but the 3- and 5-stack QDC layers may not. This depends on electronic coupling. If the stacked layers are coupled, they behave as a single ensemble and should enjoy an unobstructed output window as is the case for the 1-stack sample. But if the stacked layers are uncoupled, luminescence from all the layers should be detectable, unless some are obstructed—reabsorbed, scattered, or reflected—in which case the emissions are dominated by the overlying structures due to geometrical advantage. Such behaviour in stacks of randomly distributed QDs cannot be proven through spectroscopy alone. But if the random distribution is reduced, as is the case for QDCs, and with PL mapping capability, it is possible to draw such a conclusion as shown below.

Figures 2(a)–(d) show the PL maps of the 3-stack QDC sample at increasing integrated energy from 1.075 eV in figure 2(a) to 1.235 eV in figure 2(d). Similarly, figures 2(e)–(h) show the PL maps of the 5-stack QDC sample from 1.075 eV in figure 2(e) to 1.235 eV in figure 2(h) (see animated videos in the supplementary data for the complete ranges). The maps show luminescence which is CHP-like for the 3-stack sample, but stripes-like for the 5-stack sample. Since adjacent stacks are separated by a 10 nm GaAs spacer which is sufficiently thin to allow coupling in conventional SK QD stacks [11], a question emerges as to why CHP-like luminescence similar to the 1-stack sample described above is not observed in the 5-stack case, or is not more clearly observed in the 3-stack case because the bottom-most QDC layer for the three samples is identically grown, has the biggest dot size and the lowest GS energies, and should thus provide the same optical features (CHP-like) as observed in the previous section. The maps shown in figure 2 instead more closely match the AFM morphologies of the top-most QDC layer where the number density of QDs along the $[110]$ direction is significantly reduced (see the supplementary data), implying that the emission is dominated by the top-most layer. The bottom-most QDC layer buried along the $[110]$ direction is almost undetectable; it can be barely distinguished by the collinearity of bright or dark spots, as indicated by broken lines in figure 2.

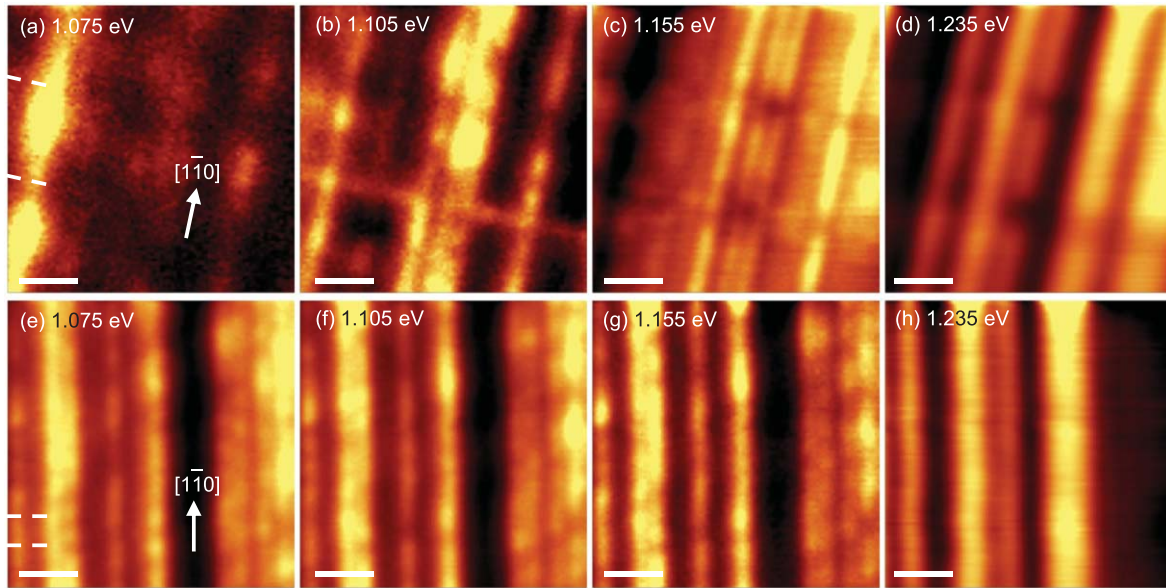


Figure 2. Same-area, room-temperature, $10 \times 10 \mu\text{m}^2$ micro-PL maps of (upper panels) the 3-stack QD chain sample at increasing integrated intensity from (a) 1.075 to (b) 1.105, (c) 1.155 and (d) 1.235 eV, and (lower panels) the 5-stack QD chain sample from (e) 1.075 to (f) 1.105, (g) 1.155 and (h) 1.235 eV. The scale bars are $2 \mu\text{m}$. The broken lines are guide to the eye and indicate some of the buried [110] dislocation lines.

One possible explanation for the much reduced [110] emission is carrier tunnelling from the bottom to the top QDC layer as has been observed in the QD bi-layer reported by Heitz *et al* [11]. However, this mechanism cannot explain the missing CHP-like emissions because carriers always tunnel towards the lower energetic state, i.e., the bottom-most QDC layer (1.1 eV active), not the top-most QDC layer (1.2 eV). If inter-stack tunnelling were present, the CHP-like emissions would have been enhanced, not suppressed.

Another possible explanation is that the top QDC layer has the highest quantum efficiency, thus dominating the weaker emission from the low quantum efficiency bottom stacks. The QDC stack is strained throughout as it is sandwiched between the top GaAs capping layer and the bottom partially-relaxed InGaAs CHP layer which in turn rests on a GaAs buffer. Since the top stack is in contact with the dislocations-free GaAs cap layer, whereas the bottom stack is in close proximity to the dislocations-prone CHP layer, the top stack would have a greater optical quality. Unless the strain profile surrounding each QD layer is carefully compensated [32], increasing the number of QD layers would in general result in accumulated strain that ultimately degrades the optical quality of the whole QD stack [33].

3.3. Multi-stack QDCs: excitation transfer

After many trials to uncover the bottom layer emissions—mostly by varying the optical path from normal to edge—it was found that the elusive emissions are not entirely missing, only significantly diminished since they are partially retrieved simply by increasing the excitation power density. This approach is however against a normal PL practice of using minimum excitation to study the true ground-state energies of QDs [9] and also to avoid sample heating.

Figures 3(a) and (b) show the macro-PL spectra of the 3- and 5-stack QDC samples, respectively. The spectra are measured from a low excitation power density I_0 of 0.11 W cm^{-2} to $50I_0$. For the 3-stack sample, increasing excitation results in intensity saturation of the 1.2 eV peak emissions from the top-most layer. Such saturation in conventional SK QDs would coincide with the appearance of one or more *higher* energy peaks as a result of state filling, and this is true for both single-layered and stacked QDs [12]. The spectra in figure 3(a) are however the opposite: as the 1.2 eV peak saturates, a *lower* energy peak emerges at around 1.1 eV, and at $40I_0$ excitation, another peak at an even lower energy of around 1.05 eV can be seen to be emerging. The sequential appearance of the 1.1 and 1.05 eV peaks upon saturation of the 1.2 eV peak is evident in the excitation-dependent PL intensity plots at the three energies shown in figure 3(c). The two additional peaks—1.1 and 1.05 eV—coincide with those of the 1-stack layer described earlier, strongly indicating that they arise from the bottom-most QDC layer.

The partial recovery of the bottom-most QDC emissions could be a direct or an indirect result of increased excitation, or a combination of both. The direct result is simply due to the greater availability of photons reaching the bottom-most stack. The indirect result is due to excitation transfer of carriers from the top- (high energy) to the bottom (low energy) layer, which is energetically favorable but ineffective at low-level excitations. The inefficiency is a result of suppressed tunnelling. At 10 nm ($\sim 36 \text{ ML}$), the GaAs spacer is sufficiently thin that tunnelling readily occur among stacks of conventional SK QDs [11]. But this is not the case for stacks of QDCs here. The tunnelling between stacks of QDCs must have been suppressed by the presence of the underlying misfit dislocations—the sole differentiating factor between the QDC

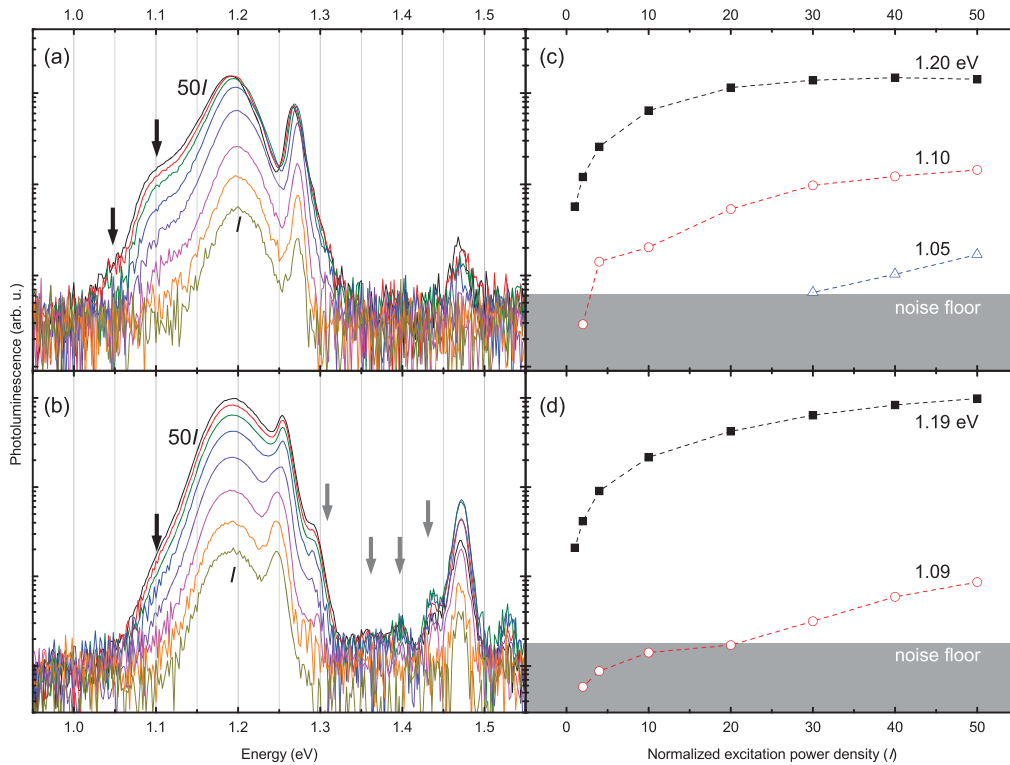


Figure 3. Macro-PL spectra of the (a) 3- and (b) 5-stack QDC samples measured at increasing excitation power density from, bottom to top, $I=0.11$ W cm^{-2} to 2, 4, 10, 20, 30, 40 and 50 times I . The solid arrows indicate peaks that appear only at high excitation levels. The grey arrows point to WL-related peaks. The increase in PL intensity as a function of excitation power density (normalized to I) for the (c) 3- and (d) 5-stack QDC samples at selected energies.

and QD stacks. Often associated with dislocations are strain fields known to cause local inhomogeneities in various physical properties [34]. The strain fields can be so strong that they affect surface atom motion and guide the nucleation of nanoscale QDs [35, 36] or the running direction of micron scale droplets [37]. Their effects on coupling are thus not surprising. External strains applied via piezoelectric crystal, for example, have been shown to affect fundamental QD excitonic properties [38], particularly to tune the excitonic binding energies [39]. Internal strains caused by interfacial misfit dislocations should likewise affect excitonic GS wavefunctions as a result of electric field induced by piezoelectric effects and/or strain gradients. Electric fields, built-in or externally applied, increase the effective distance between carriers confined in vertically-stacked quantum structures, and thus decrease coupling. The decrease is offset at high-level optical excitation. As the GS becomes saturated from the increased excitation, the first excited state (ES) would normally emerge in uncoupled nanostructures. For the multi-stack QDC structures, however, the ES wavefunctions extend further in space (are less localized) than those of the GS, penetrating further into the GaAs spacer and subsequently falling into the lower GS of the bottom stack. The extra carriers that would normally give rise to the higher-energy ES peaks thus avail themselves of the lower-energy GS of another stack which explains the successive emergence of the lower-energy PL peaks and the absence of state-filling effects in figure 3(a). Excitation transfer between an ES of one

nanostructure and a GS of another in resonant has been reported in many systems [11, 12].

For the 5-stack sample, increasing excitation also results in intensity saturation of the 1.19 eV peak of the top-most QD layer and the appearance of the 1.09 eV peak as shown in the spectra in figure 3(b) and the excitation-dependent PL intensity plots of the two peaks in figure 3(d). The saturation of the 1.19 eV peak and the emergence of the 1.09 eV peak seen in figure 3(d) are, however, more gradual than those of their equivalence in the 3-stack sample—the 1.2 and 1.1 eV peaks—in figure 3(c). This possibly results from the greater saturated intensity due simply to the 5-stack sample's greater QD areal density—approximately by 5/3 times. The state-filling effects are also absent; the high energy peaks between 1.3 and 1.47 eV are WLs as described while discussing the 1-stack sample earlier. These WL peaks cannot be observed in figure 3(a) since this is a low C-impurity area evidenced by the 3-stack sample's lowest 1.47 eV peak among the three samples.

4. Conclusion

MBE-grown InAs QD chains on InGaAs/GaAs CHPs are optically active and rich with luminescent signatures from QD ensembles, CHP template, and multiple wetting layers. The latter have so far evaded detection and can only be observed around areas with relatively high concentrations of C-

impurity evidenced from their co-occurrence with the 1.49 eV peak. Based on this observation, we recommend that PL signals should be optimized around a known impurity peak in order to obtain a fuller picture of physics—albeit at the expense of signal strength. When these InAs QD chains are stacked and separated by GaAs spacers, the top-most QDC layer dominates the emissions. The bottom-stack emissions are however missing—an unexpected result from energetic consideration since the bottom-stack QDs are the biggest and thus have the lowest energetic states. The missing emissions are likely due to degraded bottom layer with increasing number of QDC layers and the non-coupling nature of the QDC stacks. Only by increasing excitation power density until the top-most QDC layer is saturated do PL signatures from the bottom layers appear—without state-filling effects in the top-most QDC layer. The extended wavefunctions of the ES are responsible for enhanced carrier tunnelling from the high-energy top layer to the low-energy bottom layer. This unique evolution of spectral changes with increased excitation power can be used to identify carrier transfer among stacks of dissimilar-sized nanostructures.

Acknowledgments

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A Self-Aligned High-Mobility Graphene Transistor: Decoupling the Channel with Fluorographene to Reduce Scattering

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Graphene is a semi-metal with a small overlap between the valence and the conduction bands (zero bandgap material). Despite not having a bandgap, graphene shows potential for next-generation electronic and optoelectronic devices due to some of its outstanding properties such as optical transparency, mechanical flexibility, and high carrier mobility.^[1–9] Considering the fermion nature of the carriers in graphene, the carrier mobility in graphene has been reported to be as high as $200\,000\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$.^[10,11] However, these experimental values for mobilities are orders of magnitude lower than expected. These discrepancies are usually explained as being due to interactions with underlying substrates that lead to surface roughness,^[12] impurities,^[13–15] or surface phonon of silicon dioxide.^[16,17] In order to decouple the current carrying channels of graphene channel from detrimental scattering effects, there have been reports on the use of suspended graphene that shows very high mobility.^[11,18,19] Nevertheless, from a technological point of view, this suspended graphene approach has severe limitations in terms of device architecture and functionality. As a result, researchers still endeavor to overcome

degradation caused by the interactions between graphene and substrates by using a passivation layer between the graphene channel layer and the supporting silicon oxide substrate. In this approach, the passivation layer must be chosen carefully in order to provide a viable alternative for reducing charged impurity scattering. Recently, hexagonal boron-nitride (h-BN), a bi-dimensional (2D) crystal with a lattice constant very close to graphene, has proved to be a good match owing to its smooth morphology, limited density of dangling bonds, and little charge trapping. These characteristics of h-BN lead to dramatic improvements in the transport properties of graphene.^[20–23] It should be noted that these properties are usually measured on back gate devices. Moreover, it is still difficult to manufacture large area, high-quality large-size h-BN. By contrast, alternative choices for passivation layers such as self-assembled monolayers (SAMs) offer advantages including the fact that SAMs are ultrathin organic films that reconstruct at the interface of the substrate and organosilanes through physical and chemical reactions^[24–26] and their deposition is wafer-scale compliant. It has been demonstrated that SAMs modify the wettability of the underlying substrates and substantially enhance the transport properties of graphene^[27–31] even competing with graphene on high-quality h-BN flakes.^[23,27] The major obstacle to overcome in order to use SAMs functionalized substrates as a passivation layer^[32] is the complexity of the process substrate preparation.

Fluorographene is one of the thinnest insulators known to date, indeed it consists of only one or few layers of fluorinated graphene (FG) and is therefore regarded as a functional 2D material. Whereas the mechanical properties are similar to pristine graphene, the electronic properties on the other hand can be modulated from a semi-metal to insulator by tuning the stoichiometry (i.e., the carbon-to-fluorine ratio, C/F).^[33] Theoretical calculations show that the partial fluorination of graphene from C_{32}F to C_4F allows the modulation of the bandgap from 0.8 to 2.9 eV, respectively. Several experimental results have supported these observations.^[34–36] Recently, we have successfully developed a unique heterostructure composed of a semi-metal/semiconductor/insulator, directly formed using a transferred monolayer of graphene and implementing a selective fluorination process.^[37] We also demonstrated the utilization of FG as a gate dielectric.^[38] This technology has strong potential for integrated 2D materials based nanoelectronics. In this work, we present a novel, fast, and efficient method to passivate silicon dioxide substrates (SiO_2) by forming FG on the substrate surface by CF_4 plasma treatment. We studied the FG/CVD-graphene heterostructure using contact angle measurements, Raman spectroscopy, and X-ray photoemission

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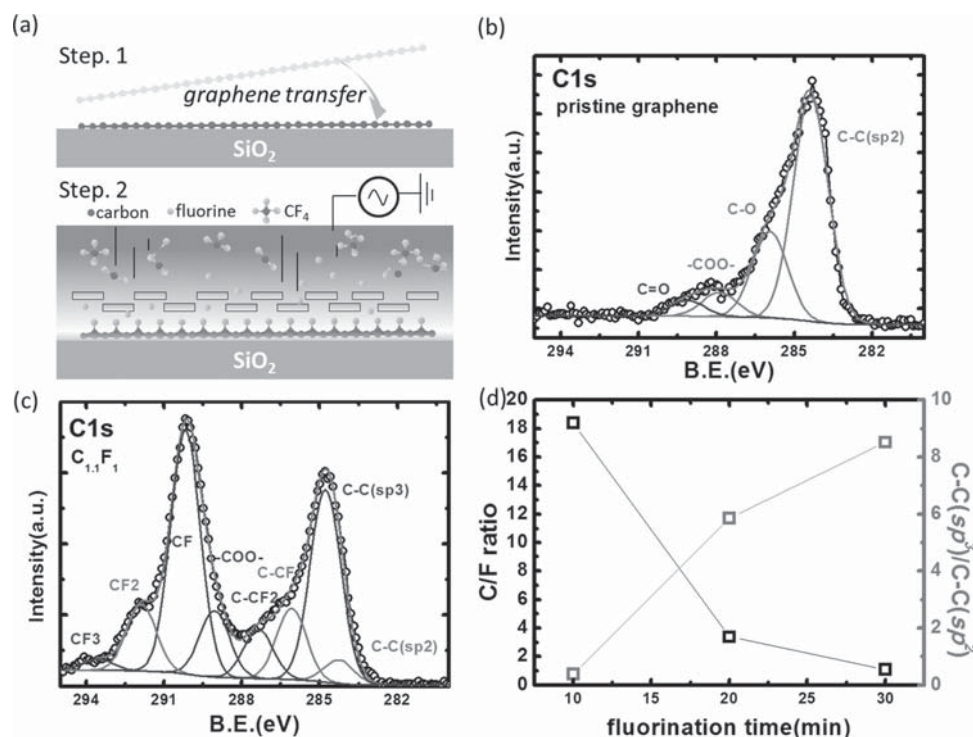


Figure 1. a) Schematic of the fabrication of the fluorinated graphene substrate. b) Deconvoluted C1s spectra for PG. c) Deconvoluted C1s spectra for PG after 30 min fluorination. d) C/F and C-C(sp^3)/C-C(sp^2) ratios as a function of the fluorination time.

spectroscopy (XPS). The fluorination process renders the graphene more hydrophobic and transforms the sp^2 bonding configuration into sp^3 configuration. We also measured a three times gain in the field-effect mobility μ by tuning the C/F ratio. We implemented these observations into the fabrication process of a self-aligned transistor where the gate was deposited at the last step as opposed to standard processes. Our gate-terminated self-aligned transistor further improves the overall performance by limiting the series access resistances and achieves a high carrier mobility $\approx 3000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, comparable to typical chemical vapor deposition graphene (CVD-graphene) on high-quality SAMs^[39] and on h-BN.^[40] As a result, we demonstrate that the FG passivation layer is a versatile and reliable option to improve the performance of graphene-based electronics.^[20,41]

Figure 1a illustrates the fabrication and the fluorination processes of the test structures investigated. First, monolayer CVD graphene was transferred onto a silicon substrate oxidized with 300 nm SiO_2 . The graphene was subsequently exposed to a low-damage CF_4 plasma for various durations.^[37] Figure S1 in the Supporting Information illustrates the CVD and fluorination process. Note that this methodology can easily be reproduced, as it requires only mainstream equipment and one graphene source. Following the fluorination, we carried out XPS measurements. Figure 1b,c shows the deconvoluted XPS analysis for the pristine graphene (PG) and 30 min FG, respectively. The C–O bonds observed on the PG are due to oxygen contamination. The remaining data including F1s spectra are shown in Figure S2 in the Supporting Information. The C1s spectra can be fitted with various bonding configurations assigned to the C–C (sp^2) bond and C–C (sp^3) bond located at 284.4 and 284.8 eV, respectively, along with C–CF (286.3 eV),

CF (289.4 eV), CF₂ (292.2 eV), and CF₃ (293.1 eV) labeled in the C1s spectra. We note that the sp^3 content increases with fluorination time along with more creation of defects; this is confirmed with Raman spectroscopy in the next paragraph. In addition, the C/F ratios correspond to 18.4, 3.4, and 1.1 for 10, 20, and 30 min, respectively, Figure 1c. The highly fluorinated sample, i.e., C/F ratio of 1.1, indicates the formation of double-side fluorinated graphene, suggesting the diffusion of the F atom from the surface toward the interface of graphene/ SiO_2 through the graphene boundary.^[38]

Following the fluorination process and XPS analysis, we carried out contact angle measurements in order to estimate the surface modification and the fluorine coverage onto the graphene.^[31] **Figure 2a–d** depicts the contact angles of SiO_2 , $\text{C}_{18.4}\text{F}_1$, $\text{C}_{3.4}\text{F}_1$, and $\text{C}_{1.1}\text{F}_1$ FG substrates. The contact angle increases from 55° to 94° . This indicates that the surface of substrates shifts from hydrophilic to hydrophobic as evidenced by the larger contact angle. Note that the contact angles of $\text{C}_{3.4}\text{F}_1$ FG and $\text{C}_{1.1}\text{F}_1$ FG are both close to 90° . Therefore, $\text{C}_{3.4}\text{F}_1$ FG represents the surface of a graphene film saturated with fluorine^[33] and leads to a similar wettability as for $\text{C}_{1.1}\text{F}_1$ FG. Lee et al. estimated the packing densities of different SAMs and observed a similar trend in contact angle when the surface coverage increased.^[39] Meanwhile, Li et al. also observed a similar saturated phenomenon with C/F ratio saturation in surface friction properties of FG.^[42]

Figure 2e displays the typical spectra over the 1200–3000 cm^{-1} range for the PG and FG. Graphene contributes to Raman spectra with three main peaks: i) D band at $\approx 1350 \text{ cm}^{-1}$ (defect induced mode), ii) G band at $\approx 1590 \text{ cm}^{-1}$ (in-plane vibrational mode), and iii) the 2D band (two-phonon mode) at

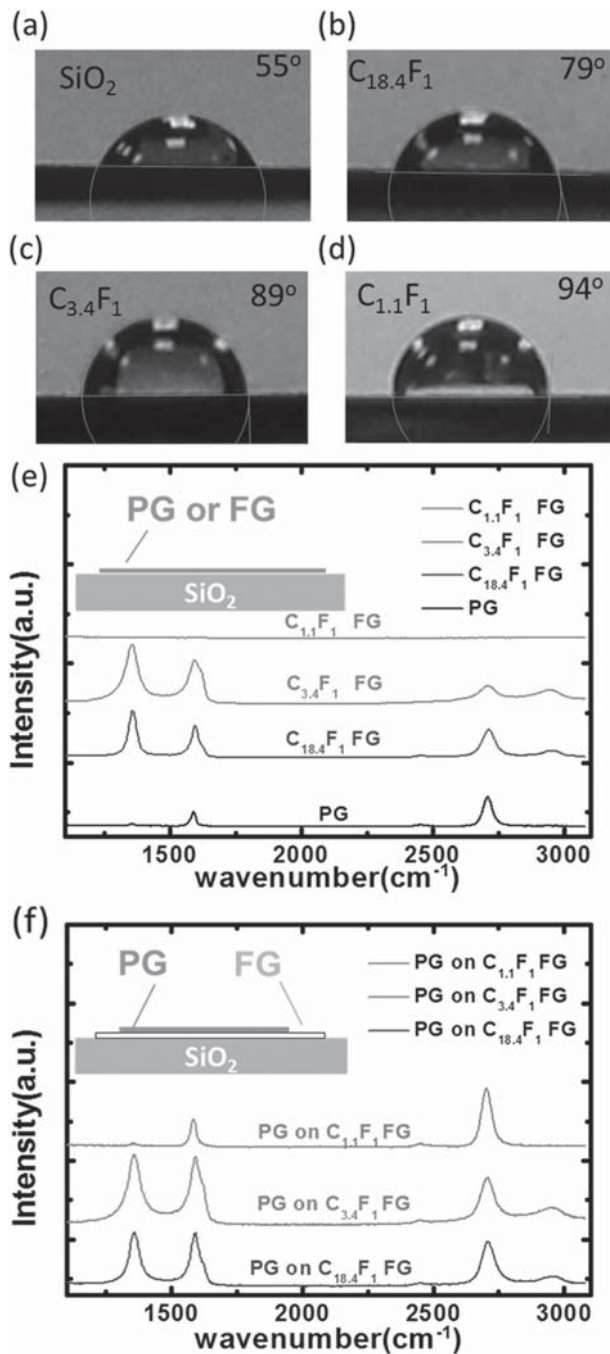


Figure 2. Contact angles measured on a) SiO₂, b) C_{18.4}F₁ FG, c) C_{3.4}F₁ FG, and d) C_{1.1}F₁ FG. e) Raman spectra of pristine and FG on SiO₂ substrate. f) Raman spectra of pristine monolayer graphene (PG) on FG with different C/F ratios.

≈2700 cm⁻¹.^[37] The pristine sample does not present any noticeable D band indicating a low density of defects and a highly crystalline phase. Moreover, the intensity ratio of the 2D over the G peak (I_{2D}/I_G) is about 2.4, evidence of monolayer graphene. While increasing the fluorination time, the D band increases, whereas the 2D band intensity reduces accordingly. The G band is broadened and its shoulder D' peak ≈1623 cm⁻¹ that originates from the intravalley resonance is more pronounced. The

disorder-induced feature in *sp*² carbon associated with defects, i.e., the (G+D) band appears at ≈2950 cm⁻¹. Compared to the pristine sample, both G and 2D bands upshift from 1591 to 1596 cm⁻¹ and from 2712 to 2714 cm⁻¹, respectively, whereas the I_{2D}/I_G ratio decreases with the fluorination time. This indicates a p-type doping. For 30 min fluorination time, all the graphene features disappeared.^[33,43] This latter observation is consistent with the increase in *sp*³ content observed by XPS, Figure 1c.

Figure 2f displays the Raman spectra of a PG monolayer transferred onto FG. The spectrum on the C_{1.1}F₁ FG exhibits a similar feature as graphene on SiO₂ substrate. The intensity ratio of I_{2D}/I_G reduces a little but remains close to 2.2 as for the monolayer graphene on SiO₂. This reduction maybe due to a charge transfer^[44] from or to the C_{1.1}F₁ FG, implying a residual doping,^[39,45] but could also originate from strain. Note that when graphene is transferred onto C_{18.4}F₁ FG and C_{3.4}F₁ FG, the D band is strongly enhanced and the I_D/I_G ratio reduces below 1. For these latest, as the *sp*² structure is to a certain extent maintained (Figure S2a, Supporting Information), we may have in addition a resonant effect due to a twisted bilayer graphene structure.^[46]

In order to investigate the electrical performance of the FG passivation layer, we fabricated a top-gated field-effect transistor (FET) structure and measured the electrical characteristics.^[47] After FG deposition, a second graphene monolayer was transferred onto it. Ni source and drain contacts were then deposited and the channel patterned. 20 nm of aluminum oxide (AlO) was utilized as a gate dielectric followed by an aluminum (Al) gate deposition. The channel length (20 μm) and width (50 μm) were patterned using optical lithography. Figure 3a shows the $I_{DS}-V_{GS}$ characteristic of the graphene-FET for the various FG passivation layers benchmarked with silicon oxide. A photograph of the device is displayed in the inset. The graphene directly on SiO₂ is affected by the charged impurities in the oxide and therefore the transport in the graphene suffers from scattering mechanisms.^[39,48] The $I_{DS}-V_{GS}$ characteristics of graphene on SiO₂ exhibits an asymmetry and p-type doping feature, Figure 3a. Several devices have been tested to extract statistics. V_{Dirac} errors bars on the different substrates are shown in Figure 3b, left axis. The V_{Dirac} of graphene on SiO₂, C_{18.4}F₁ FG, C_{3.4}F₁ FG, and C_{1.1}F₁ FG are, respectively, 1.5, 2.5, 2.5, and 1.6 V. This trend indicates a p-type doping as observed on Raman shifts. In addition, we have benchmarked the leakage current of the devices with FG passivation to SiO₂, Figure S3 in the Supporting Information. We observe that the leakage current is stable whatever the passivation and fivefold lower than the drain current indicating that the FGs do not present any leakage path. In a previous work, we demonstrated the integration of FG as a gate insulator as well and achieved a gate leakage of 500 pA much less than the drain current.^[38] This is evidence of the insulating property of the FG layer as well as its simplicity. From the $I_{DS}-V_{GS}$ characteristic, we evaluate the carrier mobility of the devices using Equation (1):

$$\mu = (L/W C_{ox} V_{DS}) (dI/dV) \quad (1)$$

where L is channel length and W is channel width as well as $V_{DS} = 0.5$ V, $C_{ox} = 100$ nF cm⁻², and dI/dV is the slope of the linear regions of the $I_{DS}-V_{GS}$ characteristics. The measured

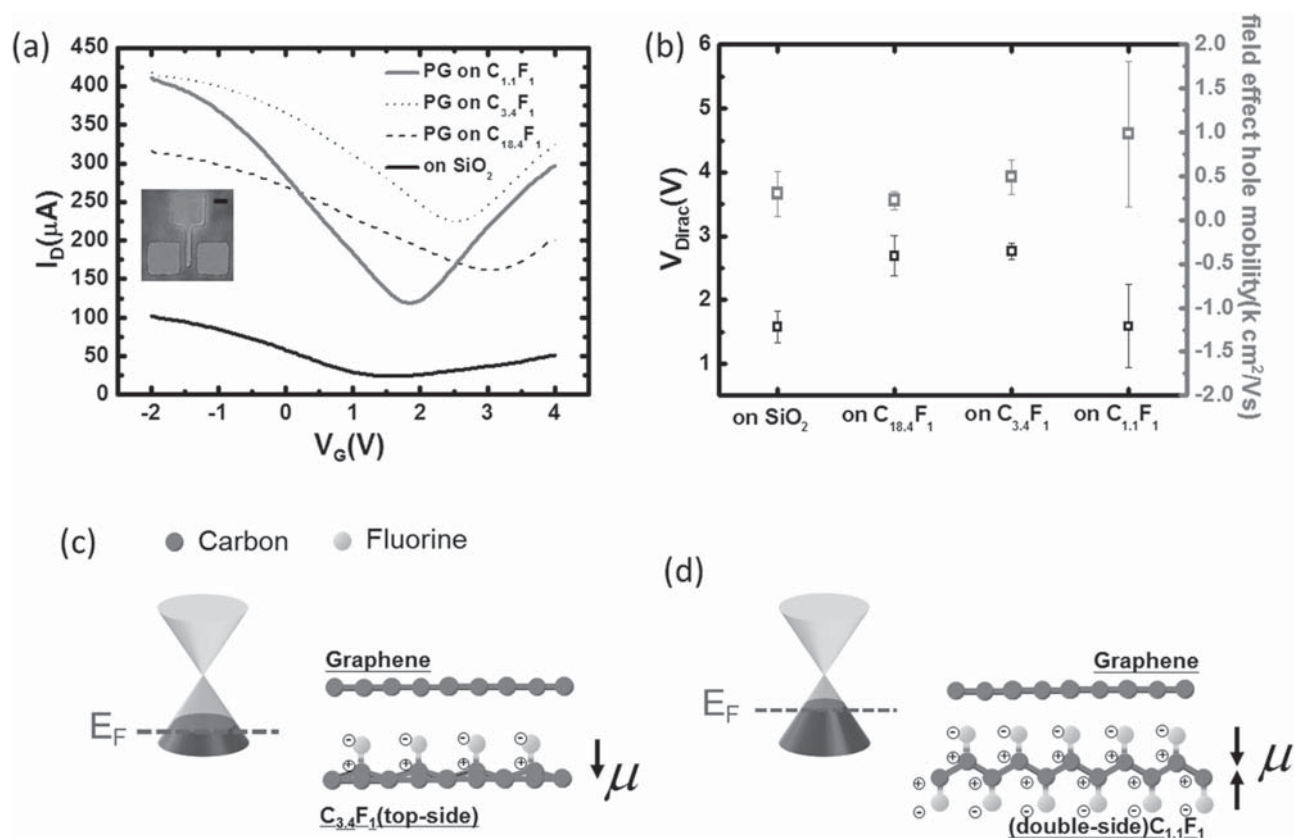


Figure 3. a) I_D - V_G characteristics of the top gate graphene-FET fabricated on FG substrate. The inset shows a photograph of the device under test. The scale bar in the inset is 50 μm . b) Comparative plot of the V_{Dirac} voltages and hole field-effect mobility as a function of the fluorination. c) Illustration of the dipole formation for $\text{C}_{18.4}\text{F}_1$ FG and $\text{C}_{3.4}\text{F}_1$ FG. d) Dipole formation for $\text{C}_{1.1}\text{F}_1$ FG. The black arrow indicates the orientation of the dipole moment μ . The Dirac cones depicted show the variation of the Fermi level induced by the charge transfer.

capacitance density is displayed in Figure S4 (Supporting Information). Surprisingly, the mobility improves as the V_{Dirac} increases with the fluorination, as opposed to usual trend observed elsewhere,^[27,31,39,49] but in this work the FG acts as a passivation and not the channel and therefore one should consider the total electrostatic picture of the graphene/FG/ SiO_2 system, i.e., graphene/dipole/ SiO_2 .^[50] In our study, both SiO_2 and the graphene channel are identical for all samples and therefore should present the same charge impurities in SiO_2 , and charged or dipolar functional groups on graphene because of unintentional atmospheric contamination (see Figure 1b). These C-O based functional groups are known to be holes donors; they alter the local electric field on the graphene channel and therefore its conductivity. The graphene sheet exhibits a given electrostatic potential. This picture is the same for all our samples. However, once the FG passivation is introduced the electrostatic potential is perturbed and the presence or absence of a dipole moment at the FG/graphene interface will affect the charge transfer occurring through the FG/graphene/adsorbates system.

In that regard, it has been demonstrated that the fluorination coverage translates into different F bonding configuration with C and therefore different dipole moment, μ .^[45,50,51] For low F content, e.g., C_4F , F bonds onto C preferably on one side, whereas for CF coverage, F covers all C atoms but on both side of the graphene sheet.^[52] For the later configuration that is

close to our $\text{C}_{1.1}\text{F}_1$ FG, the opposite dipole moments cancel out. Experimentally, we observe a ≈ 1 V increase in the V_{Dirac} voltage for both $\text{C}_{18.4}\text{F}_1$ FG, $\text{C}_{3.4}\text{F}_1$ FG. These two FGs as opposed to $\text{C}_{1.1}\text{F}_1$ FG present a dipole moment that facilitates the transfer of holes from the adsorbed contamination to the graphene sheet. This translates into a drop of the Fermi level (E_F) in the graphene and as a result in an increase of V_{Dirac} as observed experimentally. Figure 3c,d illustrates the mechanism involved for the different dipole formation. On the other hand, the $\text{C}_{1.1}\text{F}_1$ FG passivation that does not exhibit a net dipole, then the V_{Dirac} is lower. Here, we believe that the absence of net dipole reduces the charge transfer from residual adsorbates and therefore little shift in the E_F is expected as compared to SiO_2 . Indeed, no substantial variation of the V_{Dirac} is visible. The graphene (channel) is seen as decoupled from the SiO_2 substrate through the $\text{C}_{1.1}\text{F}_1$ FG passivation hence the better mobility. Note that the devices with FG passivation exhibit a higher slope, narrower minimum conductivity plateaus, and higher value of the minimum conductivity. This trend relates to a reduction of the scattering mechanisms and clearly indicates that the samples with FG passivation exhibit a lower charged impurity density.^[39,49,53]

As shown in Figure 3b, right axis, the hole mobility of devices on FG is as high as three times enhanced for the lowest C/F ratio from 300 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ on SiO_2 to 1000 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ on $\text{C}_{1.1}\text{F}_1$ FG. The peculiarity of the $\text{C}_{1.1}\text{F}_1$ FG, i.e., C/F ≈ 1 is

that all the fluorine atoms covalently bond to carbon atoms. The theoretical work of ahin et al. demonstrated that FG with $C/F \approx 1$ is an ideal configuration in terms of C to F coverage.^[52] Therefore, we believe that most of scattering centers within the FG are passivated yielding to a better conductivity and a higher mobility.^[39] The improvement compared to an oxide is obvious and scattering mechanisms have definitely been reduced. For this $C/F \approx 1$, the C–F bonds after the fluorination process stand perpendicular to the graphene plane and therefore thicken the graphene monolayer up to 1–1.5 nm.^[33] This distance may be large enough to screen the influence of the charge impurities in the oxide interface on the electrostatic potential at the graphene channel.^[54] On the other hand, for C/F ratios <1 , although we could not experimentally achieve this condition, we speculate that the larger amount of F atoms not bonded to C atoms may behave as dangling bonds and would therefore be detrimental to the conductivity and as a result to the mobility.

Finally, we fabricated a gate-terminated self-aligned field-effect transistor in order to reduce the access series resistances, **Figure 4a**. The details of the device fabrication are described in **Figure S5** (Supporting Information). Although the self-aligned technology for graphene-FET is not introduced first,^[55,56] the advantage of this design relies on the protection by Ni of the channel from photoresist exposure and therefore contamination and doping.^[57]

We carried out Raman spectroscopy measurements to monitor the quality of graphene in the channel regions, **Figure 4b**. Almost no D-peak is visible after the Ni etching and the AlO gate dielectric deposition, indicating the low defects density introduced during this fabrication process. **Figure 4c** shows the

electrical characteristics of the self-aligned graphene-FET with the $C_{1.1}F_1$ FG passivation.

The self-aligned process enhances the carrier mobility more than six folds from $\approx 300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ on SiO_2 to $1800 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ on SiO_2 with self-aligned process. The introduction of the FG passivation further improves the mobility up to $\approx 3000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. The FG passivation layer also induces a 50% enhancement in the drain current and an on/off ratio increasing from ≈ 2.4 (SiO_2) to ≈ 3 ($C_{1.1}F_1$ FG).

A comparison of the mobility enhancement on various substrates and graphene synthesized methods is shown in **Table S1** (Supporting Information). Exfoliated graphene presents mobility superior to $40\,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ on exfoliated h-BN, whereas it can reach $\approx 40\,000$ to $60\,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ with SAMs functionalized substrates, e.g., octadecyltrimethoxysilane (OTMS).^[27] However, the exhausting exfoliation process compromises the scalability of this route. On the other hand, the time-consuming fabrication process for completing octadecyltrichlorosilane (OTS),^[31] OTMS,^[27] or phenyl-alkyl-terminated(phenyl-SAM)^[29] is a major drawback. Recently, significant efforts have been devoted to synthesize CVD h-BN to become comparable with exfoliated h-BN.^[53] Therefore, CVD h-BN can be regarded as a potential candidate for the substrate passivation. However, in this case, the ability to process CVD h-BN remains challenging, as it requires the growth of two different materials to fabricate a device (h-BN and graphene).^[58] By contrast, FG is readily prepared after a unique growth of graphene and exposure to appropriate CF_4 plasma, which is mainstream CMOS technology.^[59–61] This latest procedure could easily be introduced in a large-area roll-to-roll fabrication

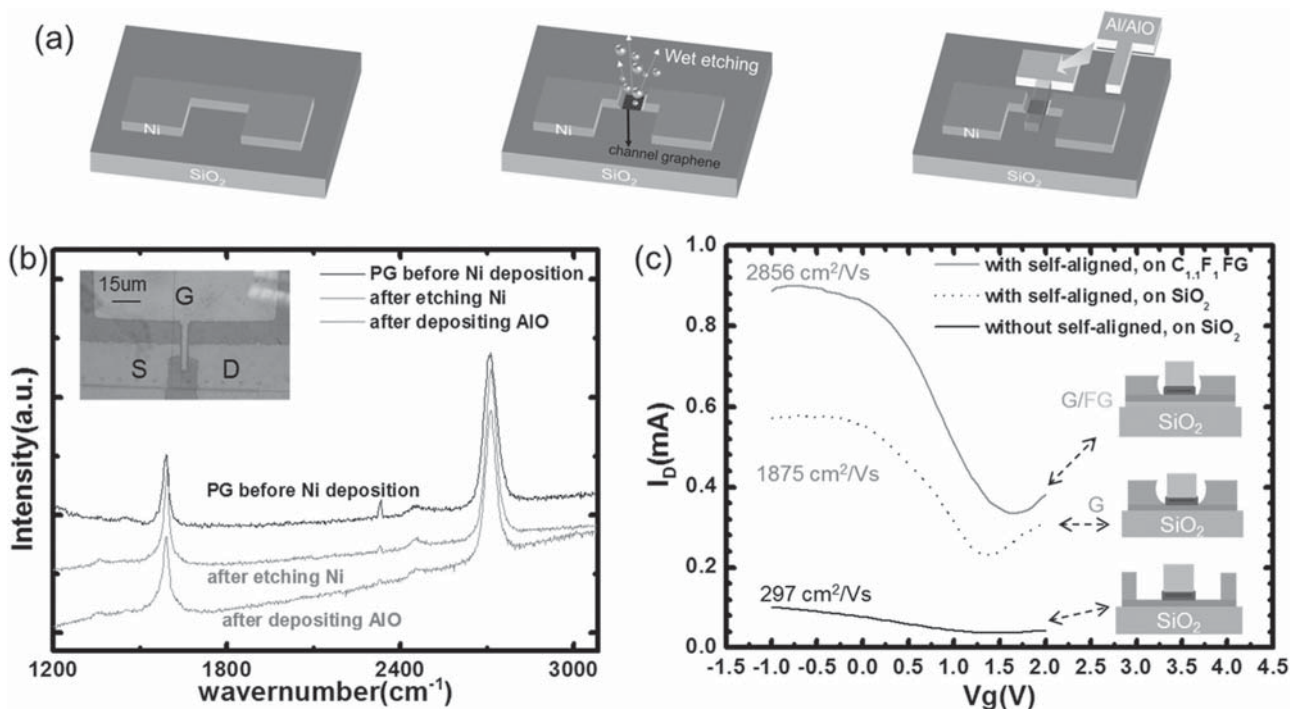


Figure 4. a) Illustration of the fabrication steps of a gate-terminated self-aligned FET. b) Raman spectra on the channel region after each processing steps. The inset is the optical photograph of the gate-terminated self-aligned FET. c) $I_{D5}-V_{G5}$ characteristic of the devices fabricated with and/or without self-aligned design and FG passivation layer.

process.^[1] Note that the best performances in Table S1 (Supporting Information) are achieved on back gate devices with large grain and often exfoliated materials, i.e., perfect lattice. It is important to point out that the grain size of the CVD graphene channel as well as the size and configuration of the test structure play an important role to achieve large mobility.^[23,53] Our CVD graphene presents grains of 1–3 μm in size and our devices are typically $\approx 10 \mu\text{m} \times 4 \mu\text{m}$. This implies that the graphene channel is composed of a few grain boundaries that inherently affect the mobility. Nevertheless, the design of a gate-terminated self-aligned FET allows to attain mobility competitive with bottom-gate CVD-graphene FET on exfoliated h-BN^[23] and on SAMs^[29,39] using standard CMOS technology and IC architectures. Therefore, we believe that there is room for a significant improvement in the carrier mobility implementing the same methodology but using larger grain CVD graphene. This technology offers a viable and cost effective route for the large-area graphene-based device integration.

In summary, we investigated the passivation strength of fluorinated CVD graphene monolayer on a gate-terminated self-aligned transistor. The electrical properties of the FG passivation layer were assessed on top gate devices and pristine graphene on the saturated $\text{C}_{1.1}\text{F}_1$ FG passivation exhibited the largest mobility due to reduction of scattering mechanisms. We also fabricated a gate-terminated self-aligned FET with the $\text{C}_{1.1}\text{F}_1$ FG as a passivation layer. As a result, this device exhibits a tenfold mobility enhancement $3000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ compared to nonself-aligned devices on SiO_2 as well as a 50% current enhancement. We demonstrated that fluorographene to be an effective passivation layer implemented with self-aligned technology and a competitive route compared to current CVD graphene on h-BN or SAMs. This process is fast, scalable, and easily applicable for the study of the electronic properties of bidimensional heterostructures.^[48]

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Tuning the work function of monolayer graphene on 4H-SiC (0001) with nitric acid

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Abstract

Chemical doping of graphene is a key process for the modulation of its electronic properties and the design and fabrication of graphene-based nanoelectronic devices. Here, we study the adsorption of diluted concentrations of nitric acid (HNO₃) onto monolayer graphene/4H-SiC (0001) to induce a variation of the graphene work function (WF). Raman spectroscopy indicates an increase in the defect density subsequent to the doping. Moreover, ultraviolet photoemission spectroscopy (UPS) was utilized to quantify the WF shift. UPS data show that the WF of the graphene layer decreased from 4.3 eV (pristine) down to 3.8 eV (30% HNO₃) and then increased to 4.4 eV at 100% HNO₃ concentration. These observations were confirmed using density functional theory (DFT) calculations. This straightforward process allows a large WF modulation, rendering the molecularly modified graphene/4H-SiC(0001) a highly suitable electron or hole injection electrode.

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Keywords: graphene, work function, doping, Raman spectroscopy, UPS spectroscopy, DFT calculations

Introduction

Graphene is a 2D-material combining various outstanding properties in a single material, such as the quantum Hall effect or massless Fermions, among others [1, 2]. Its high mobility, optical transparency, along with its flexibility, high mechanical strength and environmental stability make it a very attractive material for a broad range of applications [3, 4]. Graphene can also be exploited for precise metrological applications, as it has been demonstrated recently with exceptionally accurate measurements of the quantum Hall resistance quantization [5, 6]. In order to implement the potential of such a material into viable applications, large-

scale wafers of high quality graphene grown on insulating substrates are required for device integration [7, 8]. Moreover, to achieve performant devices, the electronic properties of the material must be modulated [9–11]. In that respect, the work function (WF) is a remarkable property that can be tuned for various optoelectronic applications, like transparent electrodes for optoelectronic devices, or multiple tunnel heterostructures matching the energy offsets of common transport materials, to achieve low and/or large charge injection barriers [12]. To reach this goal, the modification of the work function of graphene has to be obtained without damaging the overall characteristics of the material. A possible approach to vary the WF is to modify the surface by depositing a

monolayer of a molecular donor or acceptor. Recent studies have demonstrated possible WF variations using tetrafluoro-tetracyanoquinodimethane (F4-TCNQ), gold colloids or metals as acceptor materials [13–15] for example. Although these methods have demonstrated WF modulation, they present major drawbacks. For example, the transparency of graphene is reduced, which represents a strong limitation for optoelectronic applications where graphene could play a role. In addition, these adsorbed elements create scattering interfaces that may severely affect the transport properties of graphene. Finally, deposition and temperature dependence are potential limitations for the device fabrication process. Among the dominant graphene synthesis methods, chemical vapor deposition (CVD) and epitaxy on SiC substrate are the leading technologies in terms of scale and properties. For electronic applications, the growth of graphene by CVD on metals requires transferring the graphene onto an insulating substrate. This last operation involves chemicals such as PMMA and copper etchant known to induce a *p*-type doping of the material [16]. Although this approach allows the transfer of graphene on any functional substrate, the electronic properties of the graphene sheet are altered by these manipulations. Furthermore, epitaxial graphene on hexagonal silicon carbide (SiC) wafers presents homogeneous films with large areas and high electron mobility [17]. The SiC substrate is suitable for optoelectronic applications since it is transparent over a very broad frequency spectrum. It has a large thermal conductivity, and is compatible with high-frequency devices where losses due to residual conductivity of the substrate have to be minimized by using insulating materials. We have recently demonstrated the WF modulation on tri-layer graphene on SiC (0001) using *in situ* nitrogen flux [18]. Furthermore, Das *et al* have demonstrated that nitric acid (HNO₃/NA) on CVD graphene is an efficient doping agent inducing *p*-type variation of the WF [19, 20].

In this work, we have monitored the structural and electronic modifications of epitaxial graphene for different concentrations of diluted nitric acid (NA) 15 vol% (NA15), 30 vol% (NA30), 70 vol% (NA70) and 100% (NA100) of nitric acid (NA) solutions in deionized water (DI water) for 2 min. The electronic properties of the doped graphene samples were characterized by Raman spectroscopy. The changes in work function after NA doping were measured using ultraviolet photoemission spectroscopy (UPS). Based on these observations, the influence of NA doping on graphene's work function is discussed. To highlight the effect of nitric acid doping, these measurements were compared with the obtained values for pristine graphene. We demonstrate in the present work that the NA doping permits the WF modulation with respect to the dilution. Indeed, the WF first increases the electronic doping between 15 and 30 vol% (NA15, NA30) and then decreases the electronic doping between 70 and 100 vol% (NA70, NA100). This study on epitaxial graphene presents striking differences compared to the work of Das *et al* on CVD graphene where only *p*-type work function shifts are observed. We clearly demonstrate that both systems react differently to an identical chemical functionalization. These observations are supported by density functional theory calculations (DFT).

Experimental section

The graphene was grown on semi-insulating SiC(0001) substrates [17, 21]. The SiC sample was then heated to 1000 °C in a UHV chamber and further heated to 1525 °C in an Ar atmosphere to favor the formation of a large and homogeneous graphene layer. The substrate was then cooled down from 1525 °C to room temperature [18, 22]. The samples were subsequently transferred *ex situ* from the growth chamber to the AFM microscopy, Raman spectroscopy and UPS measurement systems.

The morphology of the nitrogen-doped epitaxial graphene was studied after growth by atomic force microscopy (AFM). The Raman measurements were carried out with a frequency-doubled NdYag laser operating at 532 nm as an excitation source with up to 20 mW continuous wave output power. The spectra were recorded through a 300 mm imaging spectrometer equipped with both a 600 lines/mm and 1800 lines/mm grating, and a back-illuminated CCD. A 100× objective with respective numerical apertures of 0.9 and 1.4, and a 50 μm core diameter multimode fiber acting as a pin-hole, were used to collect the signal. The expected lateral spatial resolution in the *x*–*y* plane can reach 150 nm (num app = 1.4) and 250 nm (num app = 0.9). Particular attention was paid to the incident laser power density to prevent local heating effects that may induce a shift of the Raman peaks. UPS measurements for the study of the work function have been performed using a PHI 5000 Versaprobe spectrometer (Physical Electronics) operating at a base pressure of 10^{−9} mbar, using a He I discharge lamp ($h\nu = 21.2$ eV).

Results and discussion

The typical morphology of the graphene sample is displayed in the AFM images of figure 1. The step direction and terrace width were determined by the incidental misorientation of the substrate surface with respect to the crystallographic (0001) plane. The surface is highly uniform over a large scale with atomically flat, 3 μm large terraces and 1.8 nm high steps. On defect-free areas of the sample, the terraces typically extend undisturbed over 50 μm in length. In AFM phase mode (figure 1(b)), the homogeneous contrast indicates the thickness homogeneity that corresponds to a graphene monolayer.

Figure 2 displays the typical spectra over the range 1200–3000 cm^{−1} of the pristine graphene and NA doped graphene samples [23]. For each sample, to reduce the possible errors affecting the peaks' positions and the intensity due to local inhomogeneity, we collected the average Raman spectra over an area of 1 μm², before (pristine) and after the doping. We observed the main features of graphene as well as the second-order Raman signal that originates from the SiC substrate visible between 1200 and 3000 cm^{−1}. Graphene contributes to Raman spectra with three main peaks: (i) a D band at ~1350 cm^{−1} (defect-induced mode), (ii) a G band at ~1590 cm^{−1} (in-plane vibrational mode) and (iii) the 2D band (two-phonon mode) at ~2700 cm^{−1} [24, 25]. The pristine sample does not present any noticeable D band

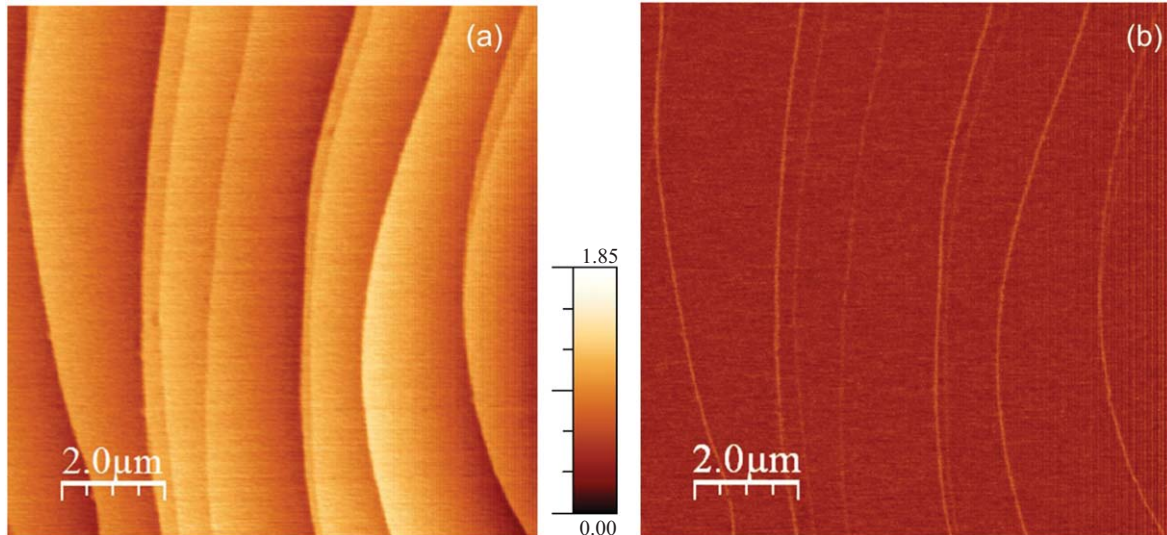


Figure 1. (a) and (b) AFM topography and phase of the pristine graphene sample.

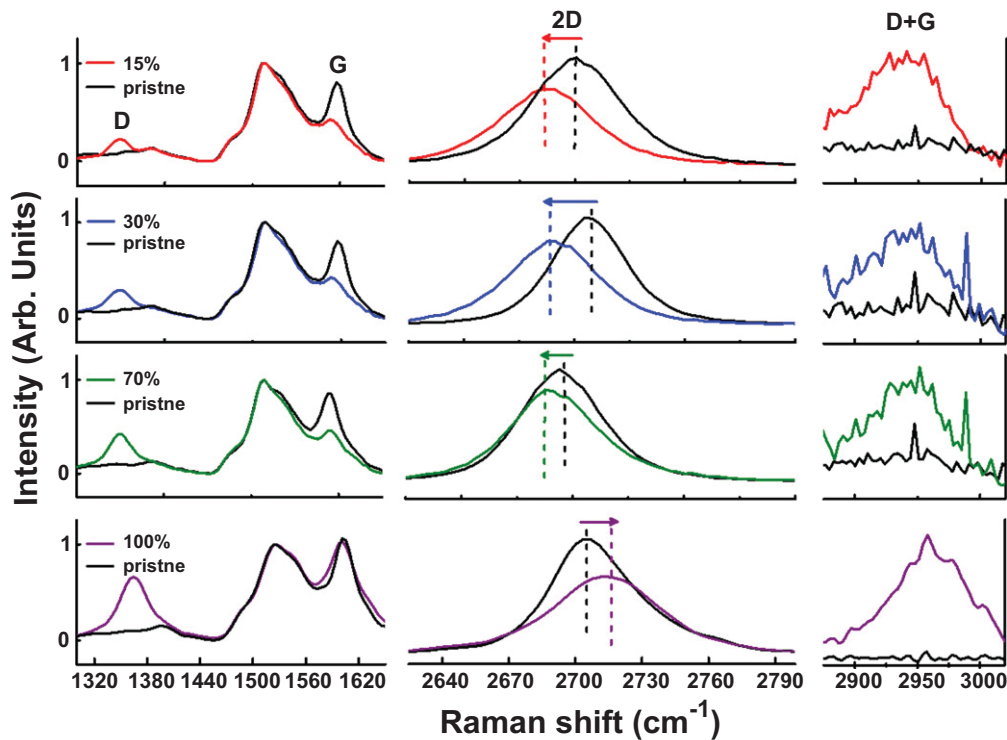


Figure 2. Raman spectra of pristine, NA15, NA30, NA70 and NA100 samples. A D peak magnitude appears with NA concentration indicating the creation of defects due to nitrogen incorporation. (G + D) band indicate a similar effect. Raman shifts indicated by arrows evidence the doping trends. The presence of the G and 2D bands across the overall area indicates homogeneous growth of graphene.

indicating a low density of defects and a high crystalline phase i.e. I_D/I_G ratio ~ 0.13 . On the other hand, all NA doped samples exhibit a higher intensity D band. The I_D/I_G ratio increases from ~ 0.13 for the pristine sample to an average of 2.5 for doped samples confirming the alteration of the structure after NA dip. In addition, we note the appearance of a (G + D) band $\sim 2950 \text{ cm}^{-1}$ caused by the disorder-induced feature in sp^2 carbon associated with defects. The 2D band full width at half-maximum (FWHM) increases from 35 cm^{-1}

for the pristine sample to an average of 42 cm^{-1} for NA15, NA30 and NA70, and raised to 50 cm^{-1} for the maximum doping for NA100. These Raman shifts clearly indicate a doping effect induced by the NA dip at various concentrations. The bending of the graphene sheet at the kinks of the terraces induces local physical stress on the carbon atoms of the graphene layer that results in an increase in the chemical reactivity of these atoms, and then we can suppose that the incorporation of dopants occurs at the edge states of the

epitaxial graphene [26, 27]. Moreover, it has been demonstrated that in addition to doping, step bunching at the step edges causes conductance anisotropy. We have confirmed that on a pristine sample using conductive-probe atomic force microscope (CP-AFM, figure SI-1), we observe an increase in the contact resistance consistent with previous studies [28–31], however we could not resolve a significant change after doping.

In order to discriminate the competition between step edges and terraces in the process in the HNO₃ adsorption, we have carried out resolved Raman mapping on pristine and NA15-doped samples (figure SI-2). The Raman mapping of the D peak indicates an enhanced intensity at the step edges as opposed to the terraces. The Raman spectra extracted for both the step edge and the terrace indicate a larger D peak at the step edge and a shoulder $\sim 1620\text{ cm}^{-1}$ assigned to the D' peak. In addition, the D + G peak $\sim 2925\text{ cm}^{-1}$ is prominent for the step edge signature. These features are clear evidence of increased disorder and support our hypothesis that the step edges are preferential sites (but not exclusive) for the incorporation of N atoms. We have previously evidenced that the N incorporates into graphitic, pyridinic and pyrrolic configurations [18, 22]. Note that in this study, our XPS experiments (figure SI-3) show that the N does not intercalate at the interface and is effectively bonded to the carbon lattice [32].

We observe that, for the NA15 sample, the position of the G band before and after doping is within the resolution of the Raman system i.e. $\sim 1\text{ cm}^{-1}$. However, there is a red shift of 14 cm^{-1} in the position of the 2D band assigned to an *n*-type doping. The defect-induced D band also increases with respect to the pristine sample as expected for doped samples. In the case of the NA30 sample, we note a significant red shift for both the G band and the 2D band positions, of 8 and 19 cm^{-1} respectively, showing a strong *n*-type doping behavior [33]. The D band also shows a prominent intensity increment after doping with NA30, which is due to the *sp*³-activation by nitrogen intercalation in the conjugated *sp*² network of graphene. Note that the epitaxial graphene is intrinsically *n*-doped due to the charge transfer occurring from the SiC substrate through the interface layer [34]. This point will be further discussed in the UPS section. NA70 sample does not present a relevant shift in the G band position. However, the red shift of the 2D band is reduced to 6 cm^{-1} , denoting a reduced *n*-type doping effect as opposed to NA15 and NA30. NA100 shows a different behavior as the G band position remains stable but the 2D band exhibits a blue shift of 11 cm^{-1} indicating *p*-type like doping [35]. We believe that this effect at high NA concentrations results from a balance between two different simultaneous effects, i.e. *p*- and *n*-type doping from physisorption of the molecules and nitrogenation reactions near the terraces, respectively.

To evaluate the electronic quality of our graphene layers, we determined the carrier mobility of the pristine and NA100% doped graphene using van der Pauw measurements at room temperature. Table 1 shows the electrical data measured for the pristine sample and NA100 extracted from Hall measurements. We have measured in previous works the electronic properties on such a monolayer graphene using the

Table 1. Electrical data extracted from Hall effect measurements on pristine and NA100% sample.

	Sheet resistance ($\Omega\text{ cm}^{-2}$)	Carrier density (cm^{-2})	Mobility ($\text{cm}^2\text{ V}^{-1}\text{ s}^{-1}$)
Pristine	800	9×10^{12}	2500
NA100	500	6×10^{12}	1700

same growth mechanism with hydrogen, nitrogen introduced *in situ* and ammonia (liquid or vapor) as doping media [18, 22]. The measurements showed outstanding properties including the quantum Hall effect and a high mobility that reached up to $11\,000\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ at 1.7 K for carrier density $\sim 10^{12}\text{ cm}^{-2}$. The lowest mobility achieved was $1400\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ at 300 K [17]. Note that Günes *et al* [14] achieved a sheet resistance of $100\Omega/\square$ using HNO₃ doping on CVD graphene. These data clearly indicate that although doping alters the lattice of graphene to some extent, it does not render the material electronically poor. The orders of magnitude are sufficient for many mainstream applications where contacts are required [36, 37].

For that purpose, and to complete the picture of the electronic properties of doped monolayer epitaxial graphene, we performed UPS measurements in order to monitor the WF as a function of the NA concentration. The UPS spectra around the secondary electron threshold region of the graphene layer treated by NA solutions are shown in figure 3(a). The secondary electron threshold was determined by extrapolation between the background and straight solid lines in the secondary electron threshold region of the UPS spectra. The work function was determined from the secondary electron threshold using the equation $\Phi = h\nu - E_{\text{th}}$, where $h\nu$ and E_{th} are the photon energy of excitation light (He I discharge lamp, 21.2 eV) and the secondary electron threshold energy, respectively. The plot in the upper-right panel of figure 3(a) is a close up of the UPS spectra of the graphene layer treated by NA solutions around the Fermi level. The zero binding energy (BE) (i.e. the Fermi Level) is taken at the leading edge of a sputter cleaned gold sample [38]. Figure 3(b) shows the work function of pristine graphene and HNO₃-doped graphene. Decomposition of HNO₃ molecules takes place upon the interaction with the graphene layer where the active edge-state electrons play a catalytic role. While the HNO₃ concentration increases, the number of species physisorbed onto the graphene layer increases. The work function of the pristine graphene layer is 4.3 eV as reported by different groups [39, 40]. Subsequently, the work function decreases from 4.3 eV to 4.1 eV after doping with 15% NA. The WF further decreases to 3.8 eV with 30% NA. Note that this reduction implies an *n*-type doping that is consistent with the variation observed in the Raman spectra on figure 2, suggesting an increase of the nitrogen content between pristine and 30% NA. Beyond 30% NA, the WF increases first to 4.05 eV at 70% NA and reaches 4.41 eV for pure NA. For the latter we also observed a blue shift in the Raman spectrum of NA100 confirming a *p*-type doping that

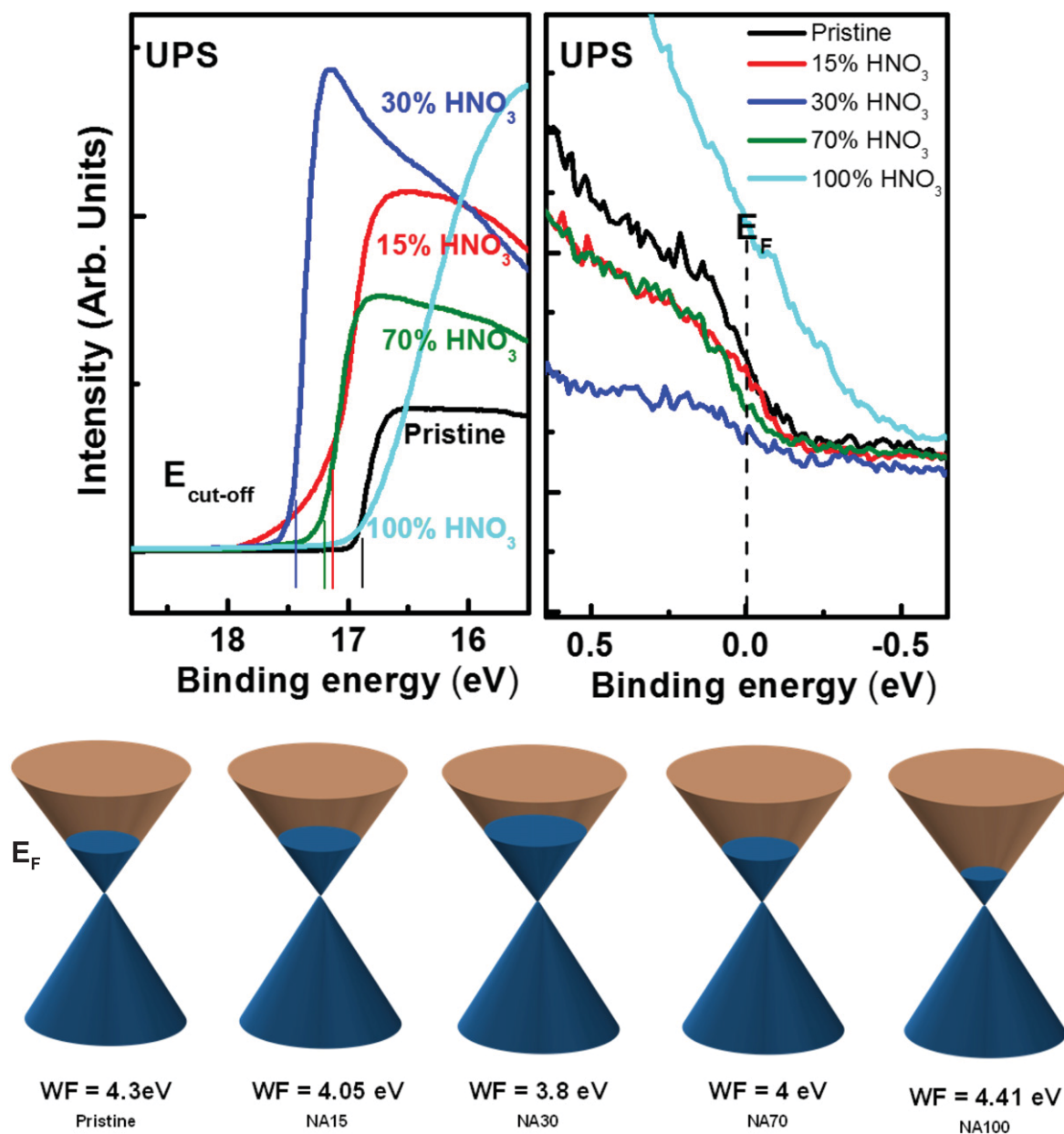


Figure 3. (a) UPS data for pristine, NA30, NA70 and NA100 samples indicating the WF shift as a function of nitric acid concentration. (b) Illustration of the Fermi level shift in the graphene Dirac cones.

compensates the initial *n*-type nature of the sample. The changes of the Fermi level position with the NA concentration are illustrated in figure 3(b). Our results clearly indicate that for low NA concentration, the nitrogenation reduces the WF towards *n*-type doping as the nitrogen content (donor) increases in the sample [41]. This is in contrast to the observation of Das *et al* where the WF presents a monotonic increase as a function of NA%. Note that the graphene utilized here is initially *n*-type due to a residual doping from the SiC substrate. We believe that the first HNO₃ molecules dissociate and saturate all available defect sites or step edges. This induces a nitrogen-doped graphene layer (NA15% and NA30%) and therefore decreases the WF [41]. On the other hand, beyond NA30%, the HNO₃ can physisorb on the surface inducing a *p*-type doping, lowering the Fermi level and

as a result increasing the WF. This was confirmed by *ab initio* calculations describing the electronic structure of graphene on SiC as well as the interaction with the HNO₃ molecules were performed using a very efficient DFT localized orbital molecular dynamic technique (FIREBALL) [42]. Numerical localized orbital basis sets of *sp*³ for C, N, O and Si, and *s* for H were used with spatial cutoff radii (in atomic units) *s* = 4.5, *p* = 4.5 (C), *s* = 4.2, *p* = 4.2 (N), *s* = 3.3, *p* = 3.8 (O), *s* = 4.8, *p* = 5.4 (Si) and *s* = 4.1 (H) [43]. In this study we have considered supercells of 5 ML SiC(0001), with zero-layer graphene and an AB stacked graphene plane on top. The lateral size roughly corresponds to a 4 × 4 unit cell of graphene. The bottom layer is saturated with hydrogen atoms. On top of the supercell, we have set from 1 to 4 HNO₃ molecules per unit cell to observe the graphene doping

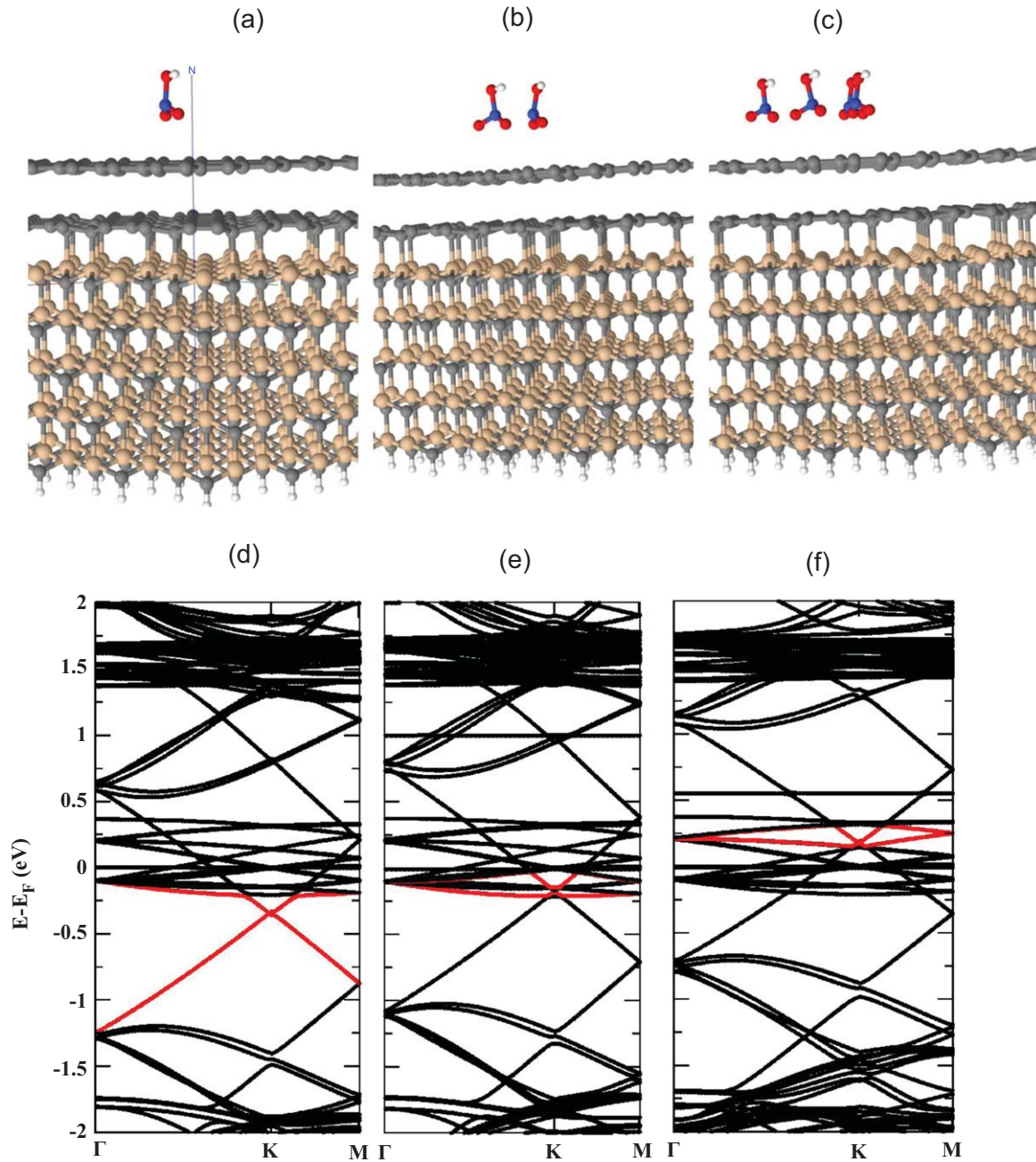


Figure 4. (a), (b), and (c) Atomic structures used for the calculations, considering one graphene layer on top of a SiC(0001) surface with a graphene buffer layer, and one, two and four HNO₃ molecules respectively. (d), (e) and (f) Corresponding band structures showing the evolution of the graphene doping from *n*- to *p*-type. The graphene Dirac cone is highlighted in red for the three configurations.

evolution with the molecular concentration, as represented in figures 4(a)–(c). The geometry of these systems was then relaxed at 0 K, using a sample of 32 k-points in the surface Brillouin zone, as previously used in similar calculations [44], maintaining the last three bottom layers in bulk positions. The equilibrium configuration is obtained when forces are less than $0.01 \text{ eV } \text{Å}^{-1}$. The final distances between the molecules and the graphene plane have been determined using the well-known LCAO-S² + vdW formalism [45–47] which specifically takes into account the van der Waals interaction in the frame of DFT. Finally, a set of 300 special k-points along the Γ –K–M path has been used for the band structure calculations

on the optimized geometries. These calculations aim at reproducing the physisorbed process leading to *p*-doping, as we did not model the graphene terraces. Results of the band structure calculations are represented in figures 4(d)–(f), corresponding to one, two or four deposited HNO₃ molecules. We can observe a variation of the graphene doping from -350 meV for one molecule (which already represents a *p*-type doping with respect to the pristine situation at -400 meV), to -180 meV for two and up to $+190 \text{ meV}$ for four molecules. Consequently, the calculations also confirm a *p*-type doping for the physisorption process in good agreement with the WF variation recorded experimentally.

Conclusions

We have investigated the doping strength of nitric acid on monolayer graphene grown on SiC (0001). The Raman measurements confirm the doping induced by various concentrations of nitric acid and indicate the incorporation of atoms into the graphene lattice. The UPS measurements showed that *n*-type and *p*-type doping are competitive processes and the work function of graphene layer can be continuously tuned from 4.3 eV to 4.4 eV with a minimum of 3.8 eV upon depositing the molecular acceptor HNO₃. This observation is supported by DFT calculations considering the physisorption of HNO₃ molecules. This simple approach allows the modulation of WF and could permit the design of tuneable electrodes to improve the carrier injection as well as band gap-engineered heterostructures.

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